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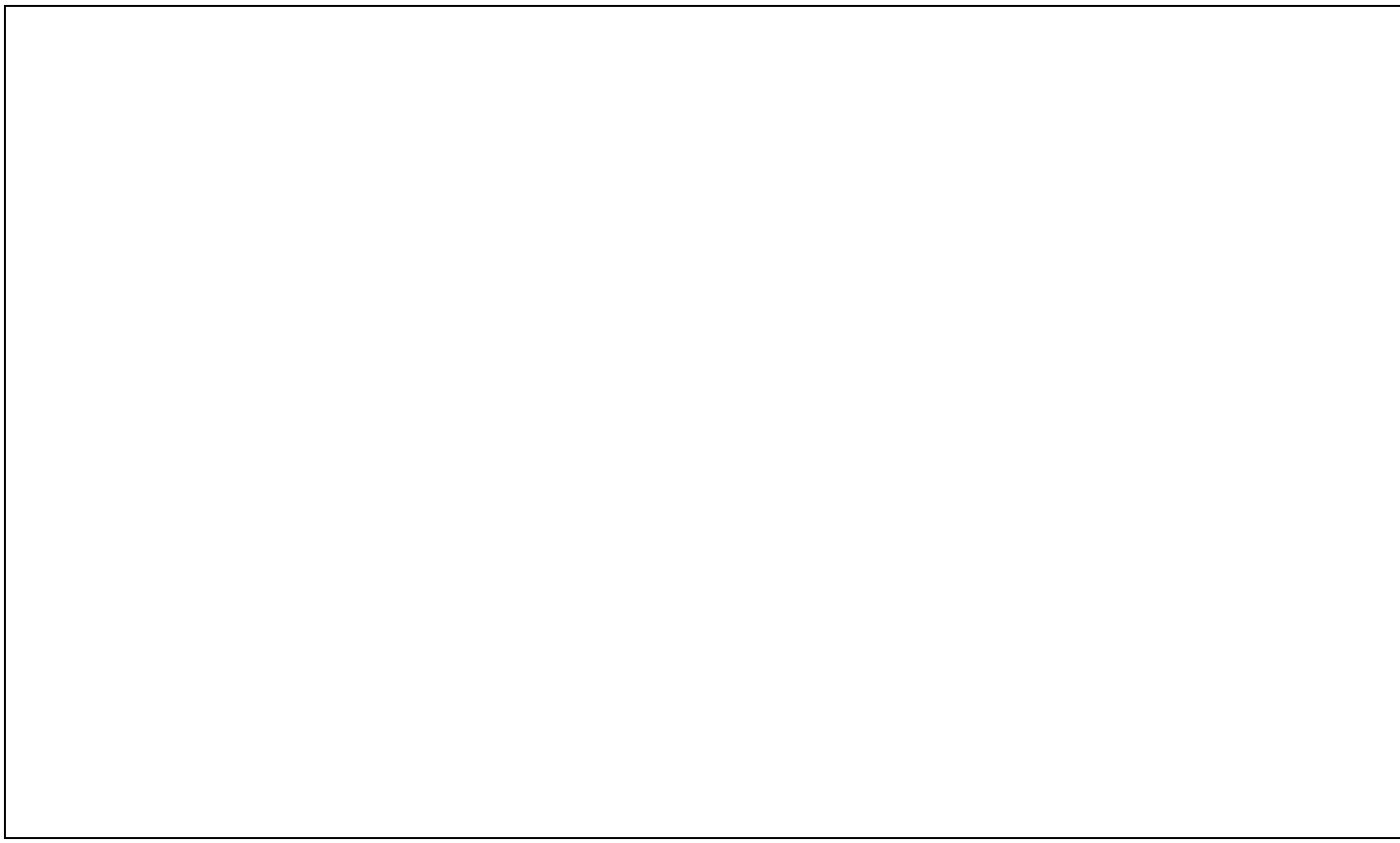

ICs for Consumer Electronics

Multistandard Modulator / PLL

TDA 6060XS

Preliminary Data Sheet 1998-10-27

Edition 1998-10-27

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TDA 6060XS		
Revision History:	**Current Version: 1998-10-27**	Editorial Update
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Recommended Operating Conditions

Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at T_A=25°C and the nominal supply voltage.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit.

Edition 1998-10-27

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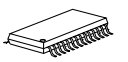
Multistandard Modulator / PLL — TDA 6060XS

Preliminary Data — **BIPOLAR**

1 Overview

1.1 Features



P-TSSOP-28-1

- Frequency and amplitude-stable balanced oscillator for the VHF, Hyper band and the UHF frequency range
- Clamped video input with peak white level detection for I^2C-Bus controlled gain setting of the video amplifier
- Programmable sound carriers 4.5 MHz, 5.5 MHz, 6 MHz, 6.5 MHz
- Second sound carrier input
- Balanced RF output
- Low-noise reference voltage
- 1-chip system for µC control (I^2C Bus)
- Fast I^2C-Bus mode possible
- 4 programmable chip addresses
- Smallest possible lock-in time; no asynchronous divider stage
- Short pull-in time for quick channel switch-over and optimized loop stability
- One high-current switch output
- 5-level A/D converter
- Lock-in flag
- Power-down flag
- Few external components

Type	Ordering Code	Package
TDA 6060XS	Q67007-A5224	P-TSSOP-28-1

1.2 Functional Description

The TDA 6060XS device combines a digitally programmable phase locked loop (PLL), with a multistandard video modulator and a programmable sound FM and AM modulator.

The PLL block with four hard-switched chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the modulator oscillator from 30 MHz to 950 MHz in increments of 250 kHz. The tuning process is controlled by a microprocessor via an I^2C Bus. The device has one output port, which can also be used as an A/D converter input. A flag is set when the loop is locked. The lock flag can be read by the processor via the I^2C Bus.

The modulator block includes a clamped video input amplifier followed by a double balanced mixer as a RF modulator, a frequency and amplitude-stable balanced oscillator for the VHF, Hyper band and the UHF range (with different tank circuits), a digitally programmable sound FM / AM modulator, a second audio carrier input and a low-noise reference voltage source.

1.3 Application

The IC is suitable for all modulator boxes.

1.4 Pin Configuration

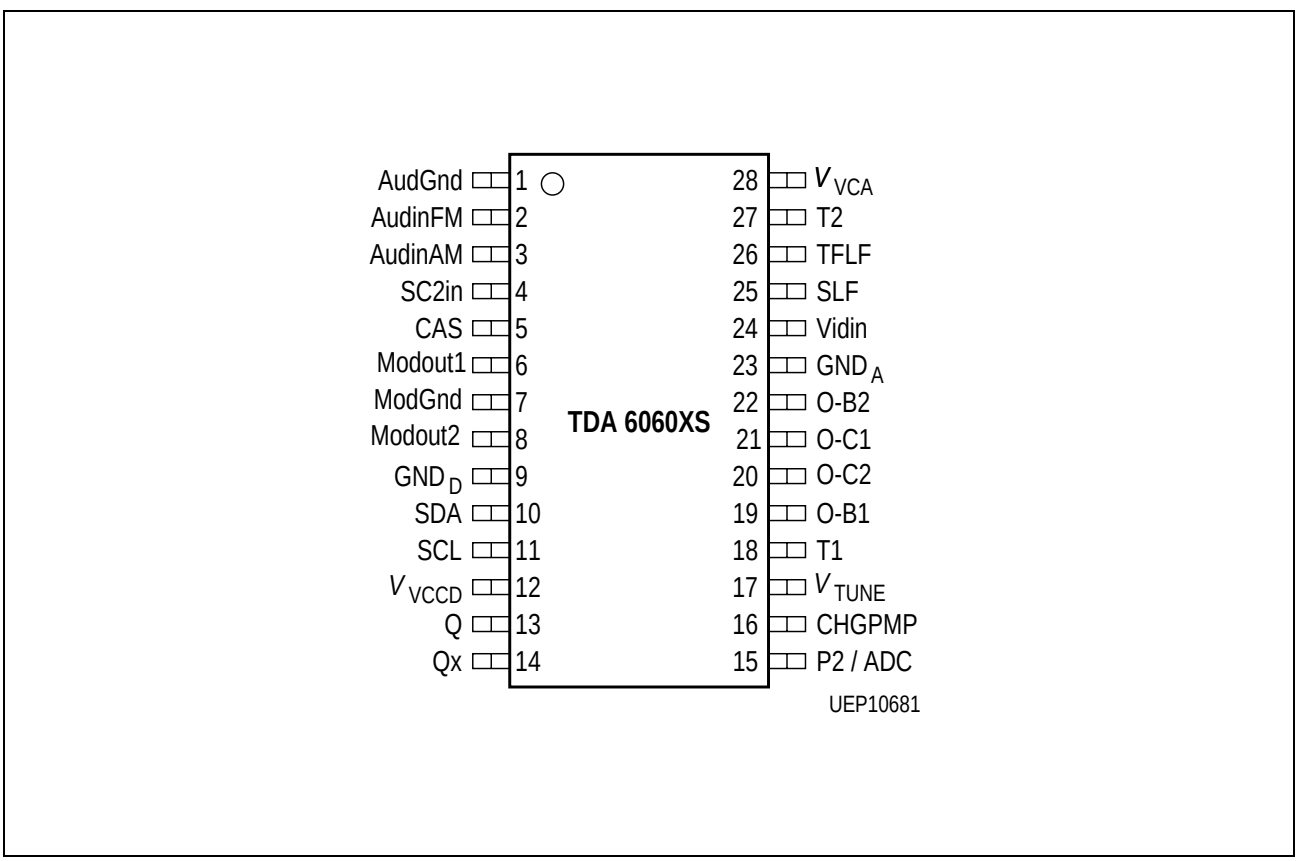


Figure 1

1.5 Pin Definitions and Functions

Pin No.	Symbol	Function
PLL Section		
5	CAS	Chip address select
9	GND_D	Ground for digital block (PLL)
10	SDA	Data input/output for the I^2C Bus
11	SCL	Clock input for the I^2C Bus
12	V_{VCCD}	Positive supply voltage for digital block (PLL)
13	Q	4 MHz low-impedance crystal oscillator input
14	Qx	4 MHz low-impedance crystal oscillator input; external oscillator input
15	P2 / ADC	Port output / ADC input
16	CHGPMP	Charge pump output / loop filter
17	V_{TUNE}	Open collector output for pull up resistor / loop filter
Multistandard Modulator Section		
1	AudGnd	Audio ground
2	AudinFM	Audio input for FM sound IF application
3	AudinAM	Audio input for AM sound IF application
4	SC2in	Second sound carrier input
6	Modout1	Modulator output, balanced to pin 8
7	ModGnd	Modulator output ground
8	Modout2	Modulator output, balanced to pin 6
18	T1	Test interface input 1
19	O-B1	Oscillator amplifier, high-impedance base input, symmetrical to O-B2
20	O-C2	Oscillator amplifier, high-impedance collector output, symmetrical to O-C1
21	O-C1	Oscillator amplifier, high-impedance collector output, symmetrical to O-C2
22	O-B2	Oscillator amplifier, high-impedance base input, symmetrical to O-B1
23	GND_A	Ground for analog block
24	Vidin	Clamped video input
25	SLF	Sound carrier PLL loop filter
26	TFLF	Tracking filter low pass filter
27	T2	Test interface input 2
28	V_{VCCA}	Positive supply voltage for analog block

1.6 Block Diagram

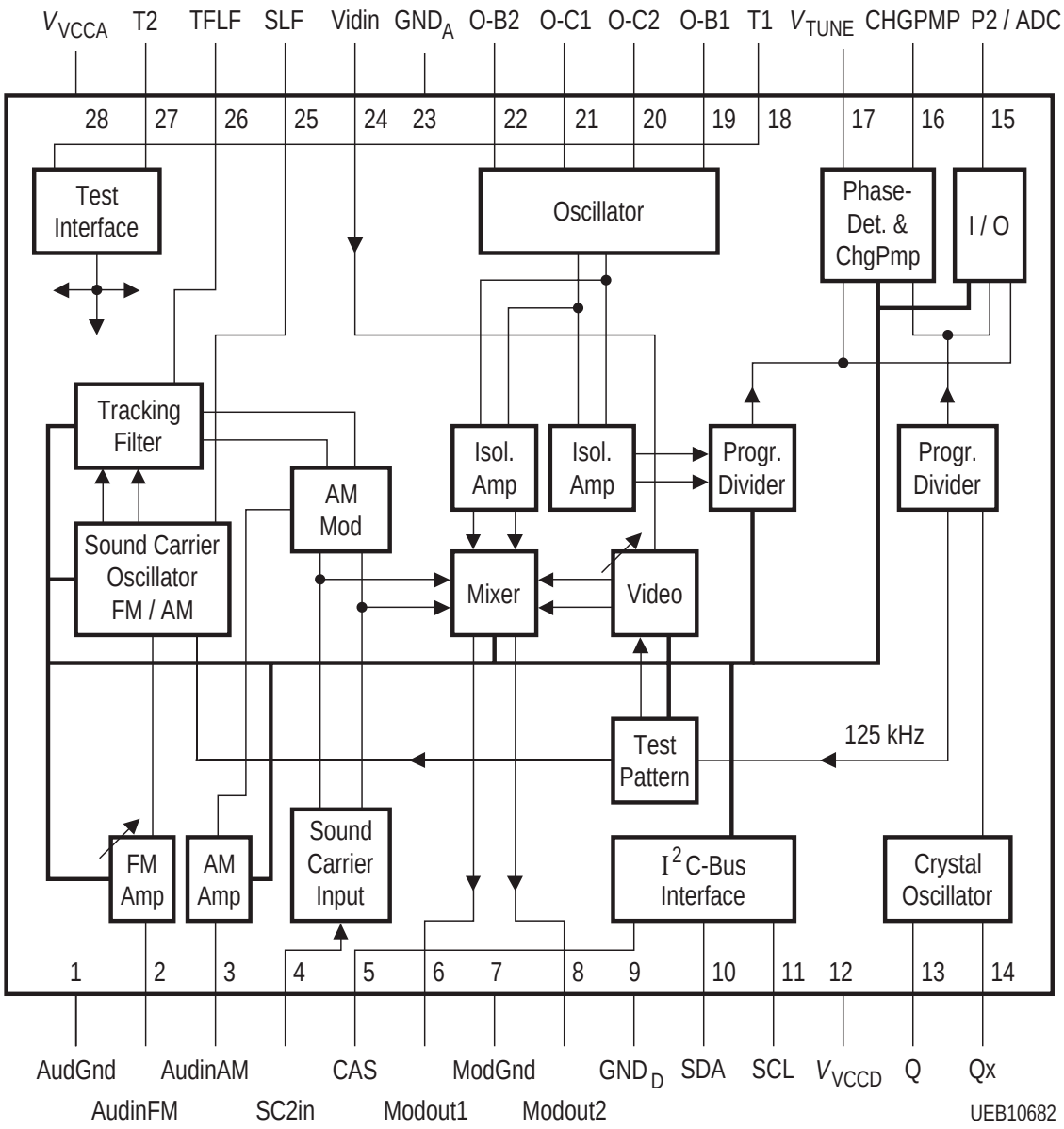


Figure 2

2 Circuit Description

2.1 Modulator Block

The modulator section includes a gain adjustable video amplifier, a double balanced mixer working as a AM video modulator for positive or negative modulation, a balanced oscillator for VHF, Hyper band and UHF, a sound modulator suitable for FM and AM modulation, a programmable sound carrier oscillator and a reference voltage source.

The audio signal is coupled to the gain settable audio pre-amplifier of the FM AF input (AudinFM) and to the AM input amplifier (AudinAM). The pre-emphasis is done with an external circuitry in front of the FM audio input. The FM audio amplifier allows a gain setting in four steps with the AU0 / 1 bits in the negative video modulation mode (PN = 0). The amplified audio signal is fed to the FM modulator. The modulated sound carrier is filtered by a tracked bandpass filter and added to the video signal. In the positive video modulation mode the audio signal is directly fed to the AM sound modulator. The sound carriers are generated by a programmable on chip oscillator. The four possible frequencies are 4.5, 5.5, 6.0 and 6.5 MHz (2-Bit). To increase the speed of the sound PLL the loop filter current can be switched to 5I with the audio mode bits (see ”Sound Carrier Frequencies” on page 14). A second FM or NICAM sound carrier may be added via the input SC2in to the internally generated carrier. The SC2in input is referenced to AudGnd and can be switched off by connecting SC2in to the supply voltage.

The positive video signal is capacitively coupled to the video input pin (Vidin). An internal clamping circuit is referenced to the sync tip level. If the video signal exceeds the maximum level the peak white level is clipped. The clipping circuit acts also as a detector and sets a flag (FLV) for the I^2C Bus. The video input amplifier allows a gain setting in four steps. The polarity of the video signal can be switched for positive or negative modulation. The setting to positive modulation is combined with the AM modulation of the sound carrier. For the residual carrier adjustment a sawtooth test picture is used when the video modulator is in overmodulation mode.This mode is active by connecting test pin T1 to ground.

The adjustments of the modulation depth and the picture to sound carrier ratio can be done in four steps.

The RF oscillator works as gain controlled LC tuned astable multivibrator. The output of the oscillator is decoupled by two isolation amplifiers, one for the modulator mixer and one for the synthesizer PLL. The VCO can be switched off by setting both audio mode bits to 1 in positive modulation mode (see ”Sound Carrier Frequencies” on page 14) The added sound carrier and video signals are mixed with the RF oscillator signal in the double balanced mixer and then fed to both RF outputs (Modout1 / Modout2).

2.2 PLL and I^2C Bus

The oscillator signal for the RF modulator is internally DC-coupled as a differential signal at the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32764 by 4 and is then compared in a digital frequency / phase detector to a reference frequency f_{ref} = 62.5 kHz. This frequency is derived from a balanced, low-impedance 4 MHz crystal oscillator (pin Q, Qx) or from a external signal source divided by Q = 64.

The phase detector has two outputs UP and DOWN that drive two current sources I+ and I- of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the I+ current source pulses for the duration of the phase difference. In the reverse case the I- current source pulses. If the two signals are in phase, the charge pump output (CHGPMP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pullup resistor at TUNE and external RC circuitry). It should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self-discharge in the peripheral circuitry. TUNE may be switched off by the control bit OS to allow external adjustments.

The software-switched bidirectional port P2 is a general-purpose open-collector output and can also be used as an A/D converter input.

In the internal or external 4 MHz reference oscillator mode a test pattern is generated in the reference divider. With the bit TP in the second control byte this test pattern is switched to the modulator input.

Data are exchanged between the processor and the PLL via the I^2C Bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I^2C Bus.

The data from the processor pass through an I^2C-Bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table 1 ”bit allocation” should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The eighth bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the first bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of two bits from the TTL input ports, three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate connection of pin CAS (see ”Address Selection” on page 14).

When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when V_{VCCD} goes below 3.2 V. It will be reset at the end of a READ operation.

The lock detector resets the lock flag FL when the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, when FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P \, (K_{VCO} / f_Q) \, (C_1 + C_2) / (C_1 C_2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_Q the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see ”Application Board” on page 30). As the charge pump pulses at 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains the lock state.

2.2.1 Bit Allocation Read/Write

Byte	MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB	Ack
Write Data									
Address byte	1	1	0	0	0	MA1	MA0	0	Ack
Progr. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	Ack
Progr. divider byte 2	n7	n6	n5	n4	n3	n2	SC1	SC0	Ack
Control byte 1	1	PN	AU1	AU0	x	x	OS	FS	Ack
Control byte 2	TP	VG1	VG0	MD1	MD0	P2	PS1	PS0	Ack
Read Data									
Address byte	1	1	0	0	0	MA1	MA0	1	Ack
Status byte	POR	FL	x	FLV	x	A2	A1	A0	Ack

2.2.2 Description of Symbols

Symbol	Description
MSB	Most Significant Bit (shifted first)
n14 to n2	Programmable divider bits: $N = 2^{14} * n14 + 2^{13} * n13 + ... + 2^3 * n3 + 2^2 * n2 + 0 + 0$
MA0, MA1	Address selection bits (see ”Address Selection” on page 14)
PN	Bit = 1: Negative modulation for video and FM for sound carriers (AudinFM active) Bit = 0: Positive modulation for video and AM modulation for sound carrier (AudinAM active)
AU0, AU1	Audio mode bits and Sound / RF VCO off mode (see ”Audio Modes” on page 14)
SC0, SC1	Sound carrier bits (see ”Sound Carrier Frequencies” on page 14)
OS	Bit = 1: Disables V_{TUNE} (for external VCO adjustment) Bit = 0: Normal PLL operation
FS	When quartz oscillator is in slave mode: Bit = 1: External frequency is 62.5 kHz, for test and special applications (test pattern and PLL lock in flag FL not available, sound carrier frequencies incorrect) Bit = 0: External frequency is 4 MHz
TP	Bit = 1: Test pattern generator on Bit = 0: Normal operation
VG0, VG1	Video gain setting (see ”Video Gain Setting” on page 14)
MD0, MD1	Modulation depth (see ”Modulation Depth Adjustment” on page 15)
Port P2	Bit = 1: Open-collector output is active Bit = 0: Open-collector output is inactive, ADC available
PS0, PS1	Picture / sound ratio setting (see ”Picture Carrier / Sound Carrier Adjustment” on page 15)
POR	Power on reset, flag is set at power-on and reset at the end of READ operation
FL	PLL lock indicator, flag is set when loop is locked
FLV	Clipping detector, flag is set when clipping duration is longer than 1 µsec
A0, A1, A2	A/D converter levels when P2 works as input (see ”A/D Converter Levels” on page 15)
x	don‘t care

2.2.3 Address Selection

Voltage at CAS	MA1	MA0
(0...0.1) * V_{VCCD}	0	0
Open circuit	0	1
(0.4...0.6) * V_{VCCD}	1	0
(0.9...1) * V_{VCCD}	1	1

2.2.4 Audio Modes

Audio Mode	PN	AU1	AU0
Normal audio operation AM	0	0	0
5 x I switch for sound PLL	0	1	0
Sound carrier off	0	0	1
RF VCO off (PN bit = 0) positive modulation	0	1	1
Normal audio operation	1	0	0
Audio level -1 dB (PN bit = 1) negative modulation	1	1	0
Audio level -2 dB (PN bit = 1) negative modulation	1	0	1
Audio level -3 dB (PN bit = 1) negative modulation	1	1	1

2.2.5 Sound Carrier Frequencies

SC Frequency	SC1	SC0
4.5 MHz	0	0
5.5 MHz	0	1
6.0 MHz	1	0
6.5 MHz	1	1

2.2.6 Video Gain Setting

Video Gain	VG1	VG0
Normal operation	0	0
- 1 dB	0	1
- 2 dB	1	0
- 3 dB	1	1

2.2.7 Modulation Depth Adjustment

Modulation Depth	MD1	MD0
Normal operation	0	0
+ 5 %	0	1
- 5 %	1	0
- 10 %	1	1

2.2.8 Picture Carrier / Sound Carrier Adjustment

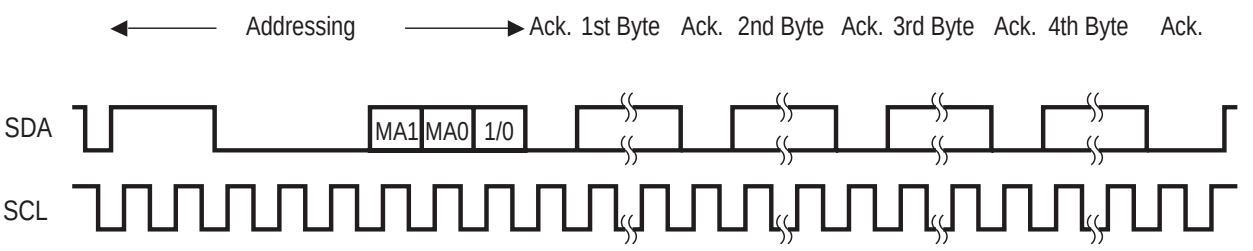
Picture Carrier to Sound Carrier Ratio	PS1	PS0
Normal operation	0	0
- 1 dB	0	1
+ 1 dB	1	0
+ 2dB	1	1

2.2.9 A/D Converter Levels

Voltage at P2 / ADC	A2	A1	A0
(0...0.15) * V_{VCCD}	0	0	0
(0.15...0.3) * V_{VCCD}	0	0	1
(0.3...0.45) * V_{VCCD}	0	1	0
(0.45...0.6) * V_{VCCD}	0	1	1
(0.6...1) * V_{VCCD}	1	0	0

2.2.10 Test Pin Configuration

Picture Carrier to Sound Carrier Ratio	T2	T1
f_{cy} at P2 (P2 working as output; bit P2 = 1)	0	0
f_{ref} at P2 (P2 working as output; bit P2 = 1)	0	1
RF modulator in overmodulation mode	1	0
Normal operation	1	1



Telegram examples:

Start-Addr-DR1-DR2-CW1-CW2-Stop
Start-Addr-CW1-CW2-DR1-DR2-Stop
Start-Addr-DR1-DR2-Stop
Start-Addr-CW1-CW2-Stop
Start-Addr-ST-Stop

Start = Start Condition
Addr = Address
DR1 = Divider Ratio 1st Byte
DR2 = Divider Ratio 2nd Byte
CW1 = Control Word 1st Byte
CW2 = Control Word 2nd Byte
Stop = Stop Condition
ST = Read Status Byte

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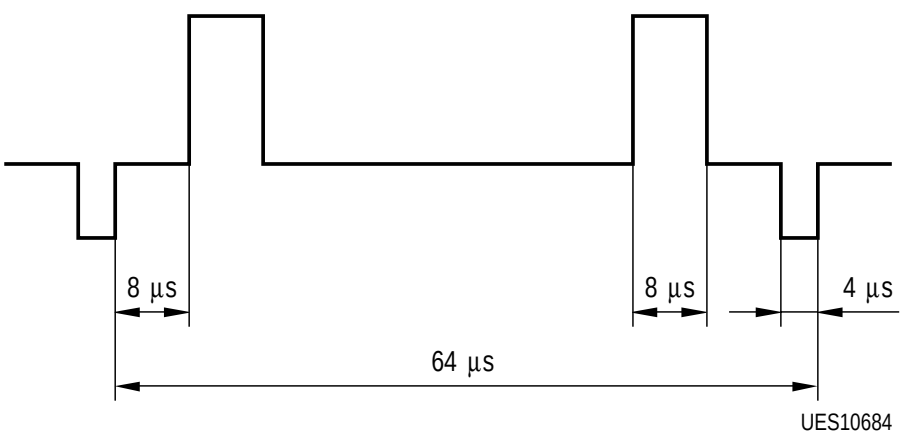


Figure 3 Test Picture

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
PLL					
Supply voltage	V_{VCCD}	- 0.3	6	V	
Output CHGPMP	V_{CHGPMP}	- 0.3	3.5	V	
Crystal oscillator pins Q, Qx	V_{Q}	- 0.3	V_{VCCD}	V	
Bus input/output SDA	V_{SDA}	- 0.3	6	V	
Bus input SCL	V_{SCL}	- 0.3	6	V	
Chip address switch CAS	V_{CAUS}	- 0.3	V_{VCCD}	V	
Output active filter V_{TUNE}	V_{TUNE}	- 0.3	35	V	
Bus output SDA	I_{SDAL}	0	5	mA	Open collector
Port output P2	I_{PL}	0	20	mA	Open collector
Port output P2	V_{P}	- 0.3	6	V	
Junction temperature	T_{J}		125	°C	
Storage temperature	T_{S}	- 40	125	°C	
Thermal resistance (junction to ambient)	R_{thSA}		130	K/W	
Modulator					
Supply voltage	V_{VCCA}	- 0.3	6	V	
Video input	I_{Vidin}		tbf	mA	
Modulator outputs	$V_{Modout1/2}$	tbf	6	V	Open collector
FM audio input	$V_{AudinFM}$	- 0.3	6	V	
AM audio input	$V_{AudinAM}$	- 0.3	6	V	
Second sound carrier input	V_{SC2in}	- 0.3	6	V	

Ambient Temperature: T_{amb} = 0 to 80 °C

Note: The maximal ratings may not be exceeded under any circumstances, not even momentary and individually, as permanent damage to the IC will result.

3.2 Operational Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{VCCD}	4.5	5.5	V	
Supply voltage	V_{VCCA}	4.5	5.5	V	
Modulator output voltage	V_{Modout}		tbf	mV	
Programmable divider factor	N	256	32764		by 4
Video input voltage range	V_{Vidin}	0.3	1	V_{pp}	
Audio input voltage (FM or AM)	V_{Audin}		1	V_{rms}	
Oscillator frequency range	f_O	30	950	MHz	
Ambient temperature	T_{amb}	0	80	°C	

Note: Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed.

3.3 AC/DC Characteristics

Parameter T_{amb} = 25 °C; Ch 21 ... Ch 69 V_{VCC} = 5 V	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Digital Part						
Supply current	I_{VCCD}	16	21	29	mA	V_{VCCD} = 5 V
PLL						
Crystal Oscillator Connections Q, Qx						
Crystal frequency	f_Q	3.2	4.0	4.8	MHz	Series resonance
Crystal resistance [1)]	R_Q	10		100	Ω	Series resonance
Oscillation frequency	f_Q	3.99975	4.000	4.00025	MHz	f_Q = 4 MHz
Drive current [1)]	I_Q	tbf	tbf	tbf	μA_{rms}	f_Q = 4 MHz
Input impedance [1)]	Z_Q	-600	-750	- 900	Ω	f_Q = 4 MHz
Margin from 1st (funda-mental) to 2nd and 3rd harmonics [1)]	a_H	20			dB	f_Q = 4 MHz
Charge Pump Output CHGPMP (V_{VCC} = 5 V)						
Output current	I_{CPL}	± 22	± 50	± 75	µA	V_{CP} = 2 V
Tristate current	I_{CPZ}		1		nA	PN = 1, T0 = 1, V_{CP} = 2 V
Output voltage	V_{CP}	1.0		2.5	V	Locked
Drive Output V_{TUNE} (open collector)						
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V
LOW output voltage	V_{TL}			0.5	V	I_{TL} = 1.5 mA
Port Output P2 (open collector)						
HIGH output current	I_{POH}			10	µA	V_{POH} = 5 V
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 15 mA
ADC Port Input P2						
HIGH input current	I_{ADCH}			10	µA	
LOW input current	I_{ADCL}	- 10			µA	
Address Selection Input CAS						
HIGH input current	I_{CASH}			50	µA	V_{CASH} = 5 V
LOW input current	I_{CASL}	- 50			µA	V_{CASL} = 0 V

3.3 AC/DC Characteristics (cont'd)

Parameter T_{amb} = 25 °C; Ch 21 ... Ch 69 V_{VCC} = 5 V	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
I^2C-Bus						
Bus Inputs SCL, SDA						
HIGH input voltage	V_{IH}	3	–	5.5	V	
LOW input voltage	V_{IL}	–	–	1.5	V	
HIGH input current	I_{IH}	–	–	10	µA	$V_{IH} = V_S$
LOW input current	I_{IL}	- 20	–	–	µA	V_{IL} = 0 V
Bus Output SDA (open collector)						
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA
Edge Speed SCL, SDA						
Rise time	t_r			300	ns	
Fall time	t_f			300	ns	
Clock Timing SCL						
Frequency	f_{SCL}	0		400	kHz	
HIGH pulse width	t_H	0.6			µs	
LOW pulse width	t_L	1.3			µs	
Start Condition						
Set-up time	t_{susta}	0.6			µs	
Hold time	t_{hsta}	0.6			µs	
Stop Condition						
Set-up time	t_{susto}	0.6			µs	
Bus free	t_{buf}	1.3			µs	
Data Transfer						
Set-up time	t_{sudat}	0.1			µs	
Hold time	t_{hdat}				µs	
Input hysteresis SCL,SDA [1)]	V_{hys}		200		mV	
Noise immunity SCL,SDA [1) 2)]	V_N		5		V_{pp}	
Capacitive load for each bus line	C_L			400	pF	

3.3 AC/DC Characteristics (cont'd)

Parameter T_{amb} = 25 °C; Ch 21 ... Ch 69 V_{VCC} = 5 V	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog Part						
Supply current	I_{VCCA}	33	43	57	mA	Incl. mixer outputs
Video Modulator						
Video input voltage	V_{Vidin}		0.5		V_{pp}	
Video gain steps	Δ Gain		- 3		dB	3 steps, 1 dB each
Step width of gain setting	δ Gain	0.8	1	1.2	dB	
Intermodulation ratio	a_{IMA}	60			dB	f_{SC} - f_{CC}
Harmonic wave ratio	a_H	60			dB	f_{PC} + 2 f_{CC}; f_{PC} + 3 f_{CC}; f_{PC} + 4f_{CC}
Modulation depth	$m_{D/N}$ $m_{D/P}$	80 80	90 90	98 98	% %	
Modulation depth adj. range	Δm_D	-10		+ 5	%	
Video signal to noise ratio	V_{S+NN}	48	51		dB	CCIR 17-line bar, line 22 HP = 200 kHz LP = 5 MHz unweighted
Audio in video (test procedure 1)	a_{AV}	54	60		dB	FM modulation; Δf = 27 kHz; V_{Vidin} = 0 V_{pp}
Audio in video (test procedure 1)	a_{AV}	54	60		dB	AM modulation; m = 65 %; V_{Vidin} = 0 V_{pp}
Differential gain	DG		3	5	%	V_{Vidin} = 0 V_{pp}
Differential phase	DP		1	5	deg	V_{Vidin} = 0 V_{pp}
Video frequency response	a_V			± 1	dB	f = 50 Hz ... 5 MHz
FM Modulator						
FM audio input voltage	V_{Audin*}		0.5		V_{rms}	*A pre-emphasis network input
FM carrier frequency range	FM_C	4.5		6.5	MHz	

3.3 AC/DC Characteristics (cont'd)

Parameter T_{amb} = 25 °C; Ch 21 ... Ch 69 V_{VCC} = 5 V	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
FM deviation SC = 6.5 MHz SC = 6.0 MHz SC = 5.5 MHz SC = 5.0 MHz	 Δ FM Δ FM Δ FM Δ FM	 28 24 24 17.5	 35 30 30 22	 42 36 36 26.5	 kHz kHz kHz kHz	$V_{Audin*\ rms}$ = 0.5 V; f_{AF} = 1 kHz
FM modulation distortions	THD_{FM}		0.3	1.5	%	$V_{Audin*\ rms}$ = 0.5 V
FM signal to noise ratio	S+N/N	50	56		dB	f_{AF} = 1 kHz; Δf = 50 kHz; video: colorbar Ch 21, CCIR 468-3 quasi peak
Second Sound Carrier Input						
Input DC voltage	V_{SC2in}	- 0.3	0	+ 0.3	V	Normal operation
Input DC voltage	V_{SC2in}	2		V_{VCCA}	V	SC2in OFF
Input AC voltage	V_{SC2in}		tbf		V_{rms}	
AM Modulator						
AM audio input voltage*	V_{Audin*}		0.5		V_{rms}	*At voltage divider input
AM carrier frequency	AM_C		6.5		MHz	
AM modulator factor	m_{AM}	55	60	65	%	$V_{Audin*\ rms}$ = 0.5 V
AM modulation distortion	THD_{AM}			1.5	%	$V_{Audin*\ rms}$ = 0.5 V
AM signal to noise ratio	S+N/N	47	50		dB	f_{AF} = 1 kHz; m = 60 %; RMS; CCIR 468; video: colorbar
RF Modulator, Referred to Application Board						
Modulator output impedance	R_{Modout} C_{Modout}		20 0.5		kΩ pF	
RF output voltage	V_{Modout}	77	80		dBµV	RL = 75 Ω
RF output harmonics (n = 2)	a_{RF2}		- 15	- 10	dBc	f_{Modout} = 470 to 860 MHz

3.3 AC/DC Characteristics (cont'd)

Parameter T_{amb} = 25 °C; Ch 21 ... Ch 69 V_{VCC} = 5 V	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Picture Sound carrier ratio	PC / SC ratio	8	11	14	dB	L; M; DK standard
Picture Sound carrier ratio	PC / SC ratio	10	13	16	dB	BG / I standard
Sound carrier harmonics	THD_{SC}	55	65		dB	referenced to picture carrier
Rejection of PLL reference frequency	a_{fref}	60			dB	

[1] Design note: no 100% final inspection.

Note: AC/DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

4 Test Circuit 1

4.1 Measurement of Crystal Oscillator Frequency

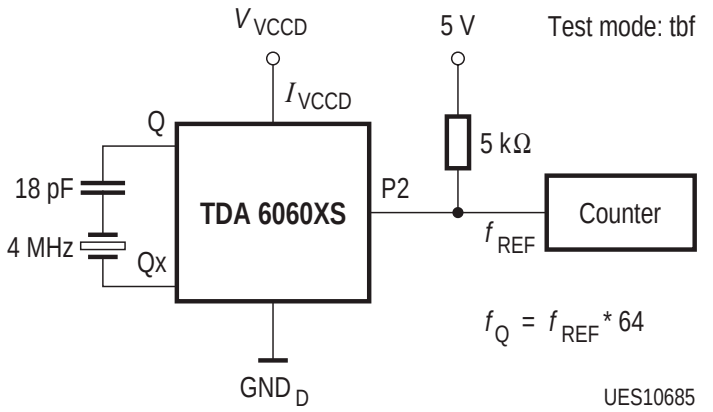


Figure 4

4.2 Test Procedure 1: Crosstalk Audio in Video

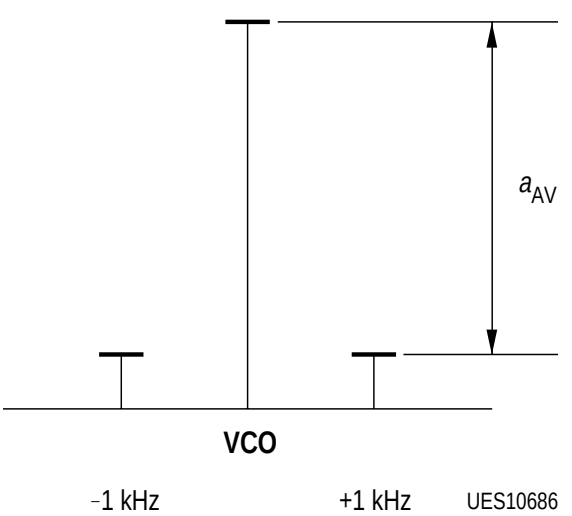


Figure 5

5 Equivalent I/O-Schematic

5.1 Equivalent I/O-Schematic of Quartz Oscillator

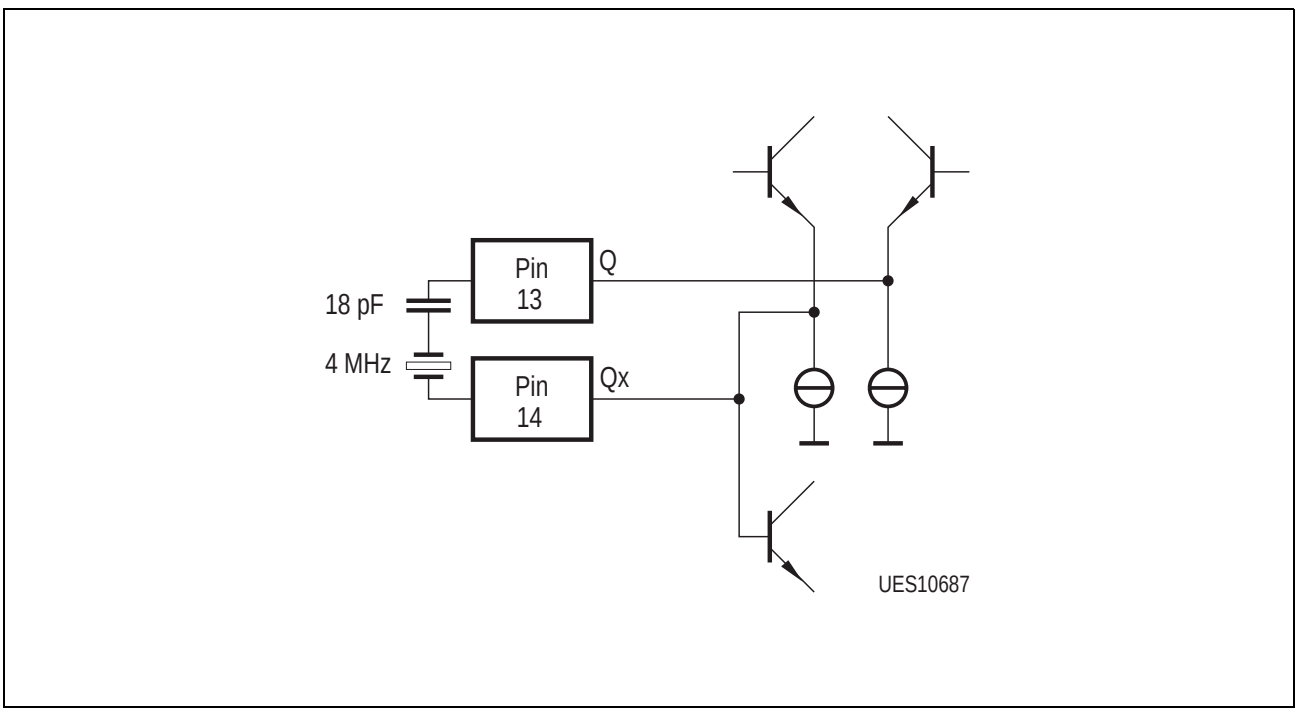


Figure 6

5.2 Equivalent I/O-Schematic of Charge Pump

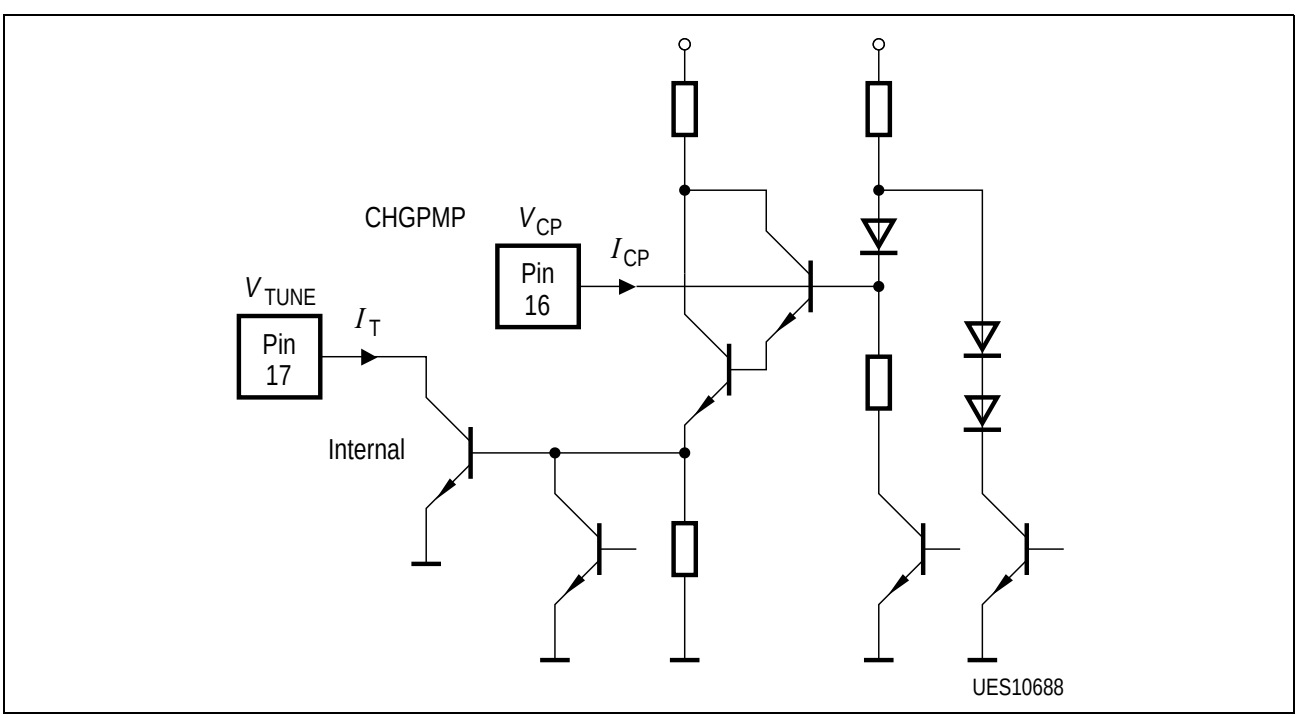


Figure 7

5.3 Equivalent I/O-Schematic of Port Pin

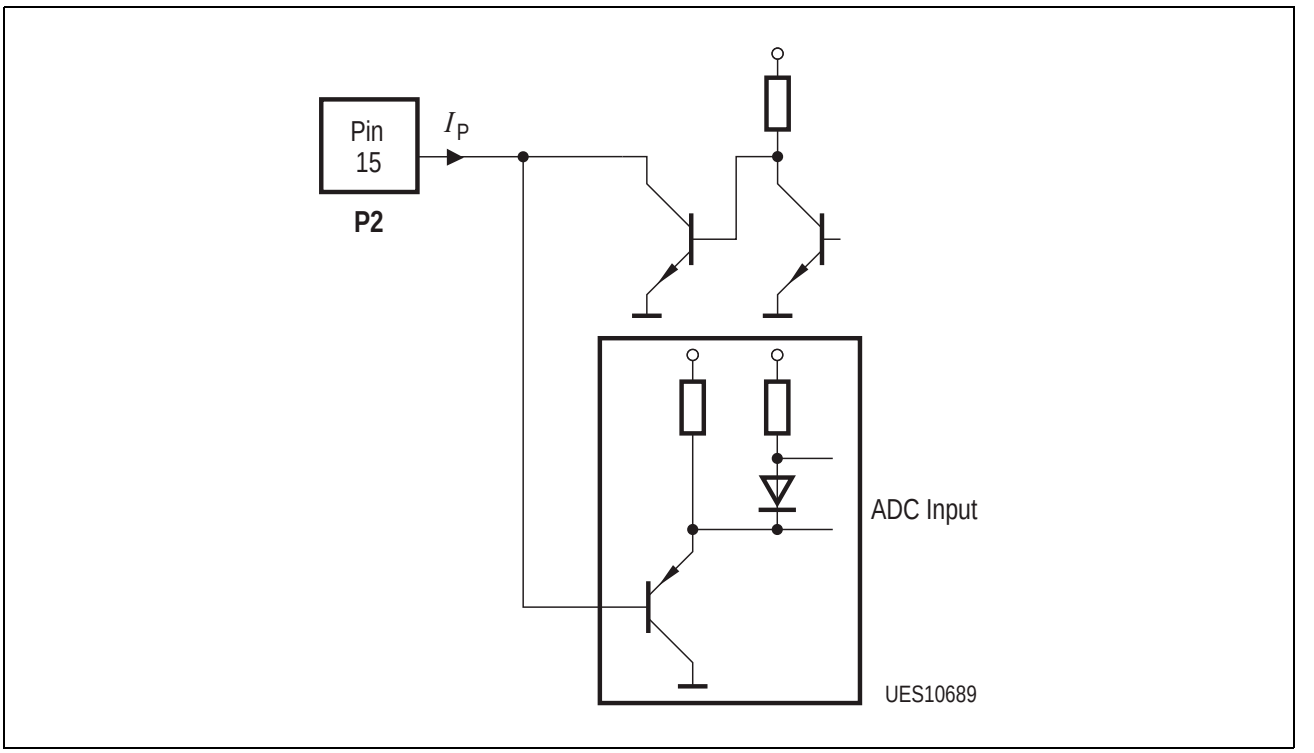


Figure 8

5.4 Equivalent I/O-Schematic of CAS Pin

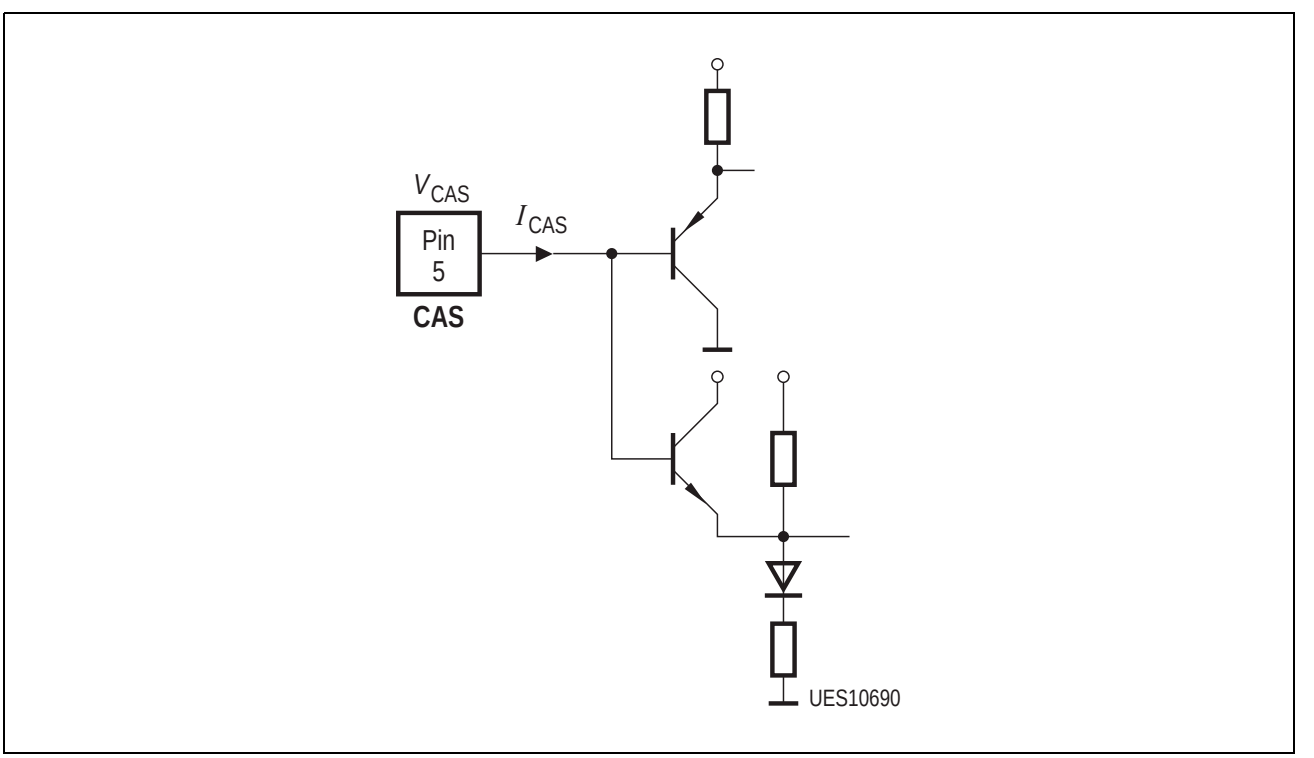


Figure 9

5.5 Equivalent I/O-Schematic of SDA / SCL Plus

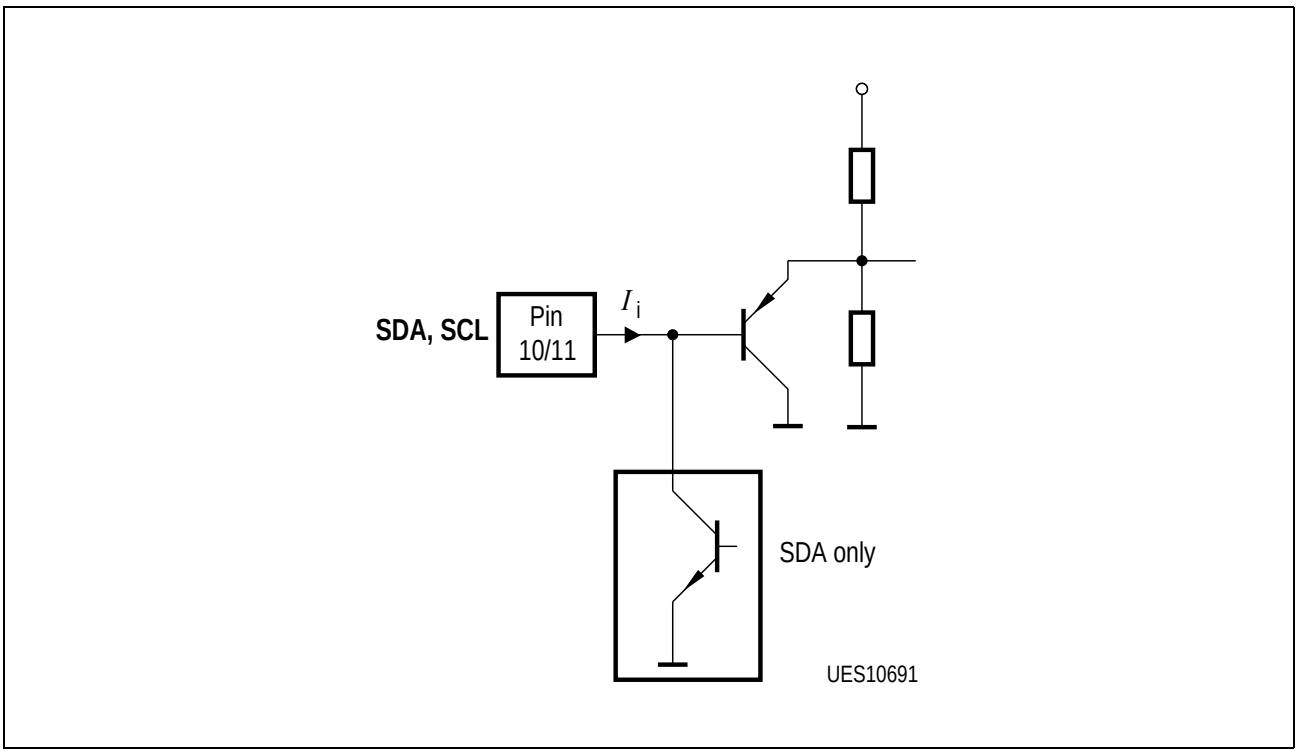


Figure 10

5.6 Equivalent I/O-Schematic of UHF- / VHF-Oscillator Pins

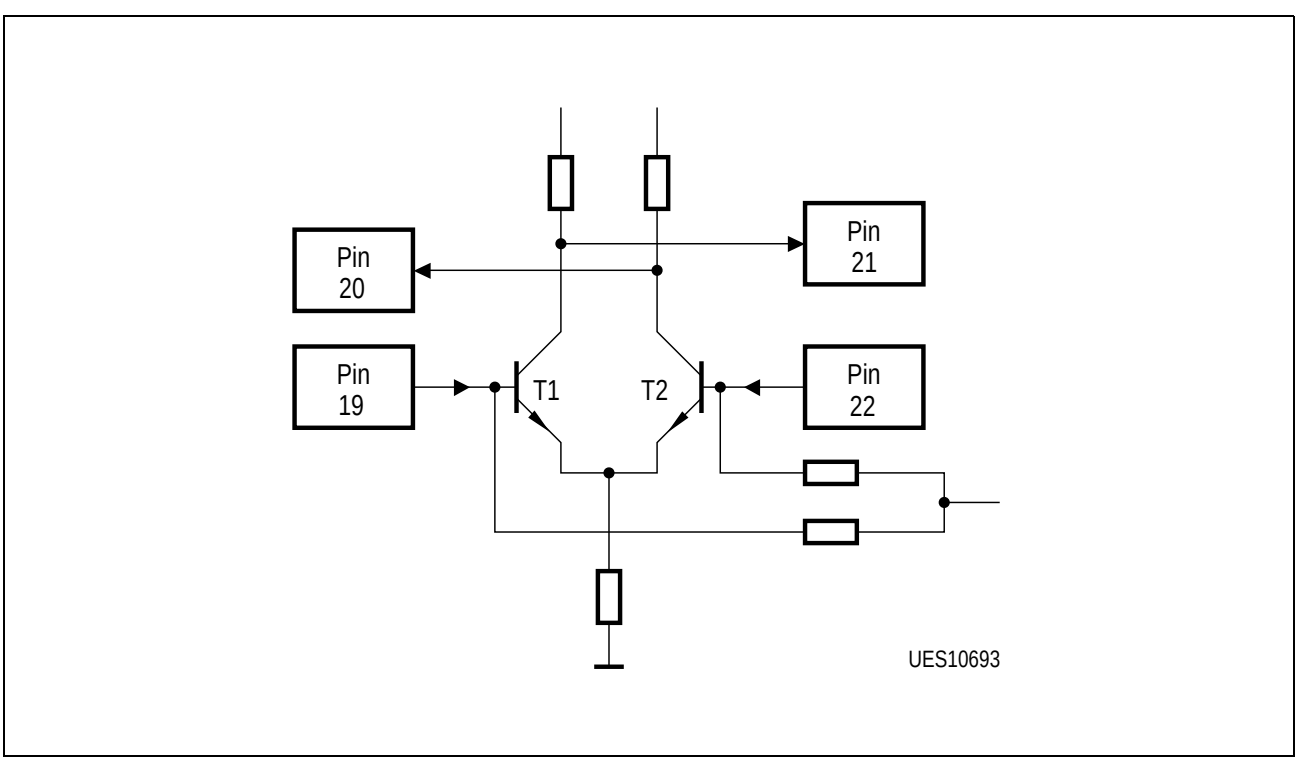
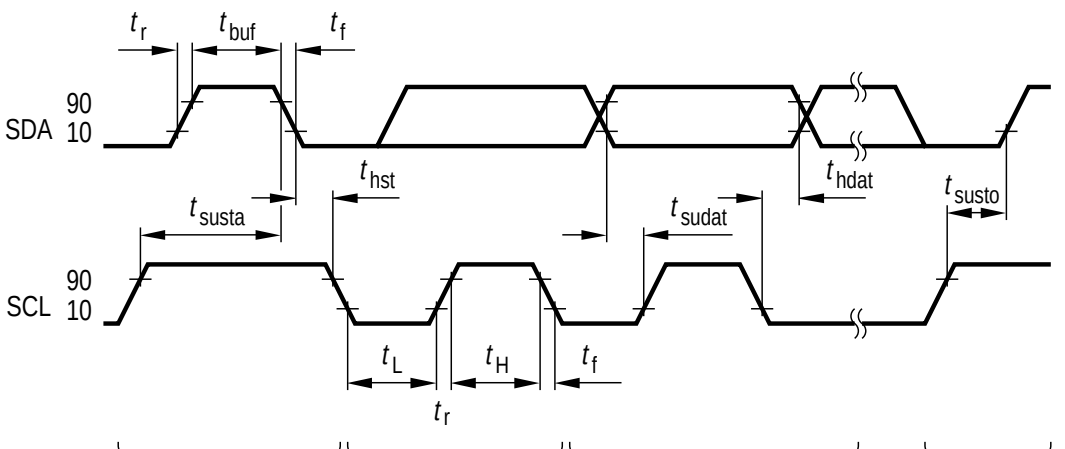


Figure 11

6 I²C-Bus Timing



t_{buf}	bus free time	t_L	LOW clock pulse width
t_r	data / clock rise time	t_H	HIGH clock pulse width
t_f	data / clock fall time	t_{sudat}	data transfer set-up time
t_{susta}	start set-up time	t_{hdat}	data transfer hold time
t_{hsta}	start hold time	t_{susto}	stop set-up time

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Figure 12

7 Test Circuit Diagram

Figure 13

8 Application Board

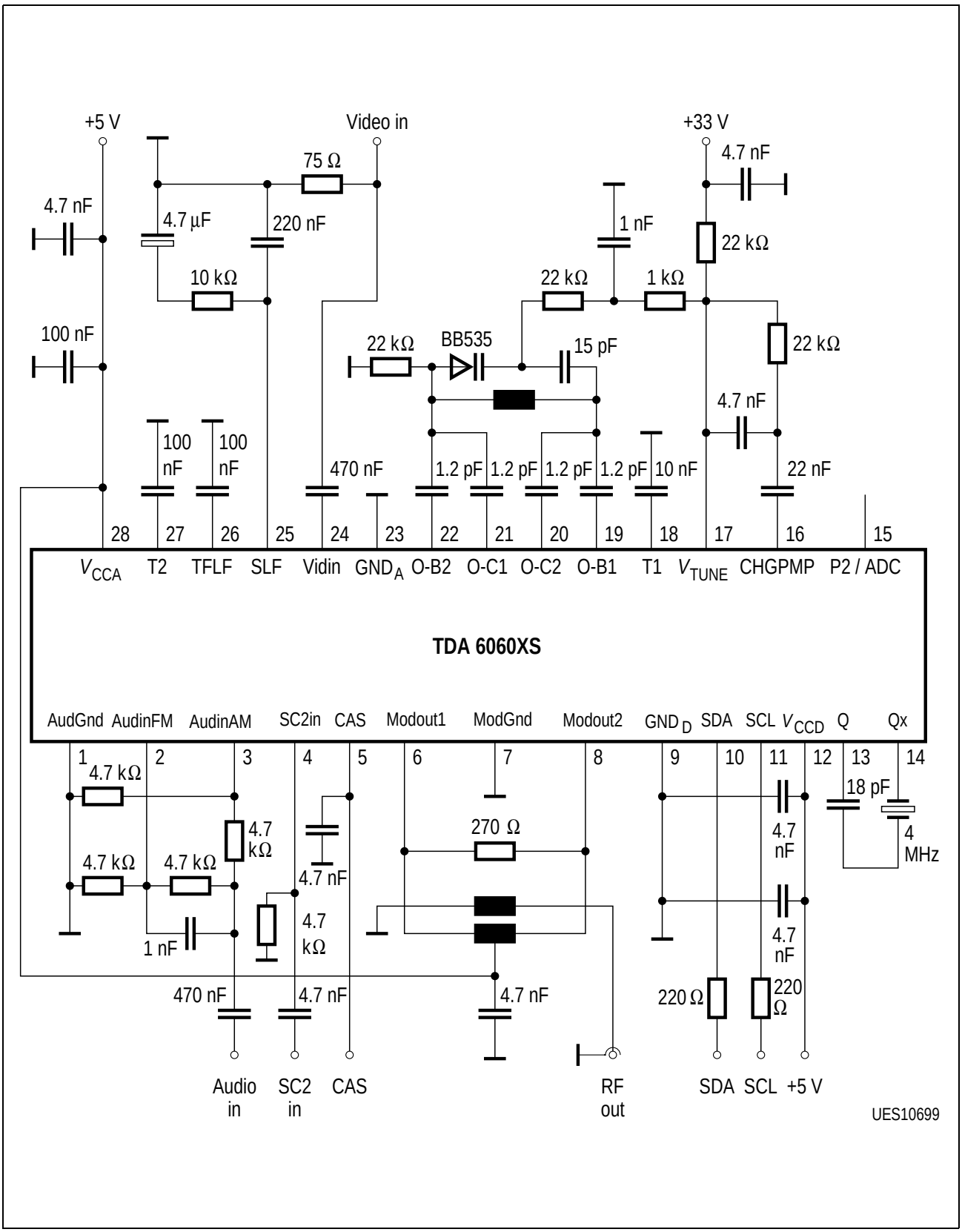
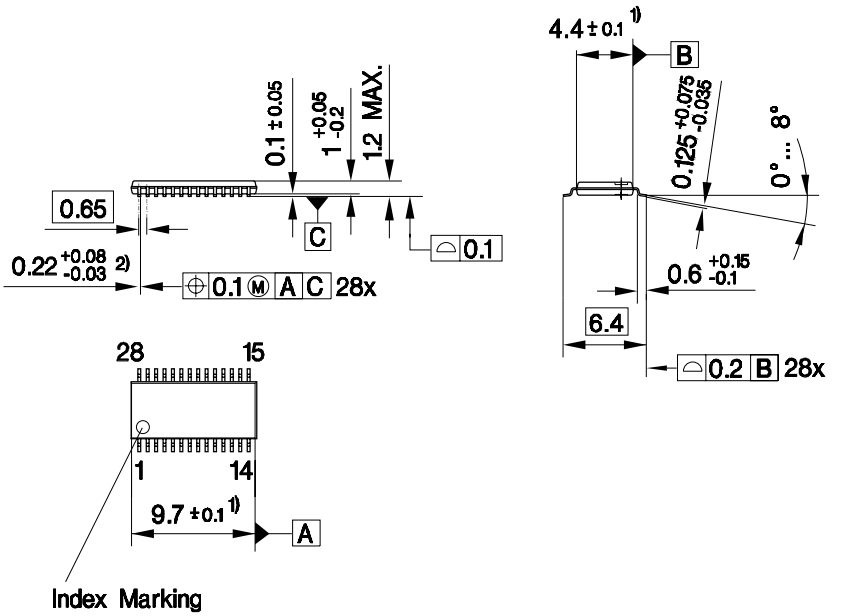


Figure 14

9 Package Outlines

P-TSSOP-28-1
(Plastic Thin Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

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Figure 15