DATA SHEET

TDA4560
Colour transient improvement circuit

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Colour transient improvement circuit TDA4560

GENERAL DESCRIPTION

The TDA4560 is a monolithic integrated circuit for colour transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 720 ns to 1035 ns in steps of 45 ns
- Output for the option of velocity modulation

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10-18}$	typ.	12	V
Supply current (pin 10)	$I_P = I_{10}$	typ.	35	mA
(R-Y) and (B-Y) attenuation	α_{cd}	typ.	0	dB
(R-Y) and (B-Y) output transient time	t_{tr}	typ.	150	ns
Adjustable Y-delay time	t_d	720 to	1035	ns
Y-attenuation	α_y	typ.	7	dB

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102); SOT102-1; 1996 November 27.

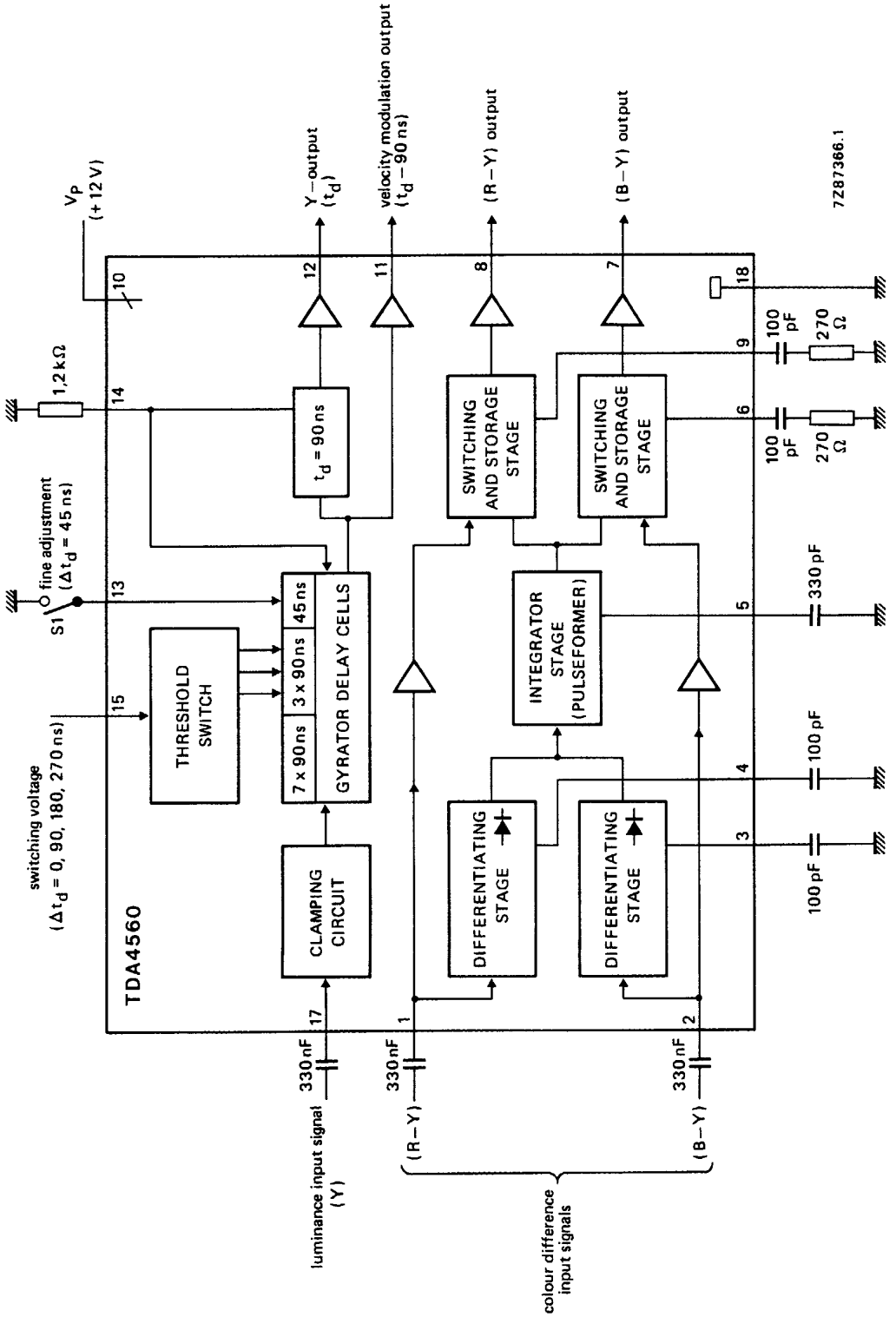


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The IC consists of two colour difference channels (B-Y) and (R-Y) and a luminance signal path (Y) as shown in Fig.1.

Colour difference channels

The (B-Y) and (R-Y) colour difference channels consist of a buffer amplifier at the input, a switching stage and an output amplifier. The switching stages, which are controlled by transient detecting stages (differentiators), switch to a value that has been stored at the beginning of the transients. The differentiating stages get their signal direct from the colour difference detecting signal (pins 1 and 2). Two parallel storage stages are incorporated in which the colour difference signals are stored during the transient time of the signal. After a time of about 600 ns they are switched immediately (transient time of 150 ns) to the outputs. The colour difference channels are not attenuated.

Y-signal path

The Y-signal input (pin 17) is capacitively coupled to an input clamping circuit. Gyrator delay cells provide a maximum delay of 1035 ns including an additional delay of 45 ns via the fine adjustment switch (S1) at pin 13. Three delay cells are switched with two interstage switches dependent on the voltage at pin 15. Thus three switchable delay times of 90 ns, 180 ns or 270 ns less than the maximum delay time are available. A tuning compensation circuit ensures accuracy of delay time despite process tolerances. The Y-signal path has a 7 dB attenuation as a normal Y-delay coil and can replace this completely. The output is fed to pin 12 via a buffer amplifier. An additional output stage provides a signal of 90 ns less delay at pin 11 for the option of velocity modulation.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC)

Supply voltage (pin 10)	$V_P = V_{10-18}$	max. 13,2	V
Voltage ranges to pin 18 (ground)			
at pins 1,2,12,15	V_{n-18}	0 to V_P	V
at pin 11	V_{11-18}	0 to (V_P–3V)	V
at pin 17	V_{17-18}	0 to 7	V
Voltage ranges			
at pin 7 to pin 6	V_{7-6}	0 to 5	V
at pin 8 to pin 9	V_{8-9}	0 to 5	V
Currents			
at pins 6,9	$\pm I_{6,9}$	max. 15	mA
at I_7, I_8, I_{11}, I_{12}		internally limited	
Total power dissipation	P_{tot}	max. 1,1	W
Storage temperature range	T_{stg}	-25 to +150	°C
Operating ambient temperature range	T_{amb}	0 to +70	°C

Note

1. Pins 3, 4, 5, 6, 9, 13 and 14 d.c. potential not published.

CHARACTERISTICS

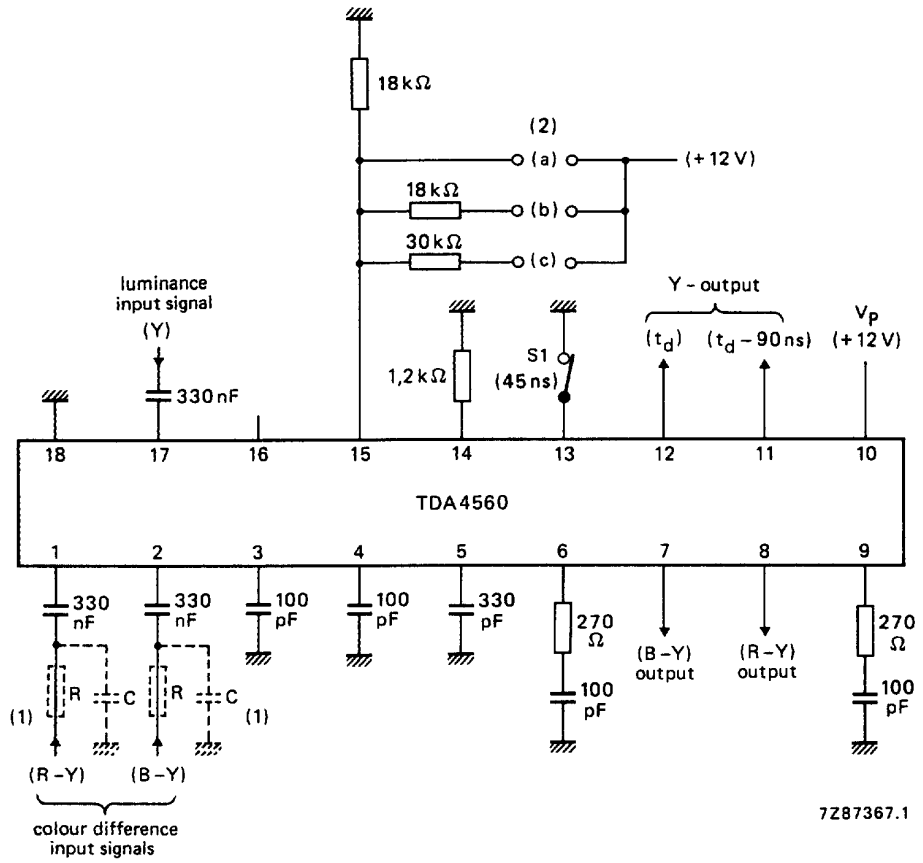
$V_P = V_{10-18}$ = 12 V; T_{amb} = 25 °C; measured in application circuit Fig.2; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply (pin 10)					
Supply voltage	$V_P = V_{10-18}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	35	50	mA
Colour difference channels (pins 1 and 2);					
(R-Y) input voltage (peak-to-peak value)					
75% colour bar signal	V_{1-18}	–	1,05	–	V
(B-Y) input voltage (peak-to-peak value)					
75% colour bar signal	V_{2-18}	–	1,33	–	V
Input resistance	$R_{1, 2-18}$	–	12	–	kΩ
Internal bias (input)	$V_{1, 2-18}$	–	4,3	–	V
(B-Y), (R-Y) signal attenuation $\frac{V_8}{V_1}, \frac{V_7}{V_2}$	α_{cd}	–	0	–	dB
Output voltage (d.c.)	$V_{7, 8-18}$	–	4,4	–	V
Output current (emitter follower with constant current source 0,65 mA)	$-I_{7,8}$	–	1,2	–	mA
(R-Y) and (B-Y) output signal transient time	t_{tr}	–	150	–	ns
Y-signal path (pin 17)					
Y-input voltage (composite signal) (peak-to-peak value)	$V_{17-18(p-p)}$	–	1	–	V
Internal bias voltage (during clamping)	V_{17-18}	–	1,5	–	V
Input current					
during picture content	I_{17}	–	8	–	μA
during synchronizing pulse	$-I_{17}$	–	100	–	μA
Y-signal attenuation $\frac{V_{11}}{V_{17}}$	α_Y	–	8	–	dB
Y-signal attenuation $\frac{V_{12}}{V_{17}}$	α_Y	–	7	–	dB
Output voltage (d.c.)	V_{11-18}	–	2,3	–	V
Output voltage (d.c.)	V_{12-18}	–	10,3	–	V
Output current (emitter follower with constant current source 0,45 mA)	$-I_{11,12}$	–	1,2	–	mA
Frequency response (note 1)					
R_{14-18} = 1,2 kΩ; V_{15-18} = 12 V	f_{12-17}	–	5	–	MHz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Y-signal path (pin 17)					
Adjustable delay (note 2) (switch open)					
at V_{15-18} = 0 to 2,5 V; R_{14-18} = 1,2 kΩ	t_d	–	720	–	ns
at V_{15-18} = 3,5 to 5,5 V; R_{14-18} = 1,2 kΩ	t_d	–	810	–	ns
at V_{15-18} = 6,5 to 8,5 V; R_{14-18} = 1,2 kΩ	t_d	–	900	–	ns
at V_{15-18} = 9,5 to12 V; R_{14-18} = 1,2 kΩ	t_d	–	990	–	ns
Fine adjustment delay (switch S1 closed)					
at V_{13-18} = 0 V	Δt_d	–	45	–	ns
Signal delay for velocity modulation (pin 11)	t		t_d – 90 ns		
Thermal resistance					
From junction to ambient (in free air)	$R_{th\ j-a}$	–	–	70	K/W

Notes

1. R_{14-18} influences the bandwidth.
2. Delay time is proportional to resistor R_{14-18}.



(1) Residual carrier reduced to 20 mV peak-to-peak (R = 1 kΩ, C = 100 pF).
(2) Switching sequence for delay times shown in Table 1.

Fig.2 Application diagram and test circuit.

Table 1 Switching sequence for delay times.

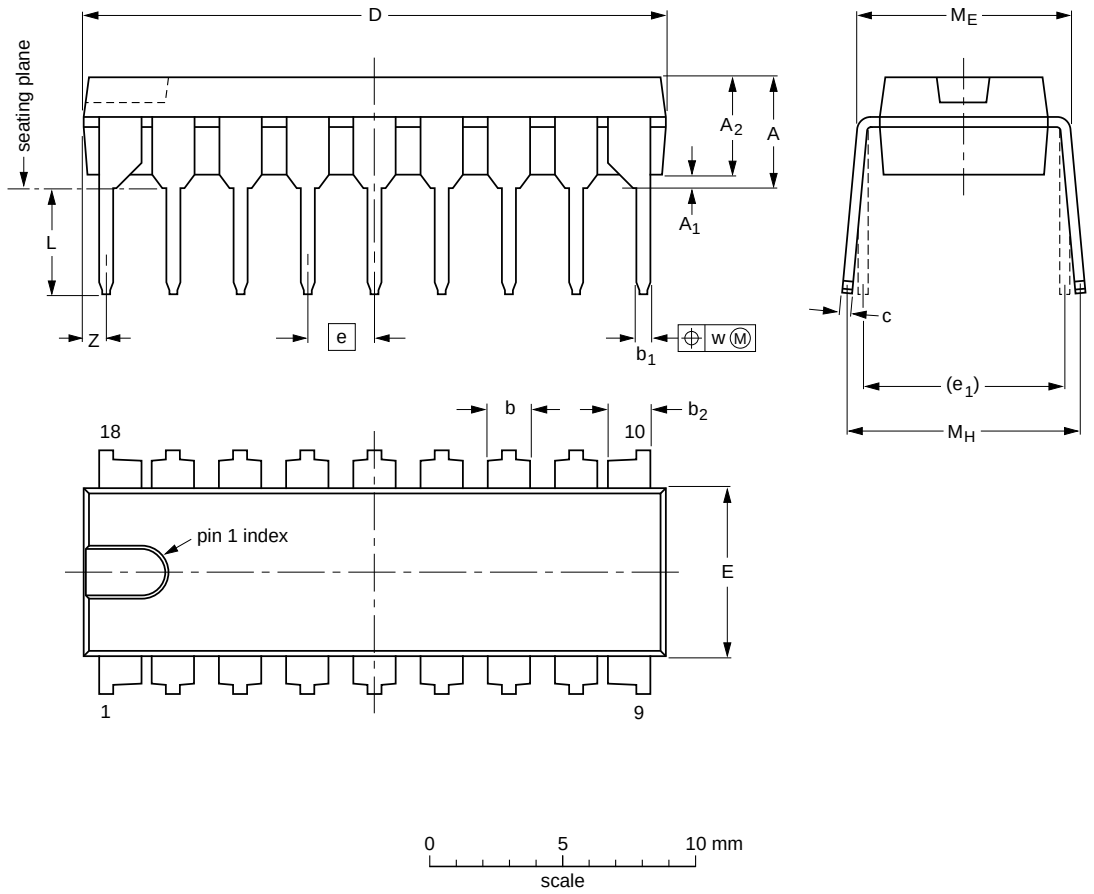
CONNECTION (2)			VOLTAGE AT PIN 15	DELAY TIME (ns) (1)
(A)	(B)	(C)		
O	O	O	0 to 2,5 V	720
O	O	X	3,5 to 5,5 V	810
O	X	X	6,5 to 8,5 V	900
X	X	X	9,5 to 12 V	990

Note

1. When switch (S1) is closed the delay time is increased by 45 ns.
2. Where: X = connection closed; O = connection open.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.