DATA SHEET

TDA3605Q
Multiple voltage regulator with switch

Preliminary specification
Supersedes data of 1995 Nov 20
File under Integrated Circuits, IC01

1997 Jul 09

FEATURES

- Two V_P-state controlled regulators (regulator 1 and regulator 3) and a power switch
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and the power switch
- Supply voltage range of –18 to +50 V (operating from 11 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3, and power switch are switched off)
- Hold output (only valid when regulator 1 is switched on)
- Reset and hold outputs (open collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Back-up capacitor for regulator 2.

PROTECTIONS

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protected on all pins
- Thermal protection
- Local thermal protection for power switch
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- Delayed second current limit protection for the power switch (at short-circuit)
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3605Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. It contains:

1. Two fixed voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.
2. A power switch with protections, operated by an enable input.
3. Reset and hold outputs can be used to interface by the microcontroller. The reset signal can be used to call up the microcontroller and the hold output indicates regulator 1 voltage available and within range.
4. A supply pin which can withstand load dump pulses and negative supply voltage.
5. Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.
6. Also there is a provision for use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3605Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		11	14.4	18	V
	reverse battery		–18	–	–	V
	regulator 2 on		2.4	14.4	18	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	during ≤50 ms; t_r ≥ 2.5 ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	500	600	μA
T_j	junction temperature		–	–	150	°C
Voltage regulators						
V_{REG1}	output voltage regulator 1	0.5 mA ≤ I_{REG1} ≤ 600 mA	9.5	10.0	10.5	V
V_{REG2}	output voltage regulator 2	0.5 mA ≤ I_{REG2} ≤ 300 mA; V_P = 14.4 V	4.75	5.0	5.25	V
V_{REG3}	output voltage regulator 3	0.5 mA ≤ I_{REG3} ≤ 400 mA	4.75	5.0	5.25	V
Power switch						
$V_{sw(d)}$	drop-out voltage	I_{sw} = 1 A	–	0.45	0.7	V
		I_{sw} = 1.8 A	–	1	1.8	V
I_{swM}	peak current		3	–	–	A

BLOCK DIAGRAM

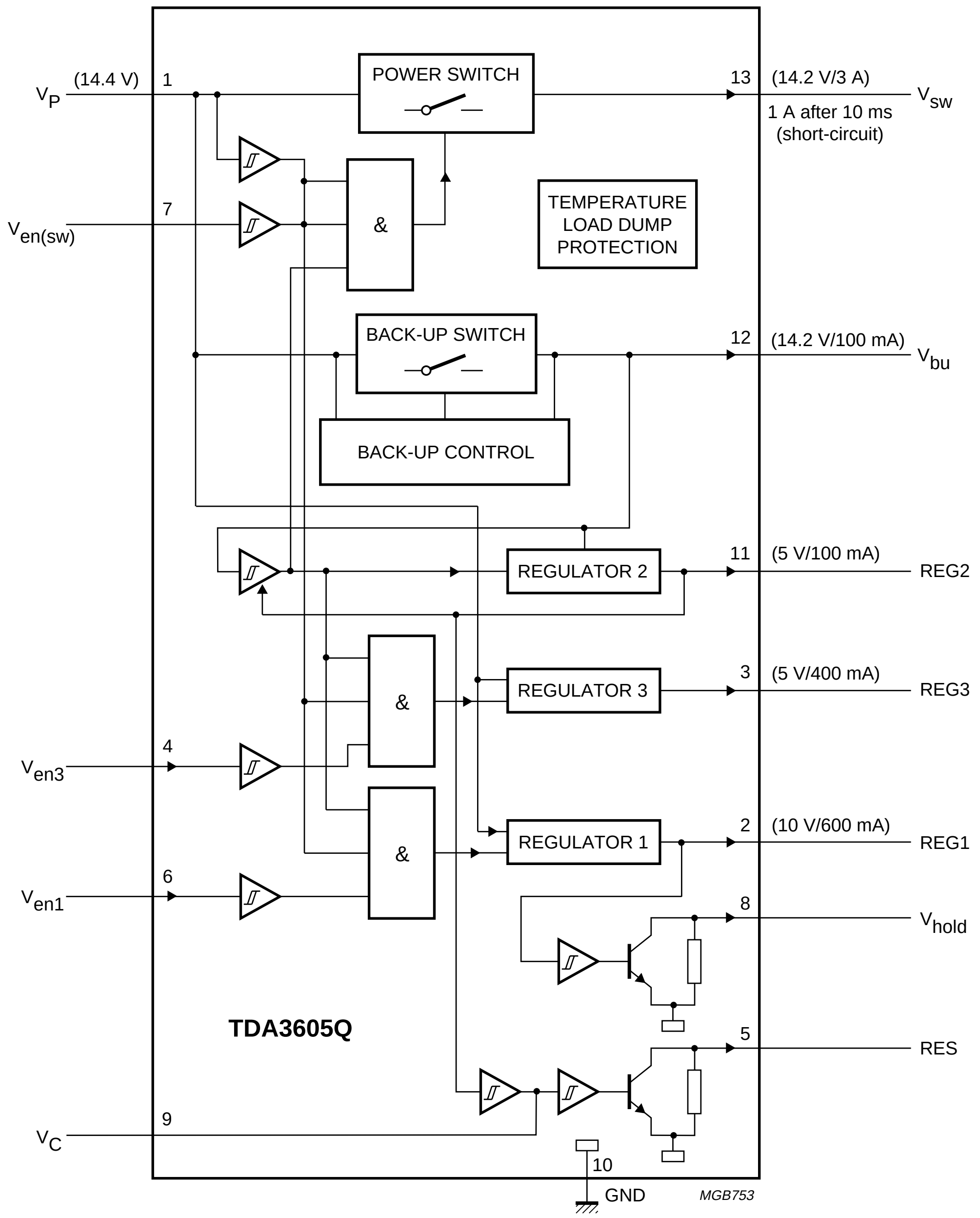


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	supply voltage
REG1	2	regulator 1 output
REG3	3	regulator 3 output
V_{en3}	4	enable input regulator 3
RES	5	reset output voltage
V_{en1}	6	enable input regulator 1
$V_{en(sw)}$	7	enable input power switch
V_{hold}	8	hold output
V_C	9	reset delay capacitor
GND	10	ground (0 V)
REG2	11	regulator 2 output
V_{bu}	12	back-up
V_{sw}	13	power switch output voltage

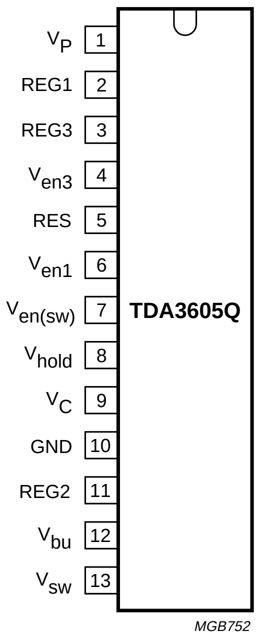


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3605Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used in the TDA3605Q.

Regulator 2 will switch-on when the back-up voltage exceeds 6.5 V for the first time and will switch-off again when the output voltage of regulator 2 is below 1.9 V (this is far below an engine start). When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output will be enabled (reset will go HIGH via a pull-up resistor) to generate a reset to the microcontroller. The reset cycles can be extended by an external capacitor at pin 9. The above mentioned start-up feature is built-in to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

The charge of the back-up capacitor can be used to supply regulator 2 for a short period when the supply falls to 0 V (time depends on value of storage capacitor). When both regulator 2 and the supply voltage (V_P > 4.5 V) are available, regulators 1 and 3 can be operated by means of enable inputs (pins 6 and 4 respectively).

Regulator 1 has a hold output (open collector) indicating that the output voltage of this regulator is settled (held HIGH by external pull-up resistor) and when the output voltage of this regulator drops out of regulation (because of supply voltage drop or high load) the hold output will go LOW. The hold output signal is only valid when regulator 1 is enabled by its enable input (pin 6).

The power switch can also be controlled by means of a separate enable input (pin 7).

All output pins are fully protected. The regulators are protected against load dump (regulator 1 and 3 will switch off at supply voltages >18 V) and short-circuit (foldback current protection).

The switch contains a current protection, but this protection is delayed at short-circuit condition for at least 10 ms. During this time the output current is limited to a peak value of at least 3 A and 2 A (DC) ($V_P \leq 18$ V). At supply voltages >17 V the switch is clamped at maximum 16 V (to avoid external connected circuitry being damaged by an overvoltage) and the switch will switch-off at load dump.

The total timing of a semi on/off logic set is shown in Fig.3.

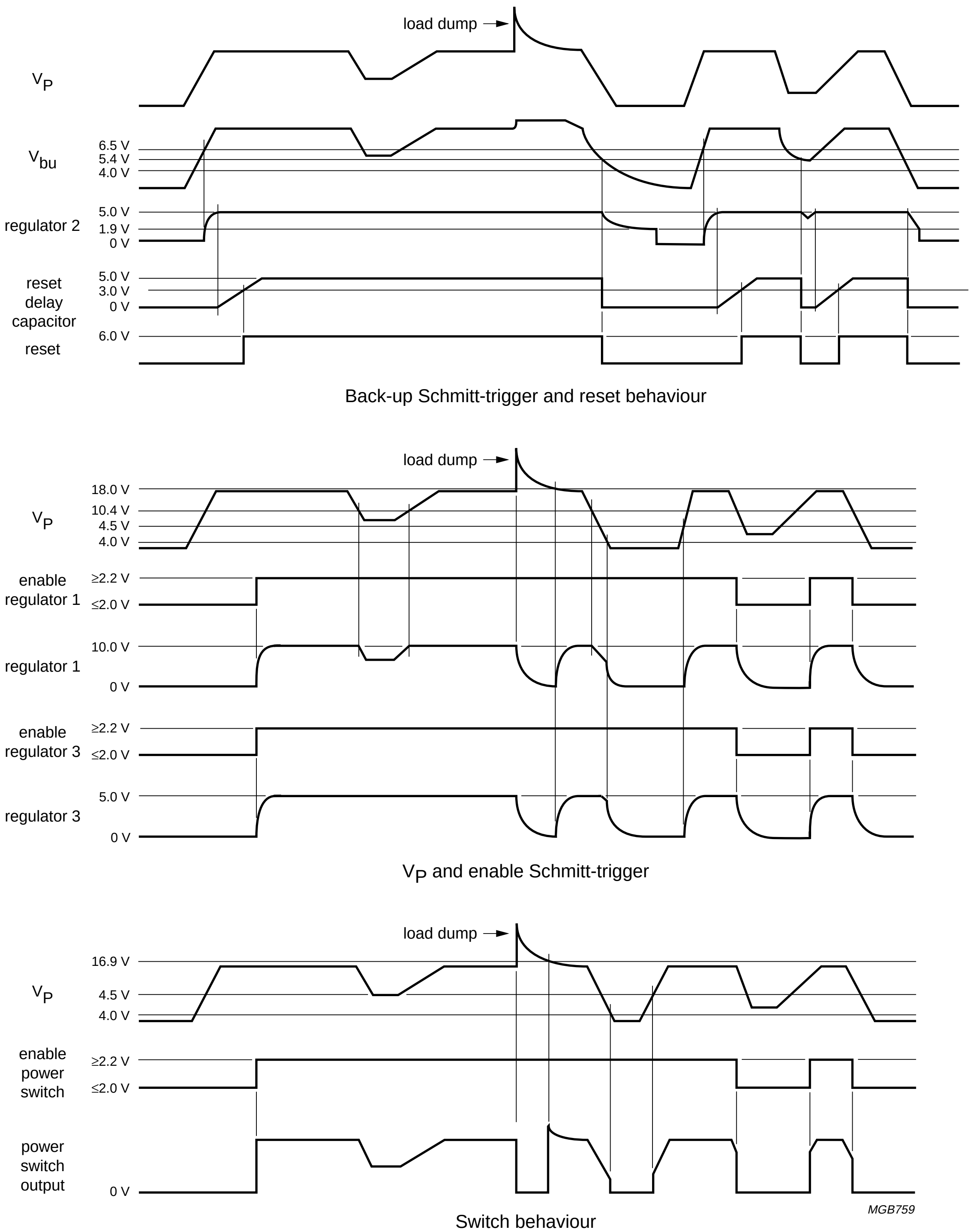


Fig.3 Timing diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	jump start	t ≤ 10 minutes	–	30	V
	load dump protection	during ≤50 ms; t_r ≥ 2.5 ms	–	50	V
V_P	reverse battery voltage	non-operating	–	–18	V
P_{tot}	total power dissipation		–	62	W
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	2	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	50	K/W

CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; see Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		11	14.4	18	V
	regulator 2 on	note 1	2.4	14.4	18	V
	jump start	t ≤ 10 minutes	–	–	30	V
	load dump protection	during ≤50 ms; t_r ≥ 2.5 ms	–	–	50	V
I_q	quiescent current	V_P = 12.4 V; note 2; I_{R2} = 0.1 mA	–	500	600	µA
		V_P = 14.4 V; note 2; I_{R2} = 0.1 mA	–	520	–	µA
Schmitt-trigger power supply for switch, regulator 1 and regulator 3						
V_{thr}	rising voltage threshold		4.0	4.5	5.0	V
V_{thf}	falling voltage threshold		3.5	4.0	4.5	V
V_{hys}	hysteresis		–	0.5	–	V
Schmitt-trigger power supply for regulator 2						
V_{thr}	rising voltage threshold		6.0	6.5	7.1	V
V_{thf}	falling voltage threshold		1.7	1.9	2.2	V
V_{hys}	hysteresis		–	4.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Schmitt-trigger for enable input (regulator 1, regulator 3 and switch)						
V_{thr}	rising voltage threshold		1.7	2.2	2.7	V
V_{thf}	falling voltage threshold		1.5	2.0	2.5	V
V_{hys}	hysteresis	$I_{REG} = I_{SW} = 1$ mA	0.1	0.2	0.5	V
I_{LI}	input leakage current	$V_{en} = 5$ V	1	5	10	μA
Schmitt-trigger for reset buffer						
V_{thr}	rising voltage threshold of regulator 2	V_P rising; $I_{REG1} = 50$ mA; note 3	–	$V_{REG2} – 0.15$	$V_{REG2} – 0.075$	V
V_{thf}	falling voltage threshold of regulator 2	V_P rising; $I_{REG1} = 50$ mA; note 3	4.3	$V_{REG2} – 0.35$	–	V
V_{hys}	hysteresis		0.1	0.2	0.3	V
Schmitt-trigger for hold						
V_{thr}	rising voltage threshold of regulator 1	V_P rising; note 3	–	$V_{REG1} – 0.15$	$V_{REG1} – 0.075$	V
V_{thf}	falling voltage threshold of regulator 1	V_P rising; note 3	9.2	$V_{REG1} – 0.35$	–	V
V_{hys}	hysteresis		0.1	0.2	0.3	V
Reset and hold buffer						
I_{Lsink}	LOW level sink current	$V_{RES/hold} \leq 0.8$ V	2	–	–	mA
I_{LO}	output leakage current	$V_P = 14.4$ V; $V_{RES/hold} = 5$ V	–	16	32	μA
t_r	rise time	note 4	–	7	50	μs
t_f	fall time	note 4	–	1	50	μs
Reset delay						
I_{ch}	charge current		2	4	8	μA
I_{dch}	discharge current		500	800	–	μA
V_{thr}	rising voltage threshold		2.5	3.0	3.5	V
t_d	delay time	C = 47 nF; note 5	20	35	70	ms
Regulator 1 (I_{REG1} = 5 mA)						
$V_{REG1(off)}$	output voltage off		–	1	400	mV
V_{REG1}	output voltage	1 mA $\leq I_{REG1} \leq$ 600 mA	9.5	10.0	10.5	V
		11 V $\leq V_P \leq$ 18 V	9.5	10.0	10.5	V
ΔV_{REG1}	line regulation	11 V $\leq V_P \leq$ 18 V	–	2	75	mV
ΔV_{REGL1}	load regulation	1 mA $\leq I_{REG1} \leq$ 600 mA	–	20	50	mV
I_q	quiescent current	$I_{R1} = 600$ mA	–	25	60	mA
SVRR1	supply voltage ripple rejection	$f_i = 3$ kHz; $V_{i(p-p)} = 2$ V	60	70	–	dB
V_{REGd1}	drop-out voltage	$I_{REG1} = 550$ mA; $V_P = 9.5$ V; note 6	–	0.4	0.7	V
I_{REGm1}	current limit	$V_{REG1} > 8.5$ V; note 7	0.65	1.2	–	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{REGsc1}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 8	250	800	–	mA
Regulator 2 (I_{REG2} = 5 mA)						
V_{REG2}	output voltage	0.5 mA $\leq I_{REG2} \leq$ 150 mA	4.75	5.0	5.25	V
		0.5 mA $\leq I_{REG2} \leq$ 300 mA	4.75	5.0	5.25	V
		7 V $\leq V_P \leq$ 18 V	4.75	5.0	5.25	V
		18 V $\leq V_P \leq$ 50 V; $I_{REG2} \leq$ 150 mA	4.75	5.0	5.25	V
ΔV_{REG2}	line regulation	6 V $\leq V_P \leq$ 18 V	–	2	50	mV
		6 V $\leq V_P \leq$ 50 V	–	15	75	mV
ΔV_{REGL2}	load regulation	1 mA $\leq I_{REG2} \leq$ 150 mA	–	20	50	mV
		1 mA $\leq I_{REG2} \leq$ 300 mA	–	–	100	mV
SVRR2	supply voltage ripple rejection	f = 3 kHz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_{REGd2}	drop-out voltage	I_{REG2} = 100 mA; V_P = 4.75 V; note 6	–	0.4	0.6	V
		I_{REG2} = 200 mA; V_P = 5.75 V; note 6	–	0.8	1.2	V
		I_{REG2} = 100 mA; V_{bu} = 4.75 V; note 7	–	0.2	0.5	V
		I_{REG2} = 200 mA; V_{bu} = 5.75 V; note 7	–	0.8	1.0	V
I_{REGm2}	current limit	V_{REG2} > 4.5 V; note 7	0.32	0.37	–	A
I_{REGsc2}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 8	20	100	–	mA
Regulator 3 (I_{REG3} = 5 mA)						
$V_{REG3(off)}$	output voltage off		–	1	400	mV
V_{REG3}	output voltage	1 mA $\leq I_{REG3} \leq$ 400 mA	4.75	5.0	5.25	V
		7 V $\leq V_P \leq$ 18 V	4.75	5.0	5.25	V
ΔV_{REG3}	line regulation	7 V $\leq V_P \leq$ 18 V	–	2	50	mV
ΔV_{REGL3}	load regulation	1 mA $\leq I_{REG3} \leq$ 400 mA	–	20	50	mV
I_q	quiescent current	I_{R3} = 400 mA	–	15	40	mA
SVRR3	supply voltage ripple rejection	f_i = 3 kHz; $V_{i(p-p)}$ = 2 V	60	70	–	dB
V_{REGd3}	drop-out voltage	I_{REG3} = 400 mA; V_P = 5.75 V; note 6	–	1	1.5	V
I_{REGm3}	current limit	V_{REG3} > 4.5 V; note 7	0.45	0.70	–	A
I_{REGsc3}	short-circuit current	$R_L \leq 0.5\ \Omega$; note 8	100	400		mA

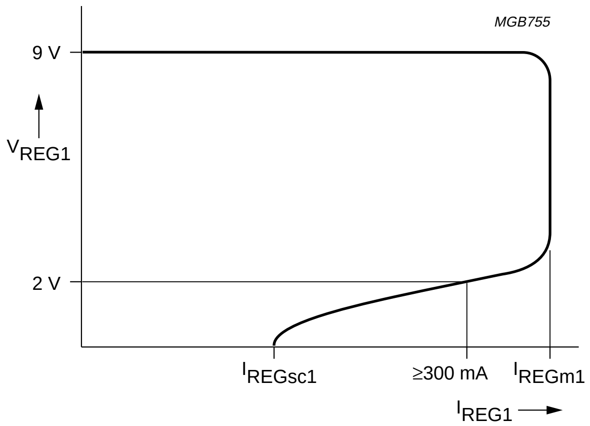
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power switch						
V_{swd}	drop-out voltage	I_{sw} = 1 A; note 10	–	0.45	0.7	V
		I_{sw} = 1.8 A; note 10	–	1.0	1.8	V
$I_{sw(dc)}$	continuous current	V_P = 16 V; V_{SW} = 13.5 V	1.8	2.0	–	A
V_{swcl}	clamping voltage	$V_P \geq 17$ V	13.5	15.0	16.0	V
I_{swM}	peak current	V_P = 17 V; notes 11 and 12	3	–	–	A
V_{swfb}	fly back voltage behaviour	I_{sw} = –100 mA	–	V_P + 3	22	V
$I_{sw(sc)}$	short-circuit current	V_P = 14.4 V; $V_{sw} \leq 1.2$ V; note 12	–	0.8	–	A
Back-up switch						
$I_{bu(DC)}$	continuous current		0.3	0.35	–	A
V_{bucl}	clamping voltage	$V_P \geq 16.7$ V	–	–	16	V
V_r	reverse current	V_P = 0 V; V_{bu} = 12.4 V	–	–	900	ms

Notes

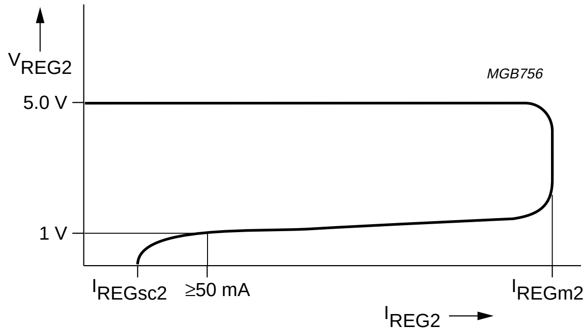
1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The quiescent current is measured in the standby mode. So, the enable inputs of regulators 1 and 3 and the switch are grounded and R2 = ∞ (see Fig.6).
3. The voltage of the regulator sinks as a result of a V_P drop.
4. The rise and fall times are measured with a 10 kΩ pull-up resistor and a 50 pF load capacitor.
5. The delay time depends on the value of the capacitor:

$$t_d = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (750 \times 10^3) \text{ (ms)}$$

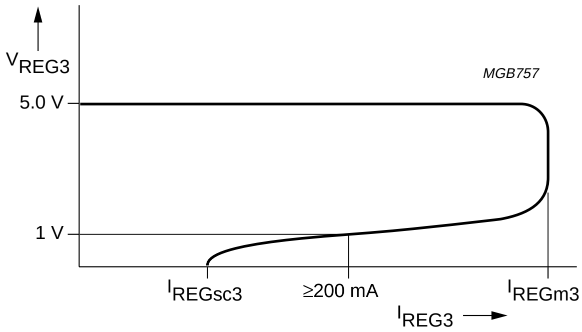
6. The drop-out voltage of regulators 1, 2 and 3 is measured between V_P and V_{REGn}.
7. At current limit, I_{REGmn} is held constant (see Fig.4 for behaviour of I_{REGmn}).
8. The foldback current protection limits the dissipated power at short-circuit (see Fig.4).
9. The peak current of 300 mA can only be applied for short periods (t < 100 ms).
10. The drop-out voltage of the power switch is measured between V_P and V_{sw}.
11. The maximum output current of the switch is limited to 1.8 A when the supply voltage exceeds 18 V.
A test-mode is built-in. The delay time of the switch will be disabled when a voltage of V_P + 1 V is applied to the switch enable input.
12. At short circuit, $I_{sw(sc)}$ of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms. A test-mode is built-in. The delay time of the switch will be disabled when a voltage of V_P + 1 V is applied to the switch enable input.



a. Regulator 1.

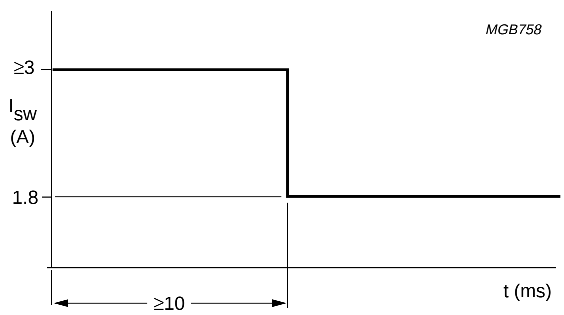


b. Regulator 2.



c. Regulator 3.

Fig.4 Foldback current protection of the regulators.

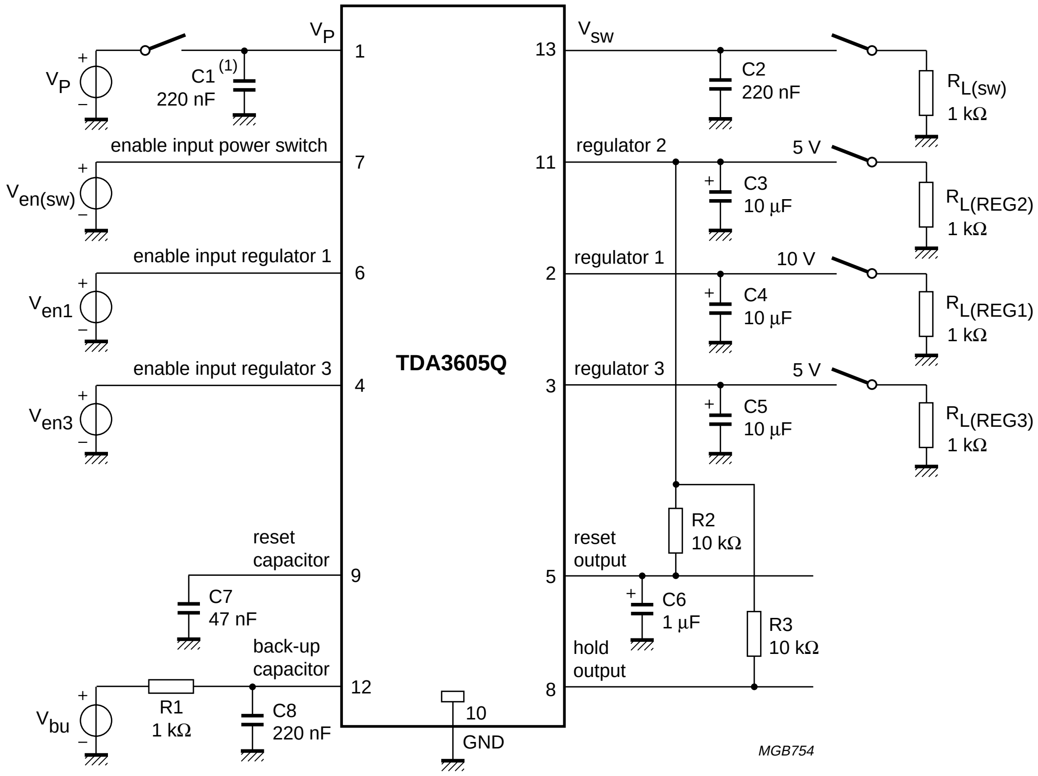


$V_{SW} \geq 5$ V.

Fig.5 Current protection of the power switch.

TEST AND APPLICATION INFORMATION

Test information



(1) Capacitor not required for stability.

Fig.6 Test circuit.

Application information

NOISE

Table 1 Noise figures

REGULATOR	NOISE FIGURE (µV)[1] at OUTPUT CAPACITOR		
	10 µF	**47 µF**	**100 µF**
1	–	150	–
2	–	150	–
3	–	200	–

Note

1. Measured at a bandwidth of 200 kHz.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated into a current noise by means of the output capacitors).

When a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 µF is connected directly to pins 3 and 8 (supply and ground) the noise is minimal.

STABILITY

The regulators are made stable with the externally connected output capacitors. The value of the output capacitors can be selected by referring to the graphs illustrated in Figs 7 and 8.

When an electrolytic capacitor is used the temperature behaviour of this output capacitor can cause oscillations at cold temperature.

The following two examples explain how an output capacitor value is selected.

Example 1

Regulator 1 is made stable with an electrolytic output capacitor of 220 μF (ESR = 0.15 Ω). At –30 °C the capacitor value is decreased to 73 μF and the ESR is increased to 1.1 Ω. The regulator will remain stable at –30 °C.

Example 2

Regulator 2 is made stable with a 10 μF electrolytic capacitor (ESR = 3 Ω). At –30 °C the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω. The regulator will be unstable at –30 °C (see Fig.7).

Solution

Use a tantalum capacitor of 10 μF or a large electrolytic capacitor. The use of tantalum capacitors is recommended to avoid problems with stability at cold temperatures.

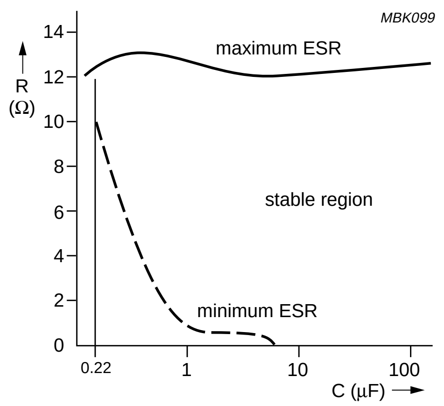


Fig.7 Curve for selecting the value of output capacitor for regulator 2.

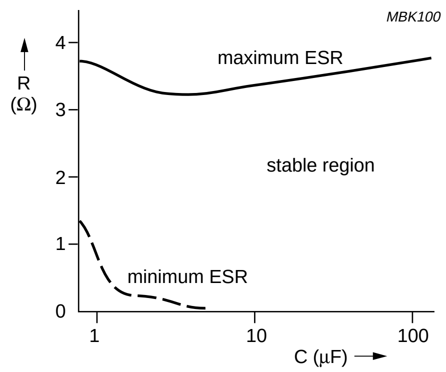
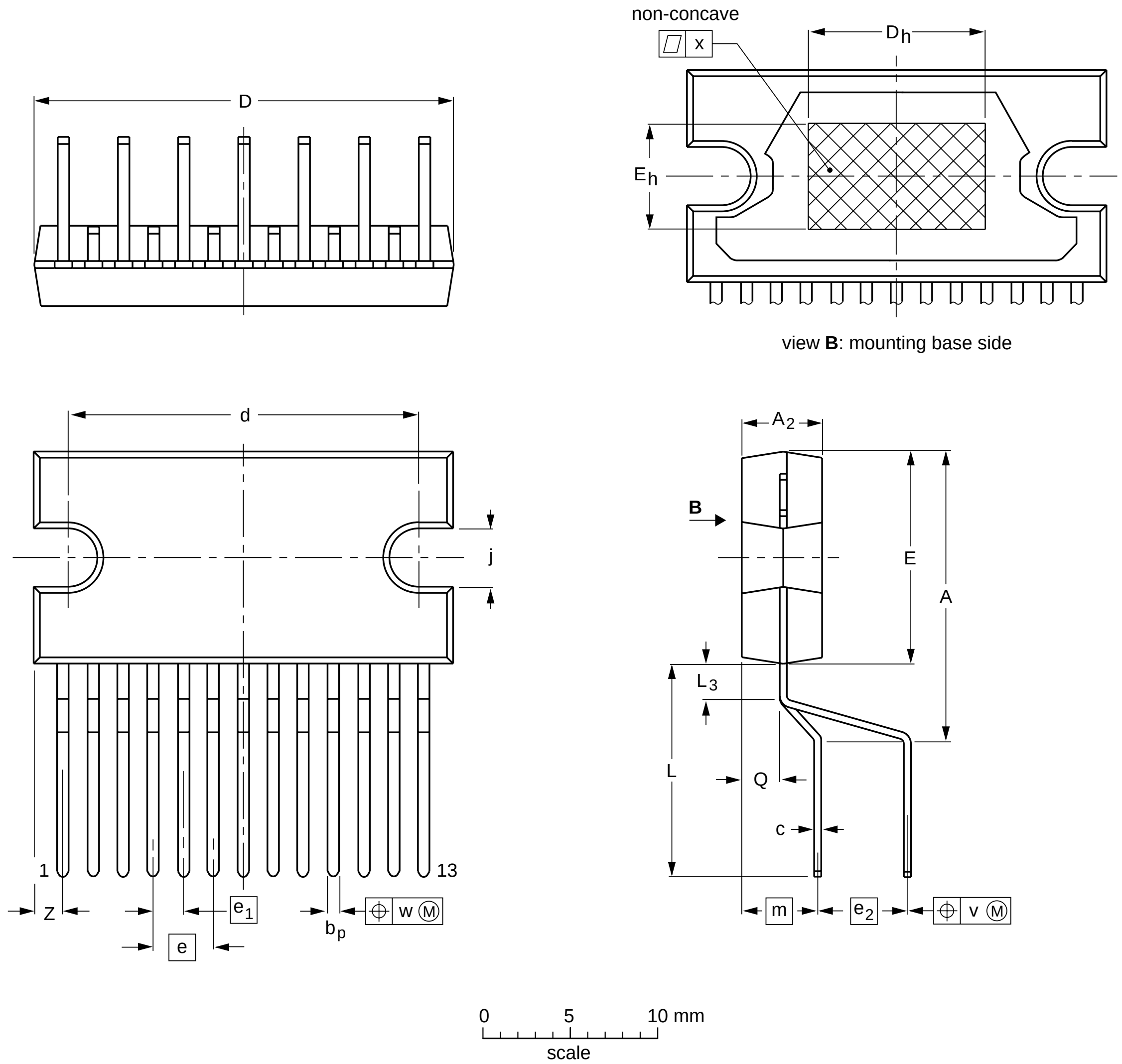


Fig.8 Curve for selecting the value of output capacitor for regulators 1 and 3.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	D(1)	d	D_h	E(1)	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	Z(1)
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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