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TDA 16888

High Performance Power Combi Controller

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TDA 16888 – High Performance Power Combi Controller

Introduction

TDA 16888 is designed for new generations of off-line Switched Mode Power Supplies (SMPS) with optional universal input and Power Factor Correction (PFC) e.g. for PCs, Monitors, CTVs and industrial applications.

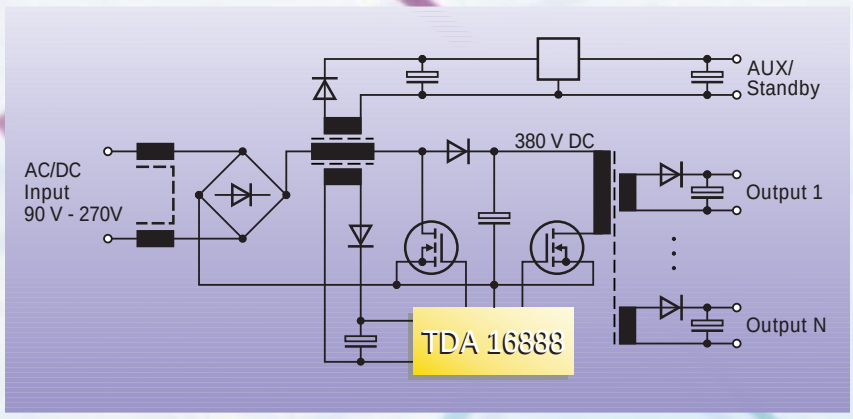


Figure 1 Basic Application Circuitry

Functionality and Benefits

This high performance SMPS Power Combi Controller is optimized to reduce system costs, supports solutions for global requirements, generates less EMI and is designed by FMEA rules.

The TDA 16888 allows load variations down to zero watts and controls low power standby operation by switching off its Pulse Width Modulation (PWM) stage.

The Power Combi Control-IC TDA 16888 includes the PWM control for an SMPS and the control for the preconverter to improve the power factor and to reduce the harmonics of the AC input current. Both sections are internally synchronized on the same operating frequency.

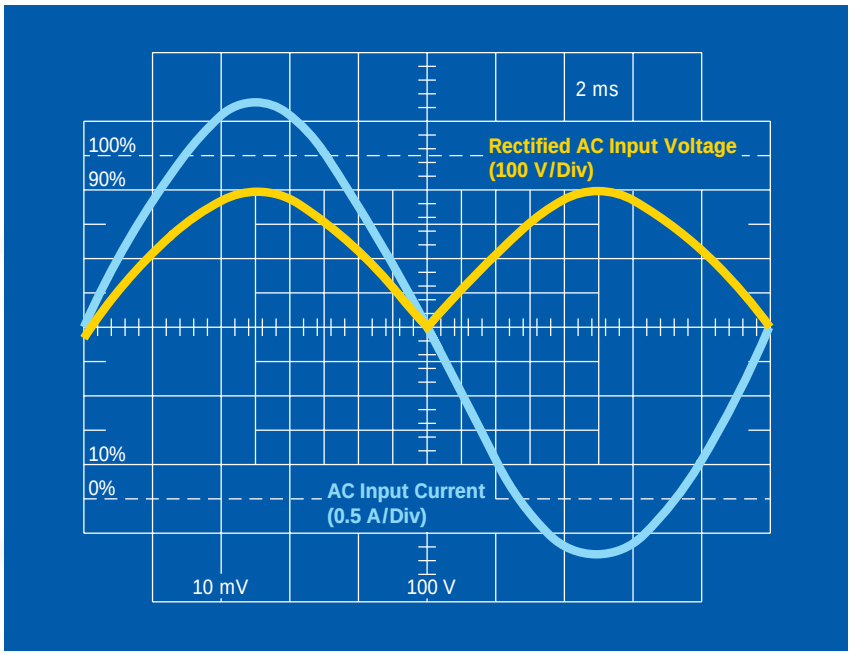


Figure 2 Input Signals

The preferred topology of the PFC preconverter is boost, but flyback is possible, too. The PWM section can be designed as a forward or as a flyback converter. Maximum duty cycle of the PFC is about 94%, in order to achieve minimal line current gaps. Maximum duty cycle of the PWM is limited to 50% to prevent transformer saturation.

There are monitoring and protection functions such as broken wire detection, undervoltage and dual step overvoltage monitoring of the bus voltage, peak current limitation for PFC and PWM section and undervoltage lockout of the IC supply voltage. The Combi-IC TDA 16888 is designed with respect to a Failure Mode Effect Analysis (FMEA).

The limitation of the PWM duty cycle, i.e. the leading edge PFC- and the trailing edge PWM operation, are done in a digital way by flip-flops. Handling the signals this way meets the requirements for an external synchronisation. On the other hand an oscillator is necessary that operates at twice of the operating frequency. For a lower current consumption and higher EMI resistance the capacitor of the oscillator is integrated. The operating frequency is set by only one resistor. The operating frequency can be increased by a sink current in parallel to this resistor. There is an additional synchronisation input that can be used for frequency adjustment or in connection with a phase locked operation.

PFC Preconverter

In normal operation the PFC section of TDA 16888 operates with dual loop control. A first control loop controls the shape of the line current by average current control enabling either continuous or discontinuous operation mode.
The second loop controls the DC bus voltage. There is a third control loop available that enables the PFC section as an auxiliary power supply even when the PWM section is disabled. During standby operation mode (disabled PWM) the PFC section is operating with half of its nominal operating frequency in order to save operating power.

Rectification of an AC voltage and smoothing with an electrolytic capacitor effects a peak current during the peak input voltage and a break in current flow during the rest of the half period of the line frequency. The RMS value of such a pulsed input current is about twice of a sinusoidal current and the harmonics of that pulsed current effect EMI to other devices. The power factor is the relation between real input power to apparent input power. With a typical main voltage rectification in electronic devices the power factor is about 0.5. Standards to improve the power factor will become effective in the near future.

But system cost must not increase by introduction of power factor correction. It depends on the output power and features like the option to supply a device from different line voltages.

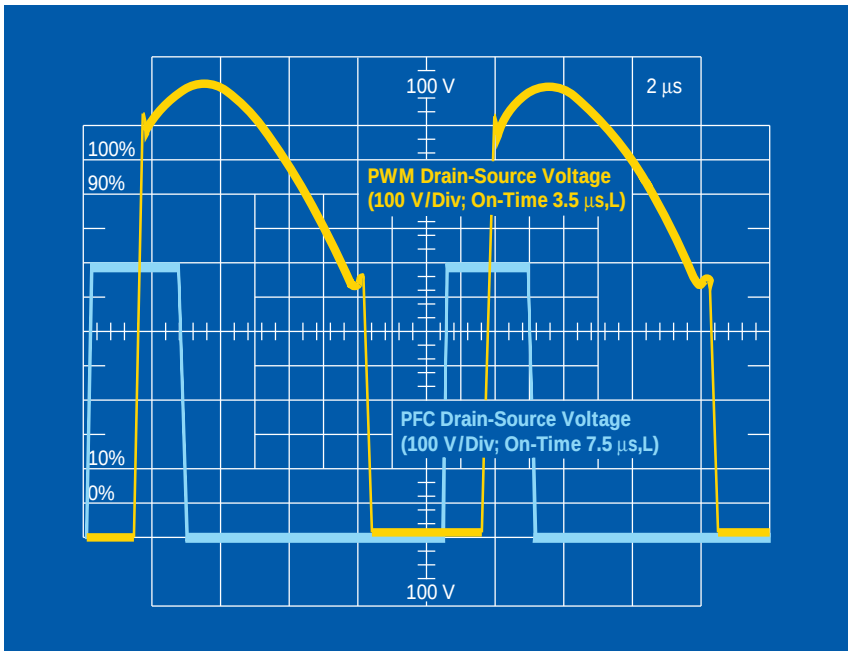


Figure 3 Output Signals

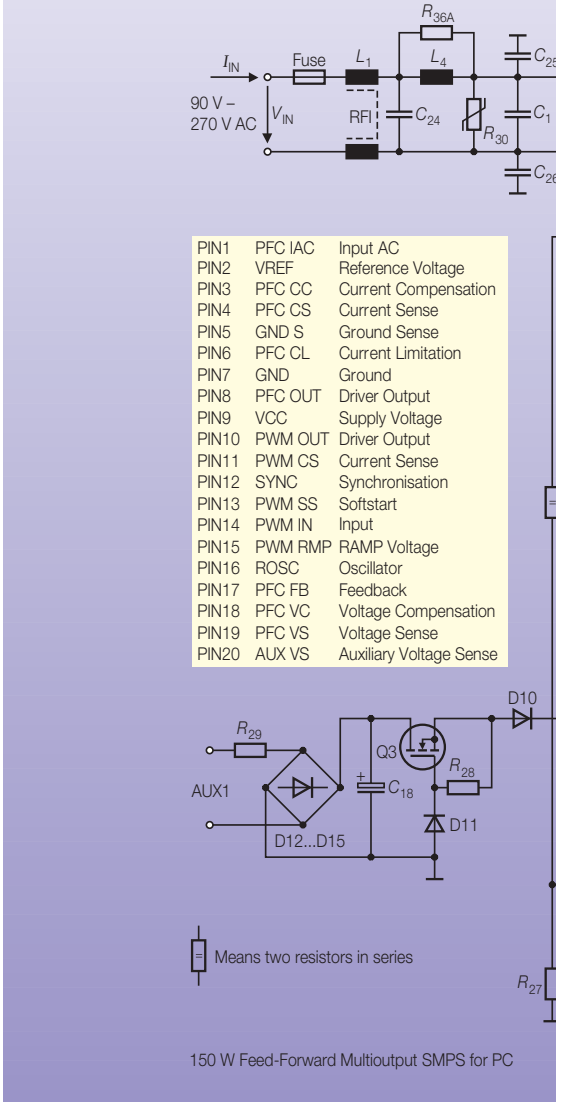
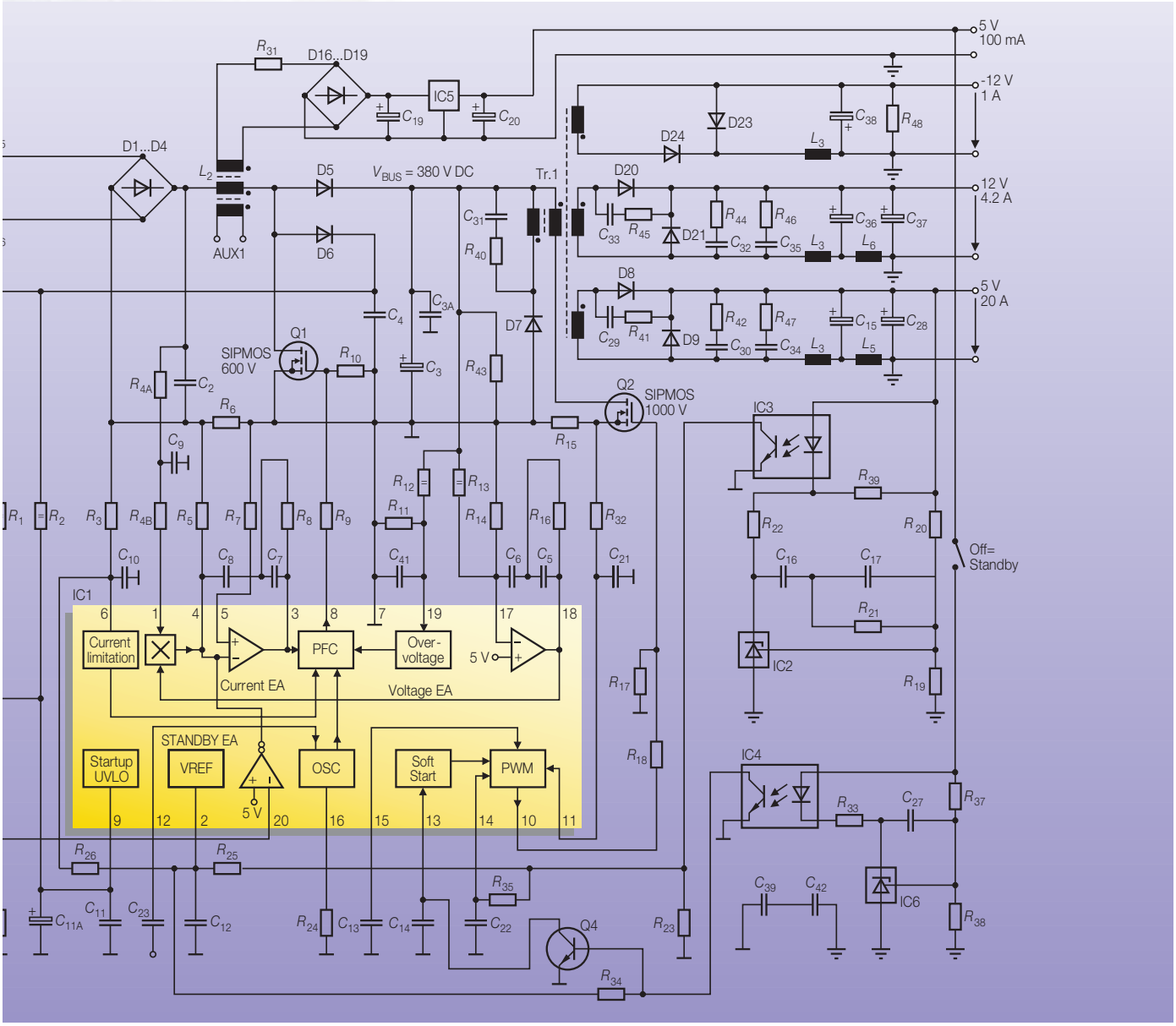


Figure 4 Application Circuitry

The most efficient way to correct the power factor with an active circuitry is to use a boost converter. Most of the energy flowing from the input via rectifiers to the bus capacitor bypasses the switching transistor of the boost converter. Connecting the boost preconverter to the line, an inrush current occurs due to charging the bus capacitor. As the capacitance of the bus capacitor is between three to ten times lower than with conventional rectification, the inrush current is much smaller even without additional measures like NTCs.

There is a peak current limitation (Pin 6) to prevent an overload of the boost transistor during inrush currents and during maximum load, which occurs for example after turn on to charge the bus capacitor. The turn off threshold is designed at +1 V to meet FMEA requirements. A broken wire to Pin 6 activates the current limitation. Another comparator (C2) at Pin 19 is detecting a broken wire to the bus voltage sense. At least 20% of nominal bus voltage is necessary to make the Combi-IC active. This feature has to be taken into account when testing the IC at low input voltages.



The typical startup of the Combi-IC is supported by the undervoltage lockout (UVLO) feature of the IC. Via a highly resistive resistor (R_2) a capacitor (C_{11}) is charged up to a threshold of 14 V at Pin 9. During this operation the current consumption of the IC is less than 100 µA. Reaching this threshold the IC becomes active sending drive pulses to the boost transistor Q1. During this operation the PWM section is not active yet in order to save supply current. The same reason is for driving the boost transistor with only half of the nominal operating frequency. Capacitor C_{11} has to be designed large enough that the circuitry is able to supply the IC before the voltage at Pin 9 reaches the turn off threshold of 11 V.

The power supply of the Combi-IC can be realized by a separate winding on the boost converter choke. Our proposal is to use a bridge rectifier on the auxiliary winding AUX 1. In this way a current can flow at low input voltages in flyback mode and at high input voltages in forward mode. The minimum supply voltage at capacitor C_{18} will occur at an input voltage level half of the bus voltage.

There is another operating condition when the supply voltage at C_{18} becomes low, i.e. at disabled PWM section and high input voltages. This condition may be the worst for the auxiliary power supply. In this application we got the power to supply the Combi-IC during all operating conditions and in addition the circuit offers an isolated auxiliary voltage of 5 V / 100 mA.

An increase of output power of the auxiliary power supply will be an option of future applications.
In order to continue the description of the auxiliary power supply there is a separate control loop and a separate output of the boost converter via diode D6. This additional circuitry is necessary to get a fast response at load changes. There are operating conditions resulting in an overshoot at the bus voltage that would stop the boost transistor for more than 100 ms. With the second output of the boost converter via D6 a not working transistor can be detected within 100 µs and the transistor can be turned on in a way, that the auxiliary output gets power but not the main output to the bus capacitor. During the standby operation the bus voltage remains at nominal level. The separate control loop can be activated by itself, when the second output of the boost converter via D6 is designed for an output voltage slightly below the nominal bus voltage (e.g. 5%). The load (R_2) which is necessary at the second output can be used for the startup of the Combi-IC.

The PFC section is working initially at half of the nominal operating frequency until a level of 20% below the nominal bus voltage is reached. Then the PWM section is able to run with a soft start (Pin 13) with nominal operating frequency on both sections or if it is disabled by transistor Q4, then the system is running in the standby mode with half of its nominal operating frequency.

Usually there is an overshoot during the charging of the bus capacitor. The reason is the long response time of the bus voltage control loop. There is a first overvoltage threshold at 10% above nominal bus voltage. The operation of the boost transistor is turned down via OTA2 and the Multiplier to avoid increasing bus voltage. A second threshold at 20% above nominal bus voltage will stop PFC and PWM section immediately until the bus voltage reaches a level of 10% above nominal bus voltage. This feature protects the power supply during hazardous mains overvoltages in combination with varistor R_{30}.

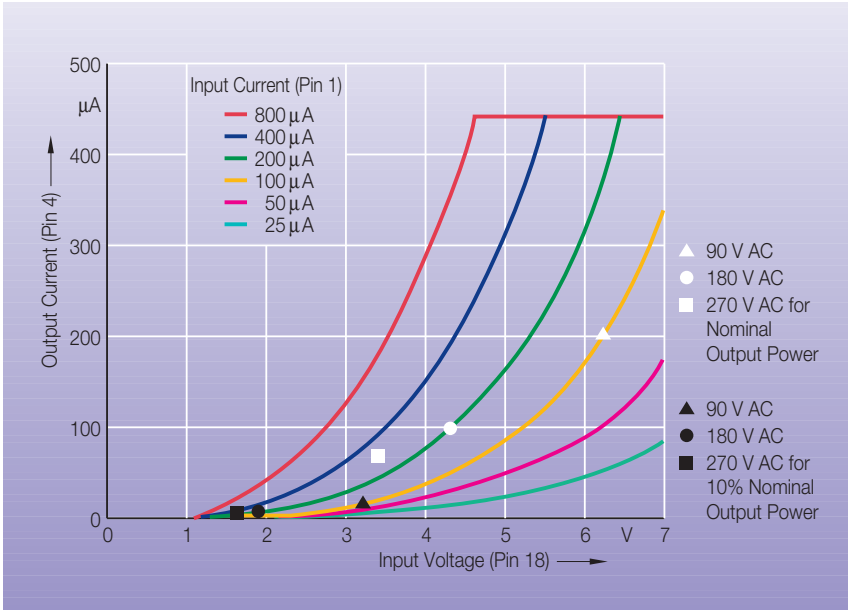


Figure 5 Dynamic Characteristics of the Multiplier

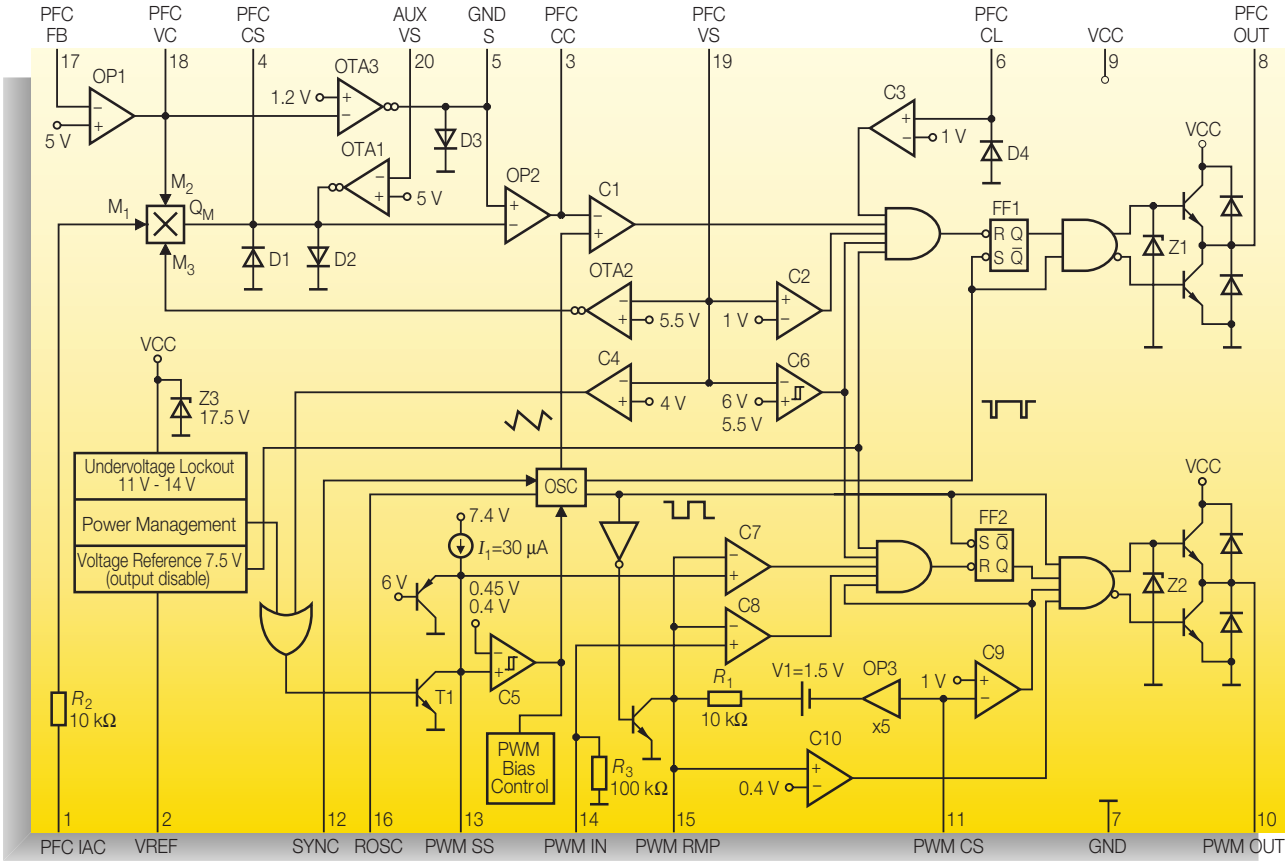


Figure 6 Block Diagram of TDA 16888

At typical operating mode of the PFC section a DC output signal with a small superimposed AC ripple can be found at the output of the voltage error amplifier OP1 at Pin 18. This signal is multiplied by the current at Pin 1, derived from the rectified AC input voltage. Consequently a multiplier output current shaped like the input voltage is achived, that can be varied in amplitude by the voltage error amplifier OP1.

A second error amplifier OP2 controls the input current like the set value of the multiplier output. In order to enlarge the effect of the voltage error amplifier OP1 there is an exponential function at the voltage input (Pin 18) of the multiplier included (cf. Figure 5).

Furthermore there is an OTA3 that cares for the stability of the bus voltage during light load and no load conditions.This is achieved by compensating the multiplier output current as long as the output voltage of OP1 is well below 1.2 V.

The ramp voltage of the PFC pulse width modulation starts from a higher voltage level of 6 V decreasing to the minimum of 1 V. The reason for this shape which is invers to commonly used ramp voltages is that the feedback of OP2 can be connected to the current sense input (Pin 4). In this way the sensed signal is smoothed and the levels at Pin 4 can be kept well above 0 V.

PWM Converter

The PWM section operates with improved current mode control, with effective slope compensation, spike suppression and especially with amplified signal levels at the pulse width comparator. The PWM section can be disabled by a short (controlled by transistor Q4) across the soft start capacitor.

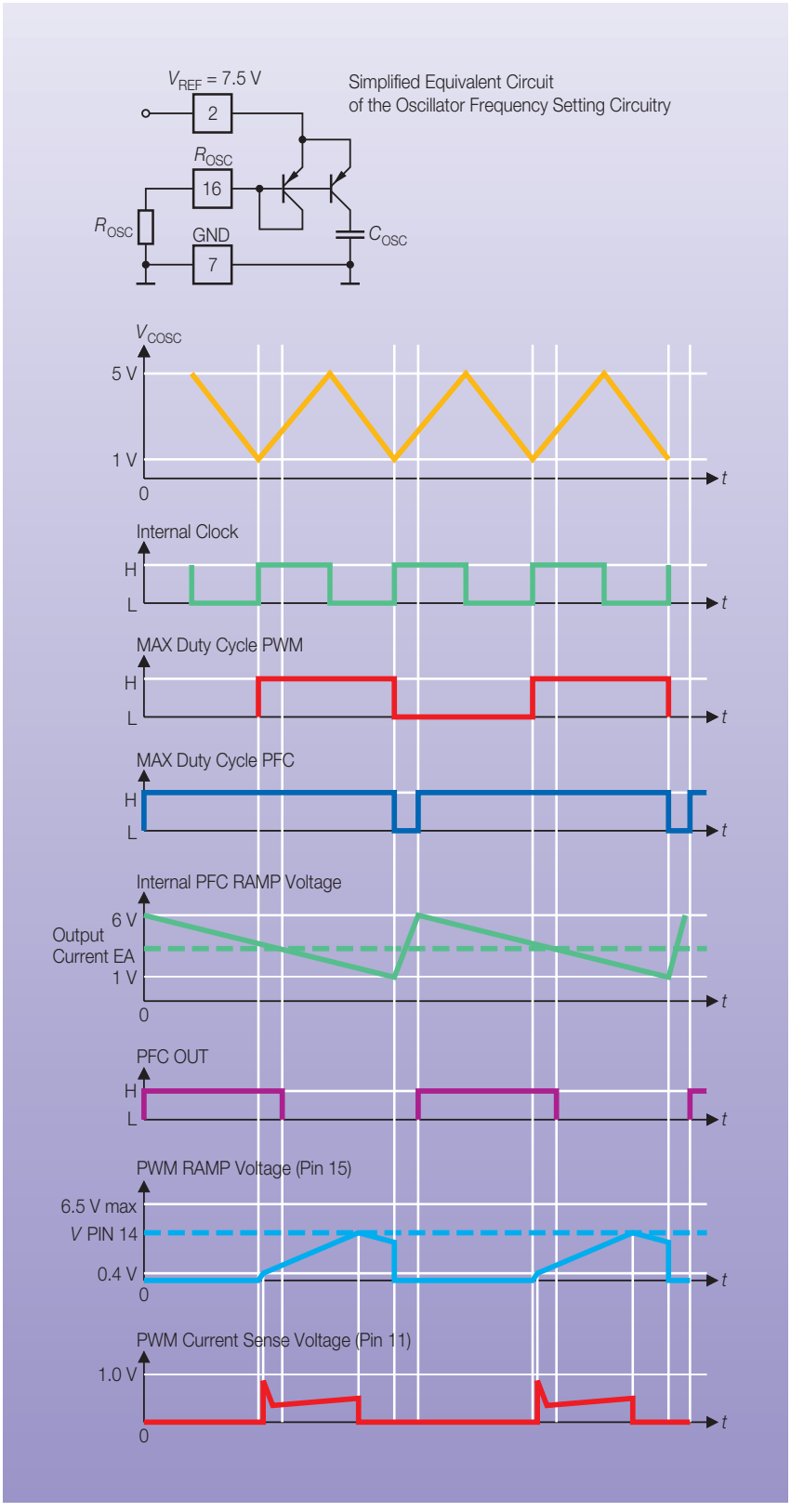


Figure 7 Typical Shape of Signals

The PWM converter starts with a soft start at a bus voltage higher than 80% of its nominal value. Operating frequency is the nominal and the same like that of the PFC preconverter. The transistor of the boost converter turns on with leading edge and that of the PWM turns on with trailing edge, delayed in minimum 50% of the operation period.

The way of control is an improved current mode. There is a capacitor at Pin 15, by means of which a basic ramp voltage is generated for slope compensation. This voltage is superimposed by the times 5 amplified voltage drop across the shunt resistor (R_{15}) fed over an internal 10 kΩ resistor in order to suppress spikes. The result is a ramp voltage with a maximum level up to 6.5 V. Correspondingly the active input range of the PWM input (Pin 14) is from 0.4 V to 7 V. The higher level on the PWM comparator cares for better resistance against EMI and better stability of operation (cf. Figure 3). In addition the current sense input (Pin 11) feeds a fast comparator (threshold = 1 V) for current limitation.

PFC and PWM Gate Drive

There is a new design for the gate drive of both sections. The employed totem pole configuration avoids cross conduction currents and has a voltage modulated turn on slope. The turn on slope increases moderately between 0 V and 3 V, increases slowly between 3 V and 5 V and increases moderately above 5 V up to the maximum of 12 V. The reason for this improved rising edge is a possible fast turn off as soon as the current limitation is activated, a continuously reduciable duty cycle down to zero and a soft current commutation from the boost or output diode to the transistor. The voltage modulation meets these demands independent of the load capacitance. The turn off is fast with a current capability of about 1.5 A peak.

When operating the Combi-IC below the undervoltage threshold, the drive outputs are active low.

Oscillator and Synchronisation

The oscillator operates with an integrated low tolerance capacitor and a special voltage and temperature compensated current mirror set by only one external resistor at Pin 16. The integration of this capacitor operating with a ramp voltage of 5 V increases the resistance against EMI and saves supply current due to its small value. The internal oscillator operates with twice of the external operating frequency for exact limitation of the PWM duty cycle below 50% by flip-flops. In the same way the leading edge turn on of the PFC and the trailing edge turn on of the PWM is generated.
Therefore the operating frequency can be changed during operation only by bypassing a current to the set resistor R_{24}.

Changing the frequency by the set current at Pin 16 does not influence the amplitude of the internal ramp voltage of the PFC pulse width modulation but will influence the external ramp voltage of the PWM at the external capacitor C_{13}.

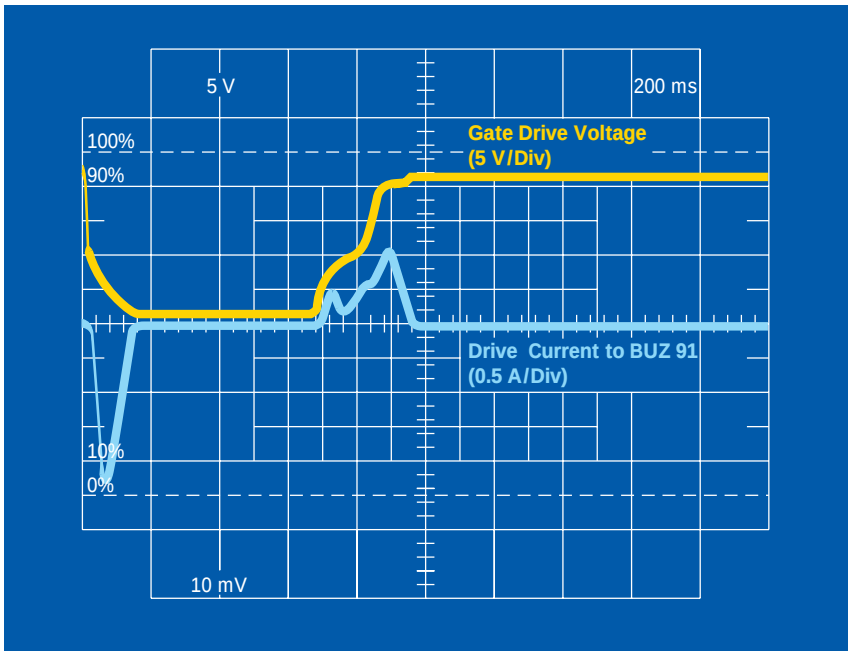
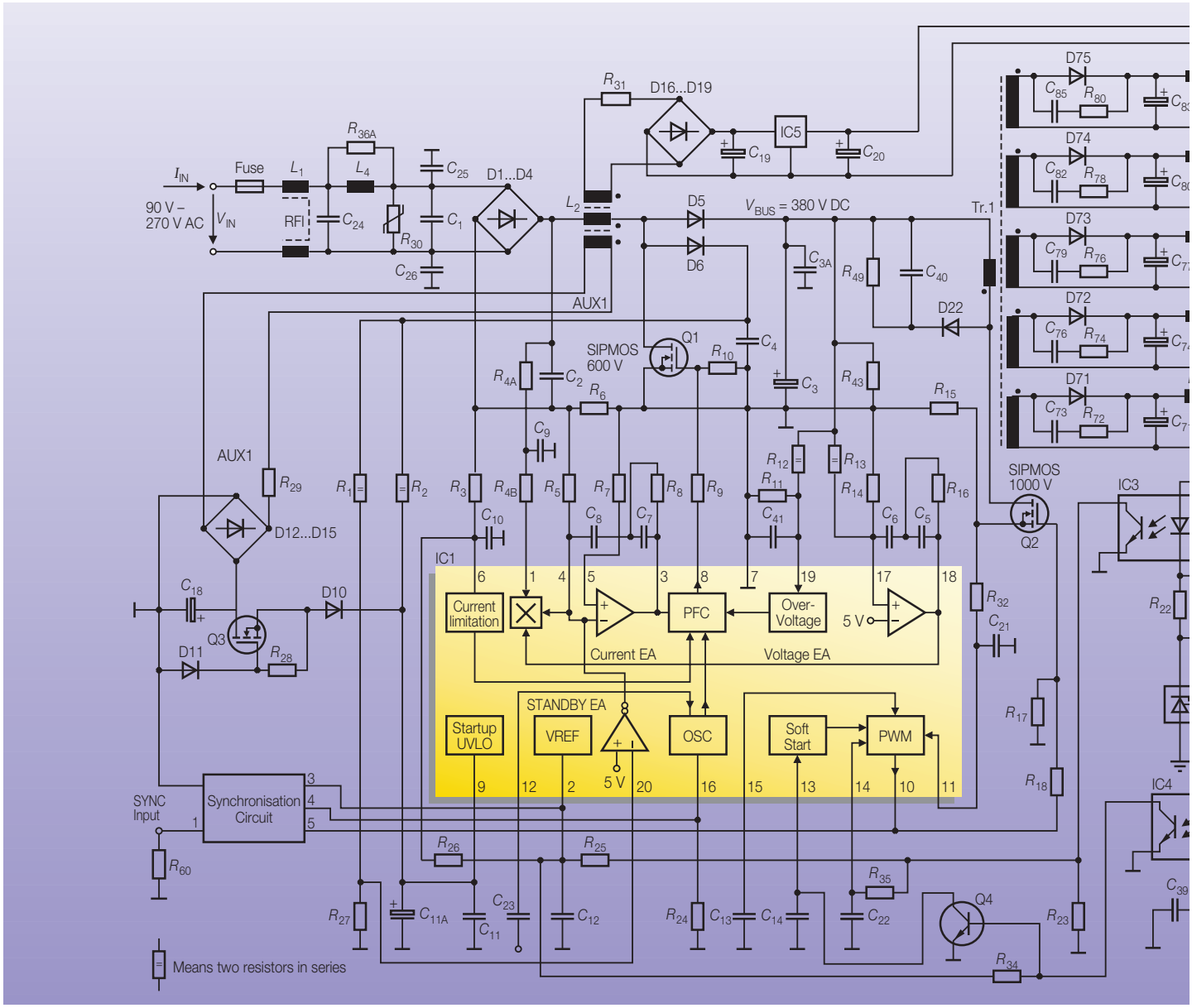


Figure 8 Gate Drive Signals



There is a synchronisation input Pin 12. A high level signal (3.5 V - 7.5 V) discharges the internal oscillator capacitor. Correspondingly a low level signal (below 0.4 V) enables the charging with the set current (R_{24}).
The internal oscillator can be completely superimposed by an external synchronisation signal. However the influence on the internal ramp voltages has to be taken into account.

For a synchronisation over a wide frequency range the variation of the set current at Pin 16 is to be preferred. For a synchronisation, which will alter the set frequency up to 20% the synchronisation input may be the better choice.

Example for External Synchronisation:

Synchronisation of the Combi-IC TDA 16888 to a Reference Frequency by a Phase-Locked Loop (PLL)

The switching frequency of the Power Factor- and PWM controller TDA 16888 may be synchronized to a reference frequency e.g. of a CRT monitor by using the standard PLL-CMOS-IC 4046.

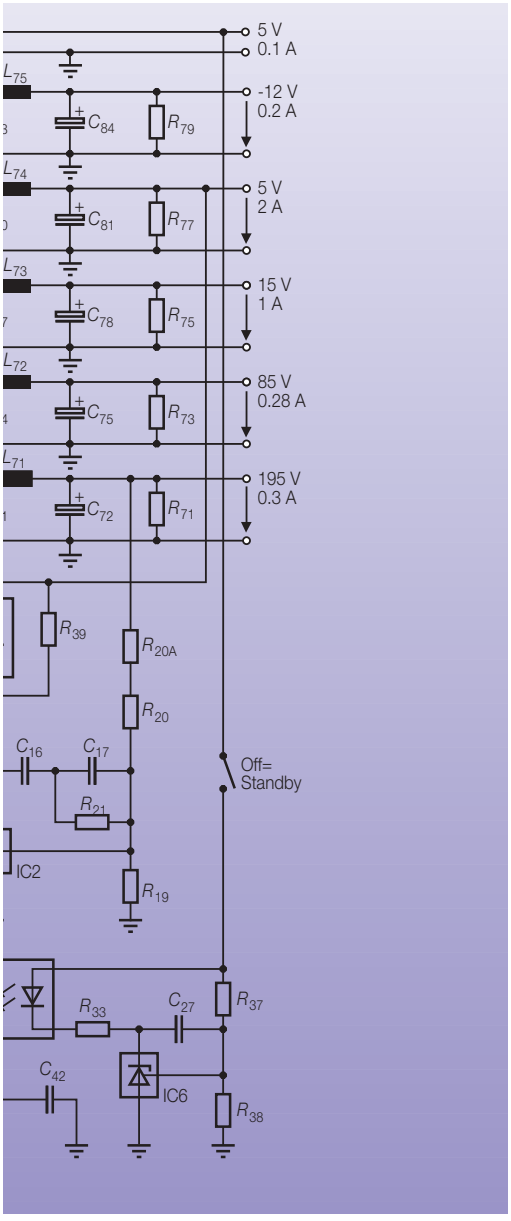


Figure 9 Application Circuitry

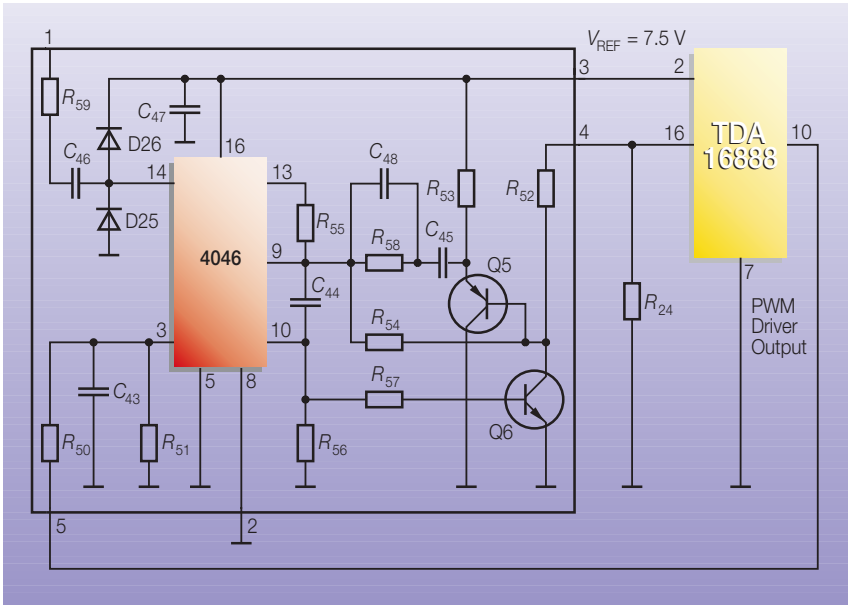


Figure 10 Synchronisation Circuitry of TDA 16888 with PLL

This device is supplied by the 7.5 V reference output V_{REF} (Pin 2) of the TDA 16888. Generally the 4046 controls the output current of Pin 16, which allows to set-up the switching frequency by the internal oscillator.

The PWM output signal at Pin 10 is fed back via a voltage divider (R_{50}, R_{51}) to Pin 3 of the 4046. Pin 14 of the 4046 is the input of the given reference frequency signal, fed from a separate winding on the deflection transformer, and compared internally by using phase comparator II.

The level of the phase comparator II output signal (Pin 13) represents the phase difference between the PWM output and the reference signal. Pin 13 feeds a low pass filter to provide VCO IN (Pin 9) of the 4046 with the average of the phase difference value. The VCO is not used, but the signal is amplified by the internal source follower.

The DEM OUT (Pin 10) controls the base current of Q6 and in this way the oscillator of the TDA 16888. R_{24} and R_{52} set the minimum and maximum limits of the frequency (adjusted to approximately 30 kHz and 120 kHz respectively).

The phase comparator II output signal at Pin 13 is filtered by R_{55} and C_{44} and fed into the VCO input at Pin 9. In addition a dynamic feedback from collector of Q6 is fed into Pin 9 via Q5 and its network. The capacitors C_{43} and C_{47} bypass high frequent currents. The response time of the phase locked loop is less than 10 ms. If there are some PWM output pulses missing, the oscillator frequency runs towards its maximum. If trigger pulses of the reference frequency are missing, the oscillator frequency decreases to the minimum set value.

The design works independent of the duty cycle of the PWM output signal, as long as its level is high enough to be realized as 'high' by the CMOS-IC.
The PLL frequency lock range and capture range are determined by R_{24} and R_{52}.