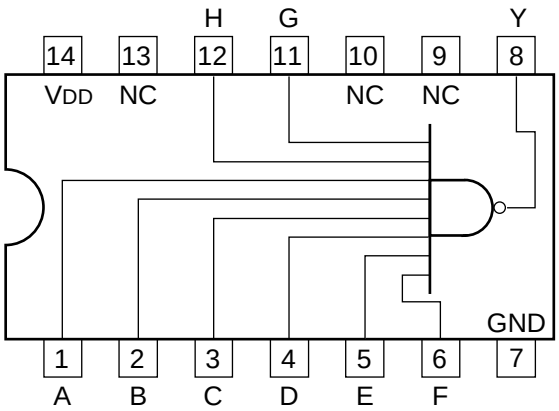
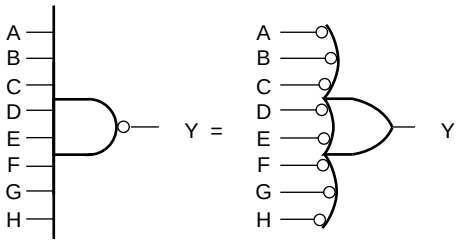
C-MOS 8-INPUT POSITIVE-NAND GATE

—TOP VIEW—





$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$
$$= \overline{A} + \overline{B} + \overline{C} + \text{- - - -} + \overline{H}$$