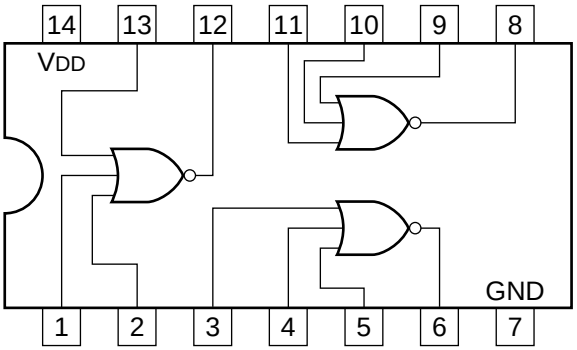
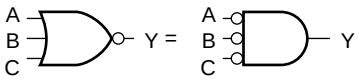
C-MOS 3-LINE POSITIVE-NOR GATE

—TOP VIEW—





$$Y = \overline{A + B + C} = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL