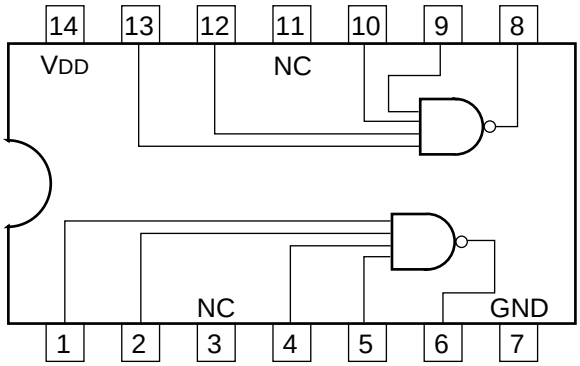
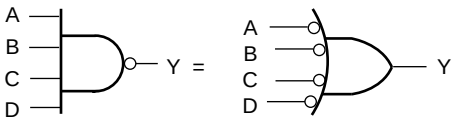
C-MOS 4-INPUT POSITIVE-NAND GATE

—TOP VIEW—





$Y = \overline{A \bullet B \bullet C \bullet D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
⋮	⋮	⋮	⋮	⋮
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL