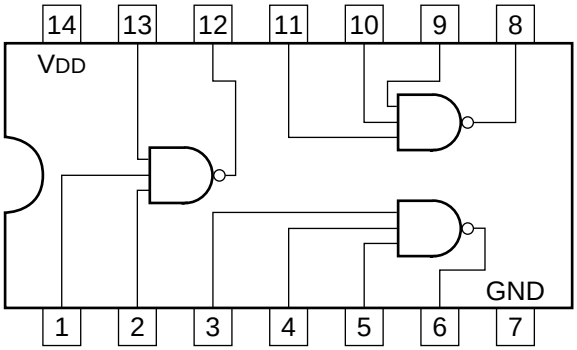
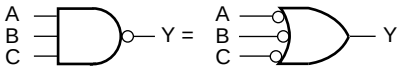
C-MOS 3-INPUT NAND GATE

—TOP VIEW—





$$Y = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL