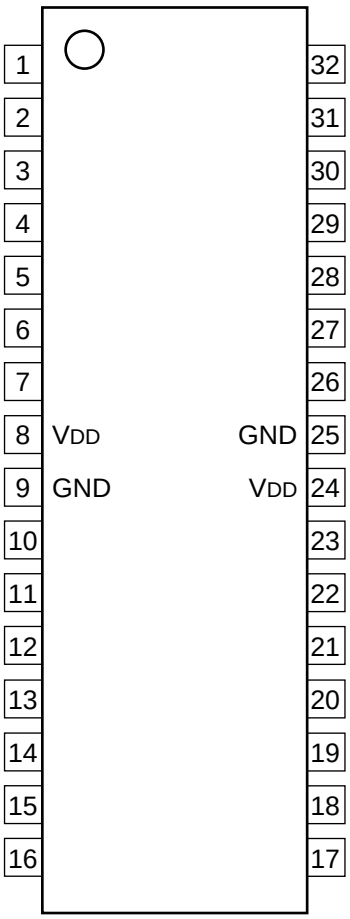
C-MOS 4 M (4,194,304 × 1/1,048,576 × 4)-BIT SRAM

—TOP VIEW—



INPUT

A0 - A21 : ADDRESS
B1/B4 : BIT TERMINAL
$\overline{CE}$: CHIP ENABLE
D : DATA
$\overline{OE}$: OUTPUT ENABLE
$\overline{WE}$: WRITE ENABLE

OUTPUT (×1 MODE ONLY)

Q : DATA

INPUT/OUTPUT

I/O1 - I/O4 : DATA

< × 1 MODE >

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	A0	17	I	B1/B4
2	I	A1	18	I	A11
3	I	A2	19	I	A12
4	I	A3	20	I	A13
5	I	A4	21	I	A14
6	I	A5	22	I	A15
7	I	$\overline{CE}$	23	O	Q
8	—	VDD	24	—	VDD
9	—	GND	25	—	GND
10	I	D	26	I	$\overline{OE}$
11	I	$\overline{WE}$	27	I	A16
12	I	A6	28	I	A17
13	I	A7	29	I	A18
14	I	A8	30	I	A19
15	I	A9	31	I	A20
16	I	A10	32	I	A21

< × 4 MODE >

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	A0	17	I	B1/B4
2	I	A1	18	I	A10
3	I	A2	19	I	A11
4	I	A3	20	I	A12
5	I	A4	21	I	A13
6	I	$\overline{CE}$	22	I	A14
7	I/O	I/O1	23	I/O	I/O3
8	—	VDD	24	—	VDD
9	—	GND	25	—	GND
10	I/O	I/O2	26	I/O	I/O4
11	I	$\overline{WE}$	27	I	$\overline{OE}$
12	I	A5	28	I	A15
13	I	A6	29	I	A16
14	I	A7	30	I	A17
15	I	A8	31	I	A18
16	I	A9	32	I	A19