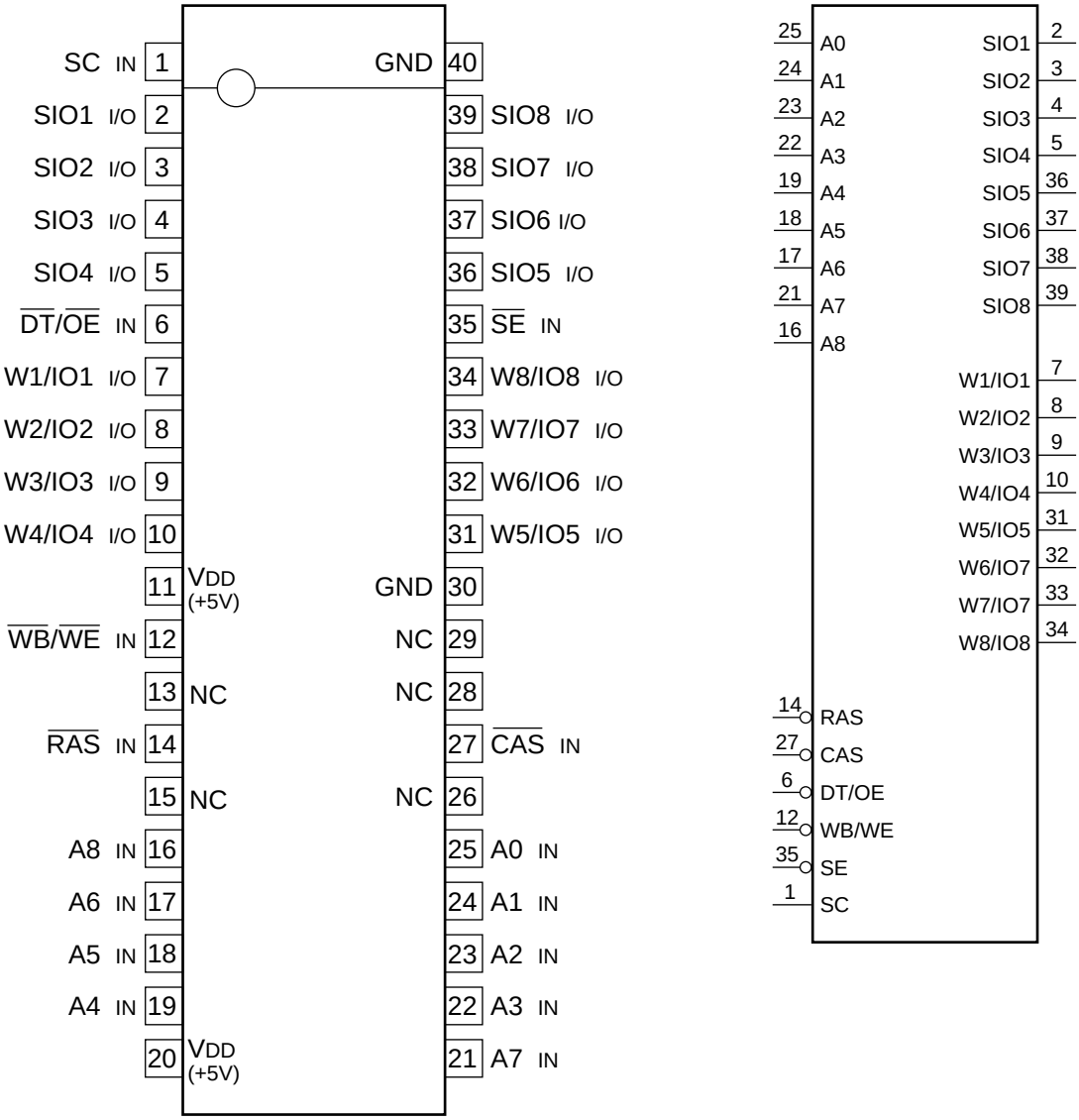
C-MOS 1M (131,072 × 8)-BIT MULTI PORT DYNAMIC RAM

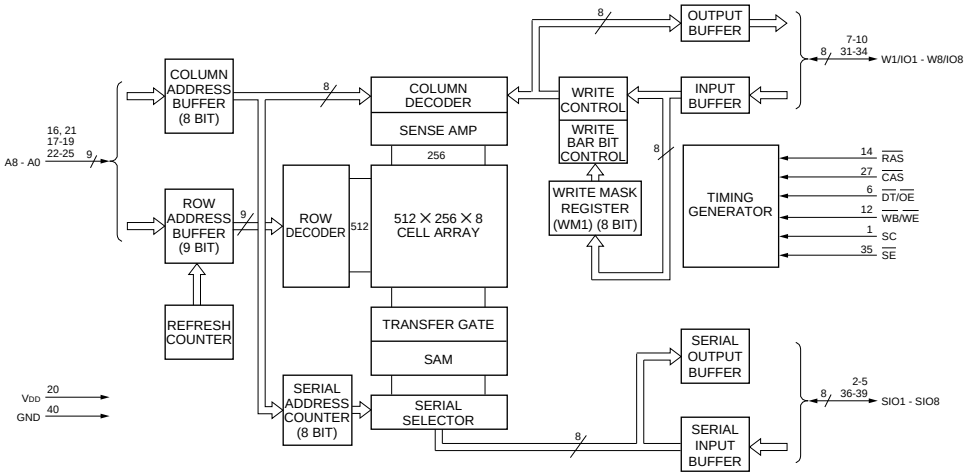
-TOP VIEW-



$\overline{A0}$ - $\overline{A8}$	;	ADDRESS INPUTS
$\overline{CAS}$	;	COLUMN ADDRESS STROBE INPUT
$\overline{DT/OE}$	;	DATA TRANSFER INPUT/OUTPUT ENABLE INPUT
$\overline{RAS}$	;	ROW ADDRESS STROBE INPUT
$\overline{SC}$	;	SERIAL CLOCK INPUT
$\overline{SE}$	;	SERIAL ENABLE INPUT
SIO1 - SIO8	;	SERIAL DATA INPUTS/OUTPUTS
$\overline{W1/IO1}$ - W8/IO8	;	WRITE MASK/DATA INPUTS/OUTPUTS
$\overline{WB/WE}$	;	WRITE BAR BIT INPUT/WRITE ENABLE INPUT

FUNCTION	RAS↓				ADDRESS		W/IO		WRITE MASK
	CAS	DT/OE	WB/WE	SE	RAS↓	CAS↓	RAS↓	CAS↓ WE↓	WM1
CAS BEFORE RAS REFRESH CYCLE	0	×	×	×	×	—	×	—	—
WRITE TRANSFER	1	0	0	0	ROW	TAP	×	×	—
ARTICIAL WRITE TRANSFER	1	0	0	1	ROW	TAP	×	×	—
READ TRANSFER	1	0	1	×	ROW	TAP	×	×	—
WRITE BAR BIT CYCLE	1	1	0	×	ROW	COLUMN	WM1	DIN	ROAD USE
READ/WRITE CYCLE	1	1	1	×	ROW	COLUMN	×	DIN	—

TAP ; SERIAL ACCESS MEMORY START ADDRESS
× ; DON'T CARE
0 ; LOW LEVEL
1 ; HIGH LEVEL
— ; NOT USE


OUTPUT BUFFER
8
7-10
31-34
8
W1/IO1 - W8/IO8
COLUMN ADDRESS BUFFER (8 BIT)
8
COLUMN DECODER
SENSE AMP
256
WRITE CONTROL
INPUT BUFFER
WRITE BAR BIT CONTROL
8
16, 21
17-19
22-25
A8 - A0
9
ROW ADDRESS BUFFER (9 BIT)
9
ROW DECODER
512
512 X 256 X 8 CELL ARRAY
WRITE MASK REGISTER (WM1) (8 BIT)
TIMING GENERATOR
14
RAS
27
CAS
6
DT/OE
12
WB/WE
1
SC
35
SE
REFRESH COUNTER
TRANSFER GATE
SAM
SERIAL OUTPUT BUFFER
VDD
20
GND
40
SERIAL ADDRESS COUNTER (8 BIT)
SERIAL SELECTOR
8
SERIAL INPUT BUFFER
2-5
36-39
8
SIO1 - SIO8