MC92100
Graphics Display Engine

Product Brief

MC92100 "Scorpion"

Graphics Display Generator, SDRAM Controller, and Digital Video Encoder

The Scorpion chip (MC92100) is a graphics display generator and NTSC/PAL digital video encoder for analog and digital video systems including Digital Versatile Disk (DVD), Set-Top Box (STB), and Internet TV applications. The display architecture has been designed to provide a high-quality television-oriented graphics overlay. The graphics overlay matches the resolution and color depth of the NTSC/PAL baseband video and reduces external memory usage. The MC92100 can provide generation of true color graphics, mixing of video and graphics, and control and display on four image layers. The MC92100 is controlled by high-level language instructions from a host processor (PowerPC™ or ColdFire™).

The MC92100 digital video encoder accepts a ITU-R-656 data stream with embedded synchronization codes or it may be genlocked with a television horizontal flyback and vertical synchronization signal. The MC92100 supports both a composite and separate luma and chroma output (S-VHS) analog video generation, or composite and RGB. It also includes Macrovision™ generation for copy protection and a closed caption inserter.

KEY FEATURES

- Graphics controller compatible with high-level languages
- True color graphics generator at VGA density with video/graphics mixing in 1.6% steps (64 levels)
- True color graphics generator for NTSC (720 x 480 pixels) and PAL (720 x 576 pixels)
- Selectable conversion from ITU-R-656 aspect ratio to square pixels
- Graphics overlay matched to resolution and color depth of high-quality NTSC/PAL
- Supports multiple storage/image formats:
  - 16 bits per pixel to store images equivalent to 24 bit computer images (4,2,2)
  - 16 bit RGB (5,6,5 and 5,5,5)
  - 2/4/8-bit Color Look-Up Table (CLUT)
- Maximum of two viewports on any horizontal lin
- Multiple viewports vertically
- Digital video encoder for converting ITU-R-656 to composite and S-VHS analog video
- Host processor interface for PowerPC and ColdFire
- SDRAM controller for shared system and graphics memory with glueless interface

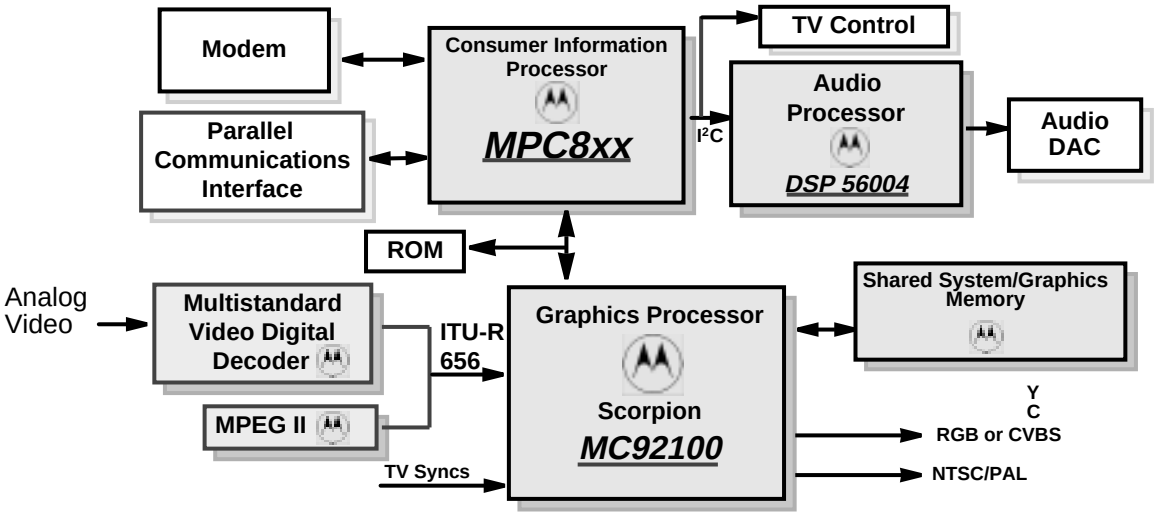

Figure 1. Typical Intelligent TV Block Diagram

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Specifications and information herein are subject to change without notice.

MC92100 Overview	
Features	**System Advantages**
True color graphics generator at VGA densities with video/graphics dedicated mixing in 1.6% steps (64 levels)	Allows smooth fading in & out for superior high resolution graphics on TV, special effects, and video viewing through graphics
Selectable conversion from ITU-R- 656 aspect ratio to square pixels	Shows computer graphic images with correct aspect ratio on a TV. Maximizes viewable graphics area.
Selectable vertical flicker filtering	Flicker reduction of non-interlaced image on a TV (interlaced)
Uses 16 bits per pixel to store images equivalent to 24-bit-per-pixel computer images (4,2,2)	High graphics resolution stored in 66% of the memory space
Supports 16 bit RGB (5,6,5 and 5,5,5)	Support of RGB color space. Primary format for graphics and software.
Graphics display requires <40% of memory bandwidth	Allows rapid processor updates and reduces external memory requirements
Digital Video Encoder (DVE) for encoding or converting ITU-R-656 to composite and S-VHS analog video	Integrated for system cost reductions, performance improvements, direct interface to televisions
Macrovision generator and Closed Caption Inserter for line 21 data	Copy protection required for motion picture applications
Four different image layers - video, two viewports, cursor	Multiple vertical viewports and up to two viewports horizontally to display graphics over video
208 PQFP	Industry standard package for manufacturing compatibility

PRODUCT DESCRIPTION AND OVERVIEW

The MC92100 is composed of four major blocks as shown in Figure 2:

- Graphics display engine with square pixel and flicker filters
- Digital video encoder with Macrovision and closed caption blocks
- SDRAM controller
- Host processor interface

Graphics Display Engine

The display architecture (shown in Figure 3) is designed to provide a high-quality television-oriented graphics overlay while minimizing system cost. The graphics are designed to match the resolution and color depth of NTSC/PAL baseband video, without adding memory to hold computer-resolution images. The close connection between the display engine and the display memory minimizes cycle losses and simplifies the future addition of graphics acceleration hardware to scale up performance.

The computer-format images are stored in either of two formats:

- RGB16 (5,6,5), red 5 bits, green 6 bits, blue 5 bits and RGB16 (5,5,5), red 5 bits, green 5 bits, blue 5 bits with the MSB being the transparency bit.
- YCrCb at 4:2:2, yielding 16 bits per pixel or 2/4/8 bits per pixel converted to YCrCb from a color look-up table.

Images with a display equivalent to a 24-bit-per-pixel computer image are stored using only 16 bits per pixel. Memory is also flexibly allocated so that no more memory is used than the amount required for the image currently being displayed.

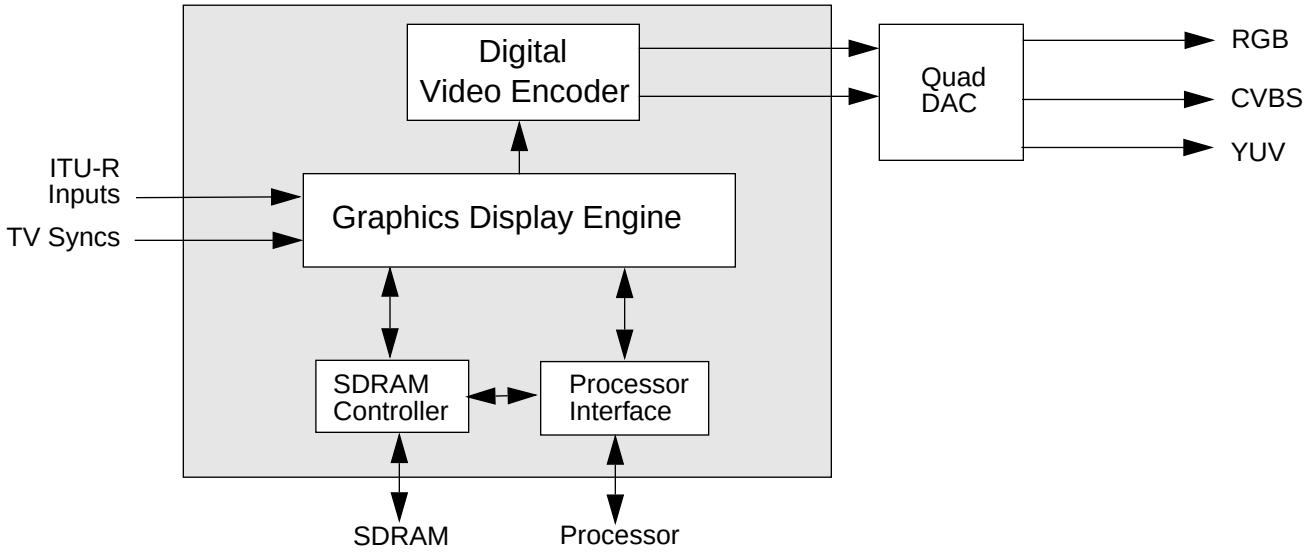

Figure 2. MC92100 Block Diagram

The MC92100 supports four image layers. At the bottom is the video; above that are two viewports; and on top is the cursor. The top three layers are individually controlled. The two viewports can be mixed at 64 levels and the result can be mixed with the video at 64 levels. A hardware cursor is provided. These features allow for powerful control over mixing video and graphics, which can be combined in 63 levels. The mix percentage is set for each pixel or pixel group.

Two independently-selectable vertical filters provide flicker reduction and pixel squaring. If graphics images have been generated on a computer, the filter reduces,with minimal impact on the image, any flicker introduced by switching from non-interlaced to interlaced scan. Square pixel images are also shown in true aspect ratio, maximizing the amount of information on the screen. The processor can turn both filters off for images prepared specifically for television, enabling the image to be displayed exactly as intended.

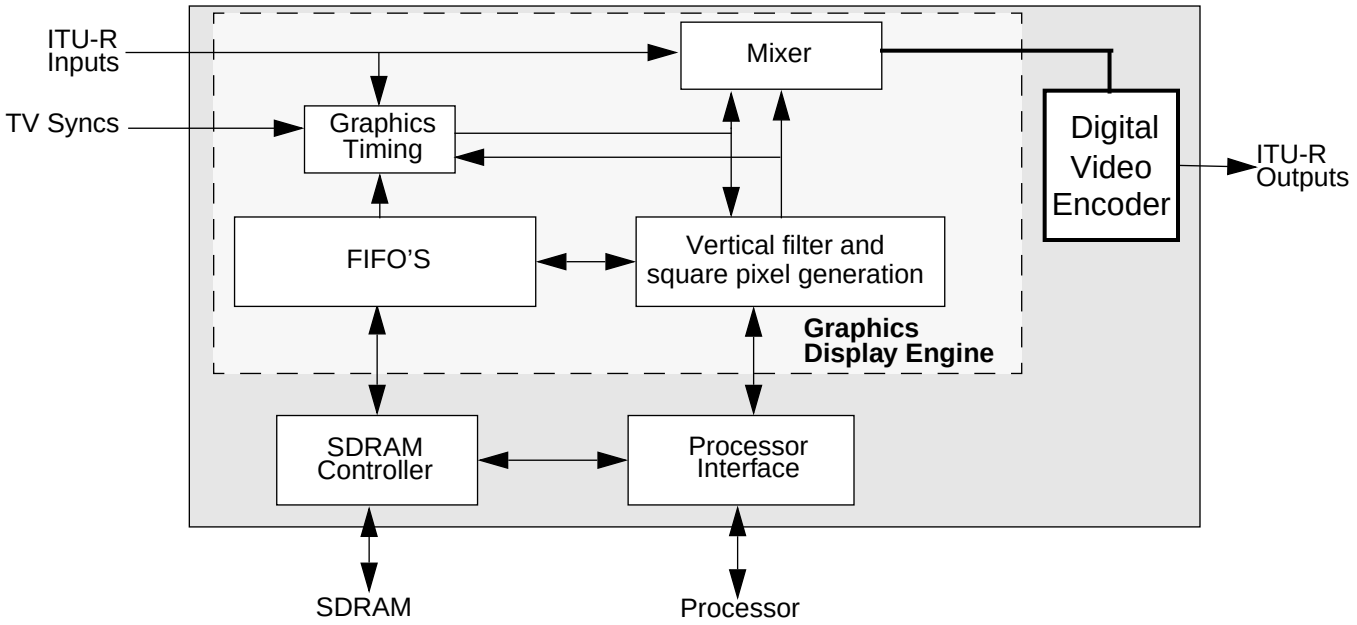

Figure 3. Graphics Display Engine

Digital Video Encoder (DVE)

The digital video encoder (in Figure 4) accepts a ITU-R-656 data stream at 27 MHz with embedded synchronization codes. This data stream and the associated clock can come from either of two sources which are controlled by two output enable lines from the DVE section. If both sources are used, each needs to be tri-stateable and able to present its data and clock when the enable signal is low. The data is separated into its YCrCb components and passed to the mixer, which is controlled by the graphics section.

The DVE's timer module generates all the master timing for regeneration of the synchronization and active video reconstruction. The timer module also supplies this information to the graphics section for genlocking the graphics to the video. The luma path has the synchronization, closed caption and Macrovision data inserted. The chroma path is low-pass filtered to 1.3 MHz and digitally modulated onto the PAL or NTSC color carrier. The two paths are then sent through an interpolation sinx/x filter to increase the data rate to 27 MHz and to match the D/A characteristics.

These signals are brought out through separate D/A converters to produce the S-VHS signals. In order to produce the composite video, the signals are digitally added and then sent to the composite D/A converter.

Externally, each of the D/A outputs requires a low-pass filter. This filter consists of three 5% capacitors and one 10% inductor. The resulting video signals are targeted to be within plus or minus 0.3 db up to 5.5 MHz and are below -40 db at 8.5 MHz and above.

Closed Captioning

Closed caption data can be inserted on line 21 of both the even and odd fields. There are two 16-bit registers, one for the even and one for the odd field data. After the two bytes of data are stored in the register, they are inserted into line 21 in its respective field and a status bit is set for this field to indicate that the register can accept new data. If data is not available at the line 21 time, null bytes are inserted. If closed captioning is not enabled, line 21 is transparent to the video data which could contain closed captioning data inserted at the video source.

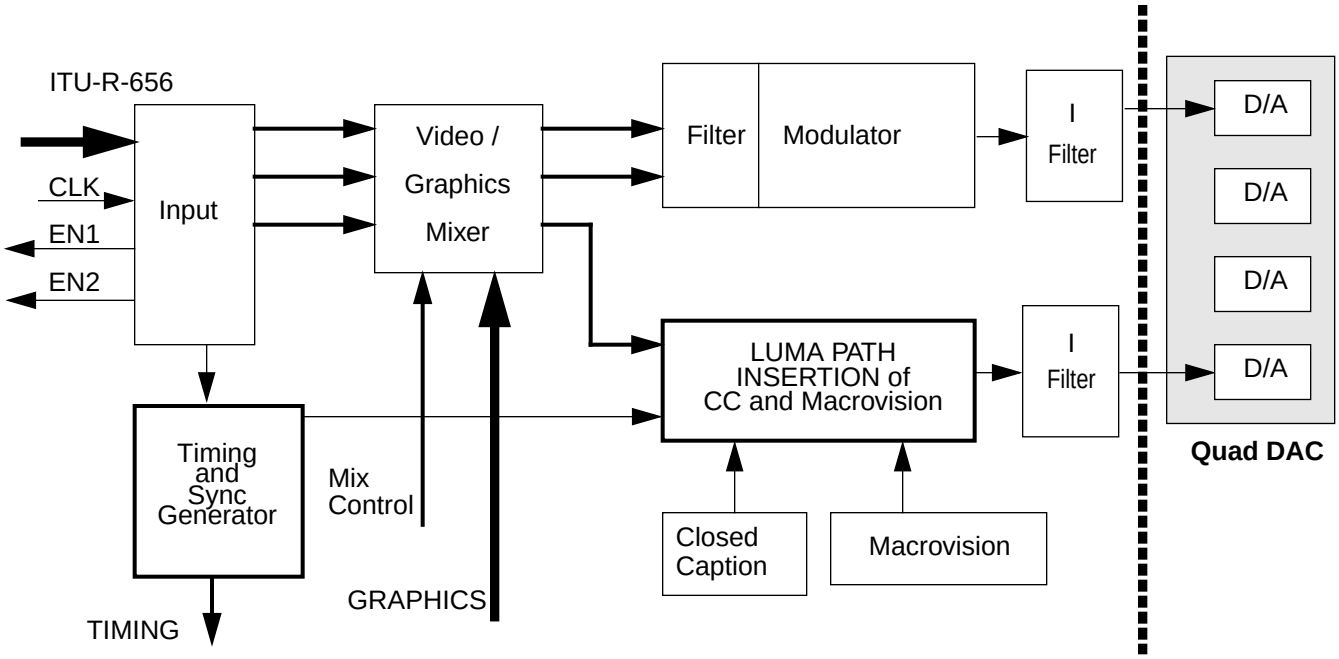

Figure 4. MC92100 Digital Video Encoder

Macrovision

Macrovision copy protection can be enabled in both PAL and NTSC modes. Macrovision conforms to the version 7 standard..

Processor Interface

The MC92100 has a processor interface that supports both the PowerPC (8XX series) and ColdFire microprocessor architectures.

MPC860/801 (PowerPC) Interface

The MC92100 is accessible to the processor through two chip selects: one for the control registers and one for the SDRAM. The PowerPC MPC860/801 interface is used to access both the MC92100 registers and the SDRAM. The port size on the MPC801 must be configured as 32 bits. Total address page size supported is 4 Mbytes (22 address lines) since the MC92100 uses two 16-Mbit SDRAMs for 4 Mbytes of total storage.

Note that there is a response time associated with the memory access due to the way the SDRAM is used. Processor accesses have a lower priority than graphics accesses to the SDRAM. When the processor is writing to the SDRAM, the data is fully buffered and the processor cycle is terminated quickly. A processor read access to SDRAM stalls the processor bus until the data is read from SDRAM by MC92100 and buffered for the processor.

Synchronous DRAM (SDRAM) Interface and Controller

The memory controller provides three key functions:

- Arbitrates between processor and display engine SDRAM accesses
- Makes the SDRAM space appear to the processor as a linear address space
- Handles SDRAM refresh

The system DRAM can be used by both the microprocessor and the graphics if the bandwidth of the memory is large enough. By utilizing SDRAM technology and organizing the system to interact with the memory in bursts (all graphics accesses are bursts of 8), the bandwidth left for the microprocessor under worst-case conditions is in excess of 60%.

The SDRAM interface supports 4 Mbytes (two 16-Mbit devices ($524{,}288 \times 16 \times 2$)) at a memory clock rate of 81 MHz with a memory data bus which is 32 bits in width. This can be extended as a user option. Memory clock is provided internally. The MC92100 performs all memory initialization, refresh, and access control.

The SDRAM controller arbitrates between graphics and processor accesses and services these accordingly. Under normal operating conditions, a graphics access

has priority over a processor access, but a processor access will not be delayed beyond one graphics access; hence, its access latency is low.

DAC Interface

Motorola offers a companion Quad DAC chip. The MC92100 interfaces with the Quad DAC chip using a 54 MHz interface bus with 18 outputs and a dual bank of registers. The registers multiplex the signals to the Quad DAC, which provides an output in RGB, YUV, or Baseband Video Format.

FUTURE ENHANCEMENTS

Picture Reduction—Picture in Graphics

The architecture allows for capture of video into the SDRAM, because the video received and the graphics generated are of the same format. This feature could decimate the video for a 1/2 PIP to a 1/16 PIP area and allow active video to be displayed in a smaller screen area while the graphics is displaying other information. This feature is not shown in the above diagrams.

Data Recovery in the VBI

Closed caption, 2X closed caption, and NABTS data recovery will be added.

Multi-Standard Video Digital Decoder

A digital decoder with a 2H adaptive comb filter is in development for future addition.

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