Ordering number : ENN6507

Thick-Film Hybrid IC

STK672-080

Stepping Motor Driver (Sine Wave Drive) Output Current: 2.8 A (No Heat Sink*)

Unipolar constant-current chopper (external excitation PWM) circuit with built-in microstepping controller

Overview

The STK672-080 is a stepping motor driver hybrid IC that uses power MOSFETs in the output stage. It includes a built-in microstepping controller and is based on a unipolar constant-current PWM system. The STK672-080 supports application simplification and standardization by providing a built-in 4 phase distribution stepping motor controller. It supports five excitation methods: 2 phase, 1-2 phase, W1-2 phase, 2W1-2 phase, and 4W1-2 phase excitations, and can provide control of the basic stepping angle of the stepping motor divided into 1/16 step units. It also allows the motor speed to be controlled with only a clock signal.

The use of this hybrid IC allows designers to implement systems that provide high motor torques, low vibration levels, low noise, fast response, and high-efficiency drive. Compared to the earlier SANYO STK672-050, the STK672-080 features a significantly smaller package for easier mounting in end products.

Applications

- Facsimile stepping motor drive (send and receive)
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X-Y plotter pen drive
- Industrial robots and other stepping motor applications

Features

- Can implement stepping motor drive systems simply by providing a DC power supply and a clock pulse generator.

<Control Block Features>

- One of five drive types can be selected with the drive mode settings (M1, M2, and M3)
  —2 phase excitation drive
  —1-2 phase excitation drive
  —W1-2 phase excitation drive
  —2W1-2 phase excitation drive
  —4W1-2 phase excitation drive
- Phase retention even if excitation is switched.
- The MOI phase origin monitor pin is provided.
- The CLK input counter block can be selected to be one of the following by the high/low setting of the M3 input pin.
  —Rising edge only
  —Both rising and falling edges

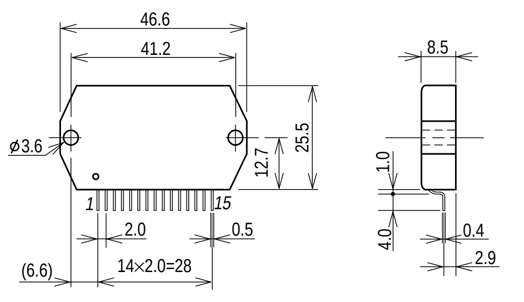
Note*: Conditions: $V_{CC}1$ = 24 V, I_{OH} = 2.0 A, 2W1-2 drive used.

Continued on next page.

Package Dimensions

unit: mm

4186



SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

- The CLK input pin include built-in malfunction prevention circuits for external pulse noise.
- ENABLE and $\overline{RESET}$ pins provided. These are Schmitt trigger inputs with built-in 20 kΩ (typical) pull-up resistors.
- No noise generation due to the difference between the A and B phase time constants during motor hold since external excitation is used.
- Microstepping operation supported even for small motor currents, since the reference voltage Vref can be set to any value between 0 V and 1/2 $V_{CC}2$.

<Driver Block>

- External excitation PWM drive allows a wide operating supply voltage range ($V_{CC}1$ = 10 to 45 V) to be used.
- Current detection resistor (0.15 Ω) built into the hybrid IC.
- Power MOSFETs for minimal driver loss
- Motor output drive currents I_{OH} up to 2.8 A (When Tc = 105°C).

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage1	$V_{CC}1$ max	No signal	52	V
Maximum supply voltage2	$V_{CC}2$ max	No signal	–0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	–0.3 to +7.0	V
Phase output current	I_{OH} max	0.5 seconds, single pulse, with $V_{CC}1$ applied.	3.3	A
Repeatable avalanche current	Ear max		30	mJ
Power loss	Pd max	θc-a = 0	8	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage1	$V_{CC}1$	With input signals present	10 to 45	V
Supply voltage2	$V_{CC}2$	With input signals present	5 ±5%	V
Input voltage	V_{IH}		0 to $V_{CC}2$	V
Phase driver voltage handling	V_{DSS}	Tr1, 2, 3, and 4 (the A, $\overline{A}$, B, and $\overline{B}$ outputs)	100 (min)	V
Phase current 1	I_{OH} 1	Tc = 105°C, CLK ≥ 200 Hz	2.8	A
Phase current 2	I_{OH} 2	Tc = 80°C, CLK ≥ 200 Hz	3	A

Electrical Characteristics at Tc = 25°C, $V_{CC}1$ = 24 V, $V_{CC}2$ = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Control supply current	I_{CC}	Pin 6 input, with ENABLE pin held low.		2.1	14	mA
Output saturation voltage	Vsat	R_L = 12 Ω		0.65	1	V
Average output current	Io ave	Load: R = 3.5 W/L = 3.8 mH per phase	0.445	0.5	0.56	A
FET diode Forward voltage	Vdf	If = 1 A		1	1.5	V
[Control Inputs]						
Input voltage	V_{IH}	Except for the Vref pin	4			V
	V_{IL}	Except for the Vref pin			1	V
Input current	I_{IH}	Except for the Vref pin	0	1	10	µA
	I_{IL}	Except for the Vref pin	125	250	510	µA
[Vref Input Pin]						
Input voltage	V_I	Pin 7	0		2.5	V
Input current	I_I	Pin 7, 2.5-V input	330	415	545	µA
[Control Outputs]						
Output voltage	V_{OH}	I = –3 mA, pin MOI	2.4			V
	V_{OL}	I = +3 mA, pin MOI			0.4	V

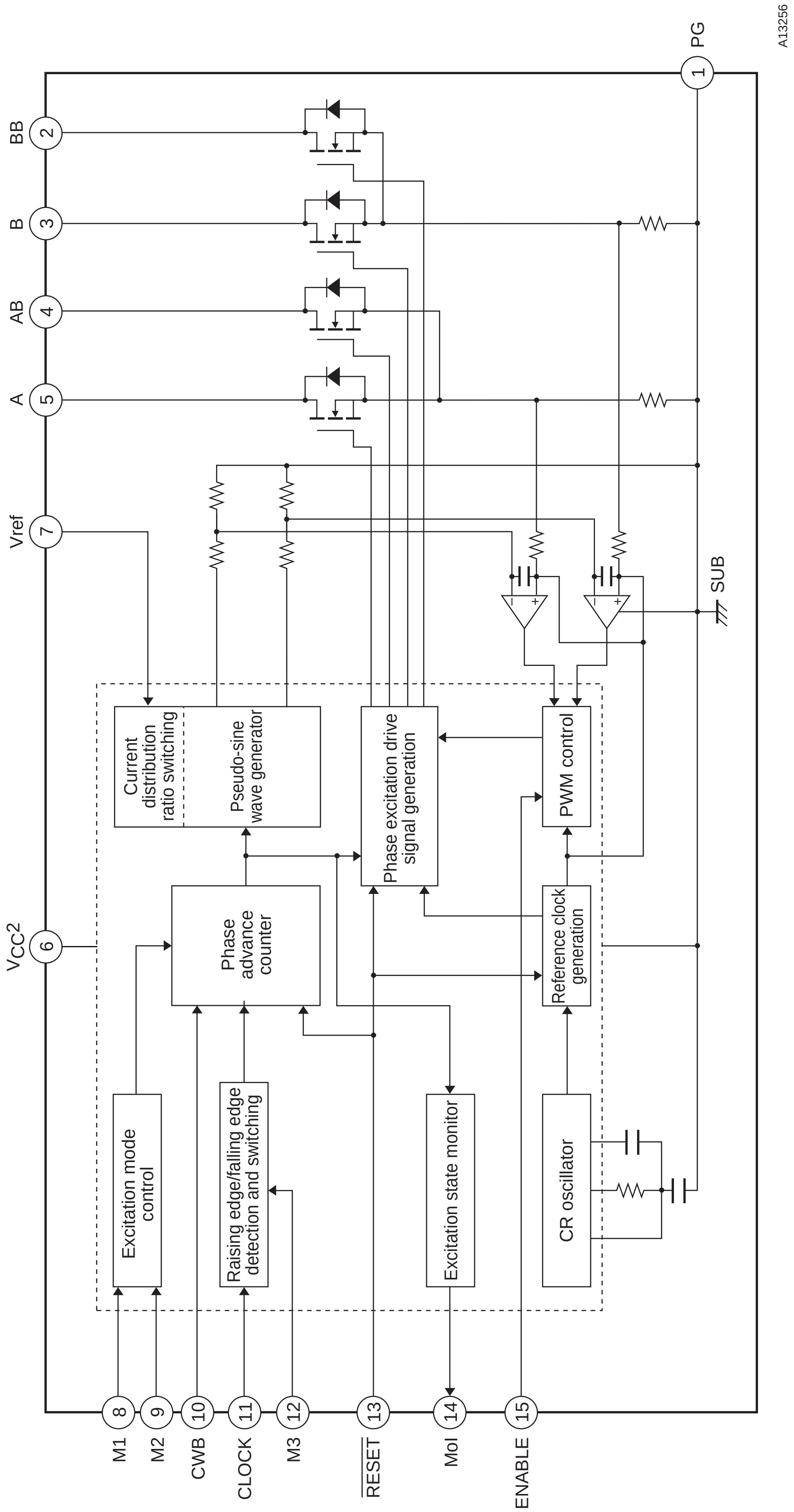
Continued on next page.

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current Distribution Ratio (A·B)]						
2W1-2, W1-2, 1-2	Vref	θ = 1/8		100		%
2W1-2, W1-2	Vref	θ = 2/8		92		%
2W1-2	Vref	θ = 3/8		83		%
2W1-2, W1-2, 1-2	Vref	θ = 4/8		71		%
2W1-2	Vref	θ = 5/8		55		%
2W1-2, W1-2	Vref	θ = 6/8		40		%
2W1-2	Vref	θ = 7/8		21		%
2	Vref			100		%
PWM frequency	fc		37	47	57	kHz

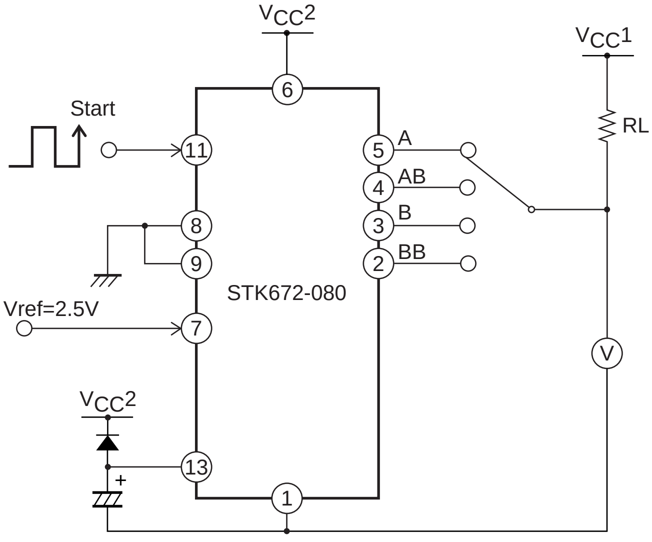
Note: A constant-voltage power supply must be used.
The design target value is shown for the current distribution ratio.

Internal Block Diagram



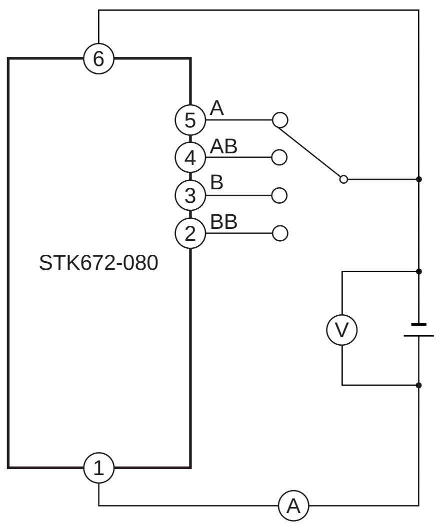
Test Circuit Diagrams

Vsat



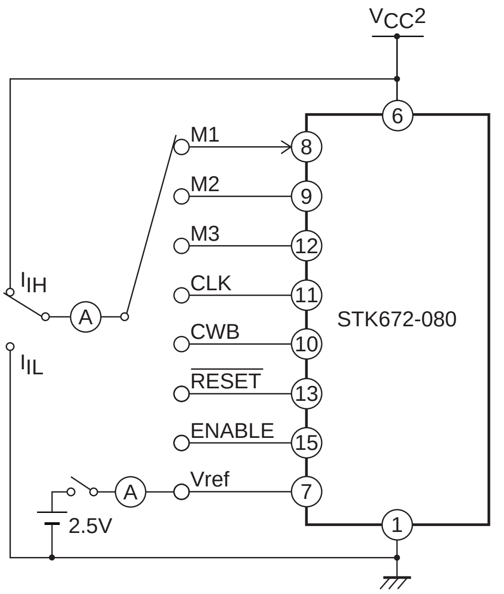
A13257

Vdf



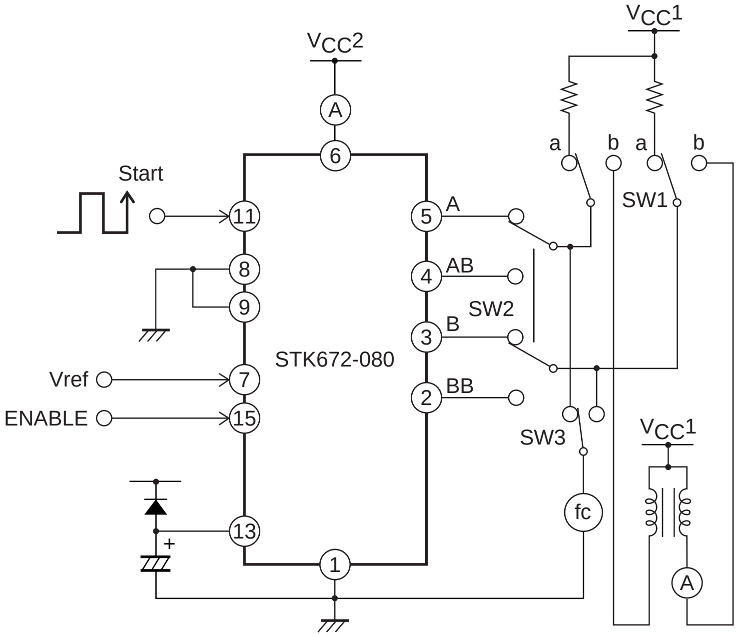
A13258

I_{IH}, I_{IL}



A13259

Ioave, Icc, fc

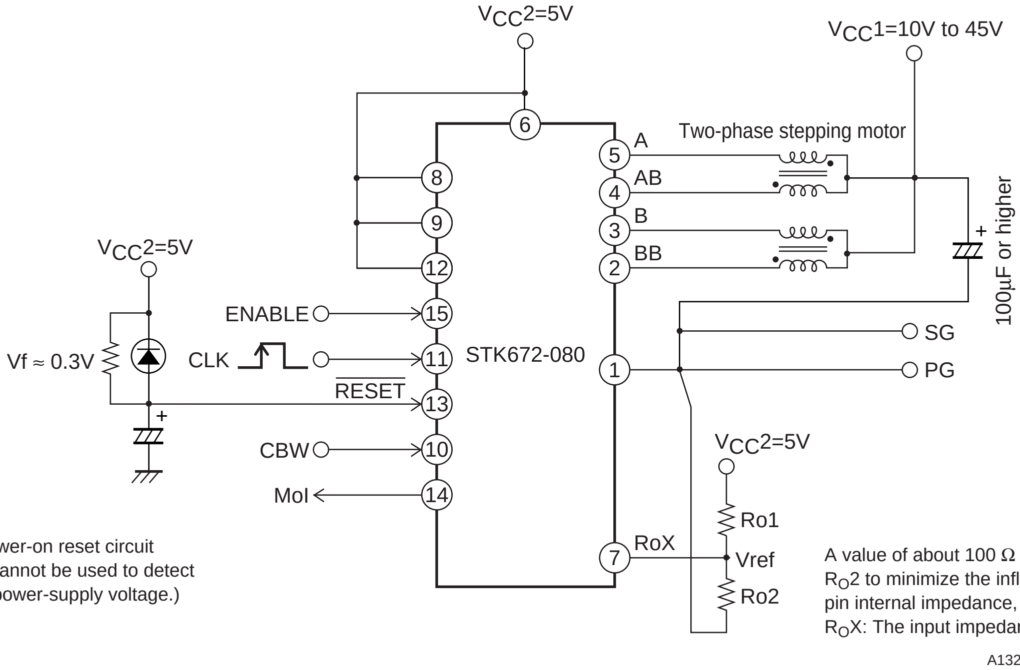


A13260

To measuring Io ave: With SW1 set to the b position, input Vref and switch SW2.
To measuring fc: With SW1 set to the a position, set Vref to 0 V, and switch SW3.
To measuring Icc: Set the ENABLE pin low.

Functional Description

2W1-2 Phase Excitation Drive (microstepping operation)



Simplified power-on reset circuit
(This circuit cannot be used to detect drops in the power-supply voltage.)

A value of about 100 Ω is recommended for R_O2 to minimize the influence of the Vref pin internal impedance, which is 6 kΩ.
R_OX: The input impedance is 6 kΩ ±30%.

Always perform a power-on reset operation when the $V_{CC}2$ supply voltage is first applied to this hybrid IC.

[Setting the Motor Current]

The motor current I_{OH} is set by the Vref voltage on the hybrid IC pin 7. The following formula gives the relationship between I_{OH} and Vref.

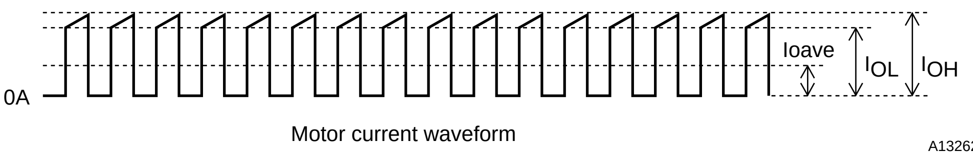
$R_OX = (R_O2 \times 6\ k\Omega) \div (R_O2 + 6\ k\Omega)$ ·········(1)

$Vref = V_{CC}2 \times R_OX \div (R_O1 + R_OX)$ ·········(2)

$I_{OH} = \frac{1}{k} \times \frac{Vref}{R_S}$ ·········(3)

K: 4.7 (Voltage division ratio), Rs: 0.15 Ω (The hybrid IC's internal current detection resistor (precision: ±3%)

Applications can use motor currents from the current (0.05 to 0.1 A) set by the duty of the frequency set by the oscillator up to the limit of the allowable operating range, I_{OH} = 2.8 A



Motor current waveform

[Function Table]

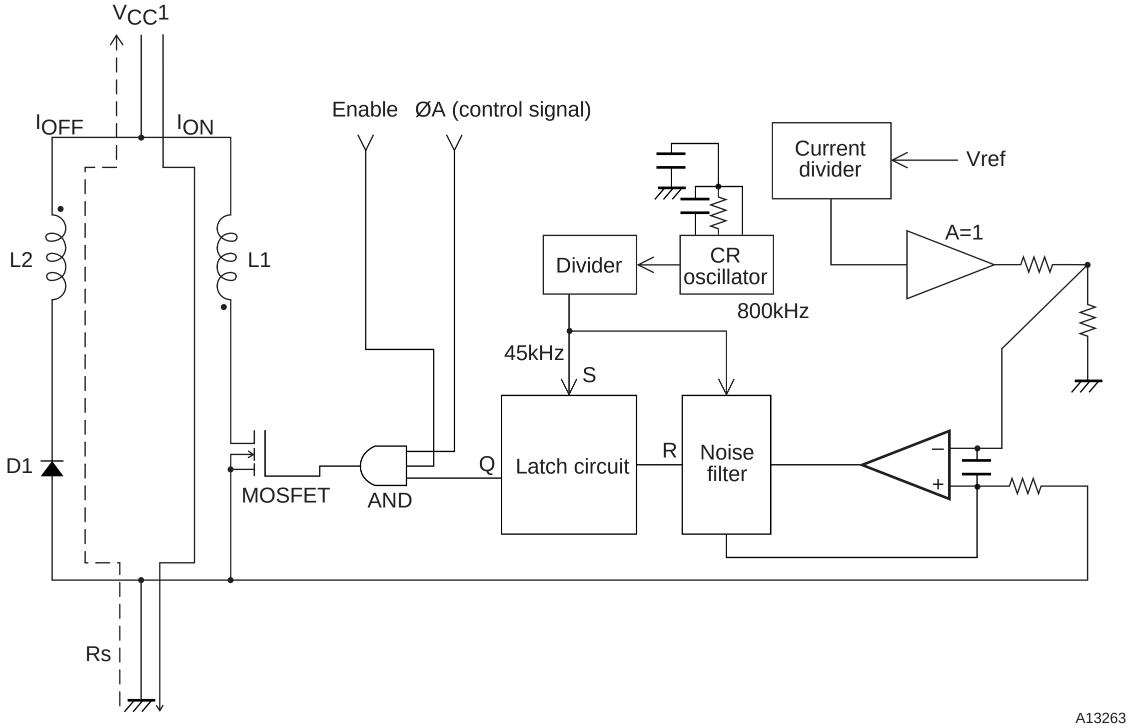
M2	0	0	1	1	Phase switching clock edge timing
M3 \ M1	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges

	Forward	Reverse
CWB	0	1

ENABLE	Motor current is cut off when low
RESET	Active low

Functional Description

External Excitation Chopper Drive Block Description



Driver Block Basic Circuit Structure

Since this hybrid IC adopts an external excitation method, no external oscillator circuit is required.
When a high level is input to øA in the basic driver block circuit shown in the figure and the MOSFET is turned on, the comparator + input will go low and the comparator output will go low. Since a set signal with the PWM period will be input, the Q output will go high, and the MOSFET will be turned on as its initial value.
The current I_{ON} flowing in the MOSFET passes through L1 and generates a potential difference in Rs. Then, when the Rs potential and the Vref potential become the same, the comparator output will invert, and the reset signal Q output will invert to the low level. Then, the MOSFET will be turned off and the energy stored in L1 will be induced in L2 and the current I_{OFF} will be regenerated to the power supply. This state will be maintained until the time when an input to the latch circuit set pin occurs.
In this manner, the Q output is turned off and on repeatedly by the reset and set signals, thus implementing constant current control. The resistor and capacitor on the comparator input are spike removal circuit elements and synchronize with the PWM frequency. Since this hybrid IC uses a fixed frequency due to the external excitation method and at the same time also adopts a synchronized PWM technique, it can suppress the noise associated with holding a position when the motor is locked.

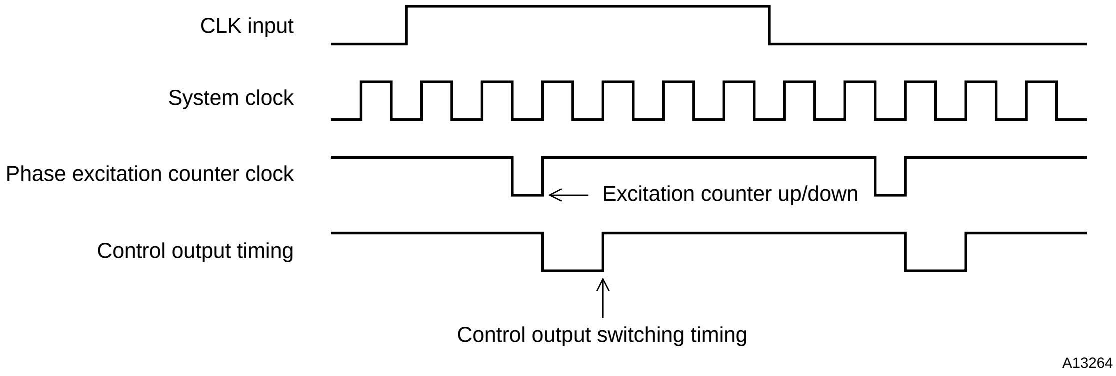
Input Pin Functions

Pin No.	Symbol	Function	Pin circuit type
11	CLK	Phase switching clock	Built-in pull-up resistor CMOS Schmitt trigger input
10	CWB	Rotation direction setting (CW/CCW)	Built-in pull-up resistor CMOS Schmitt trigger input
15	ENABLE	Output cutoff	Built-in pull-up resistor CMOS Schmitt trigger input
8, 9, 12	M1, M2, M3	Excitation mode setting	Built-in pull-up resistor CMOS Schmitt trigger input
13	$\overline{\text{RESET}}$	System reset	Built-in pull-up resistor CMOS Schmitt trigger input
7	Vref	Current setting	Input impedance 6 kΩ (typ.) ±30%

Input Signal Functions and Timing

- CLK (phase switching clock)
  Input frequency range: DC to 50 kHz
  Minimum pulse width: 10 μs
  Duty: 40 to 60% (However, the minimum pulse width takes precedence when M3 is high.)
  Pin circuit type: Built-in pull-up resistor (20 kΩ, typical) CMOS Schmitt trigger structure
  Built-in multi-stage noise rejection circuit
  Function
  —When M3 is high or open: The phase excited (driven) is advanced one step on each CLK rising edge.
  —When M3 is low: The phase moves on both the rising and falling edges of the CLK signal, for a total of two steps per cycle.

CLK Input Acquisition Timing (M3 = Low)



- CWB (Method for setting the rotation direction)
  Pin circuit type: Built-in pull-up resistor (20 kΩ, typical) CMOS Schmitt trigger structure
  Function
  —When CWB is high: The motor turns in the clockwise direction.
  —When CWB is low: The motor turns in the counterclockwise direction.
  Notes: When M3 is low, the CWB input must not be changed for about 6.25 μs before or after a rising or falling edge on the CLK input.

- ENABLE (Controls the on/off state of the A, $\overline{A}$, B, and $\overline{B}$ excitation drive outputs and selects either operating or hold as the internal state of this hybrid IC.)

Pin circuit type: Built-in pull-up resistor (20 kΩ, typical) CMOS Schmitt trigger structure
Function
—When ENABLE is high or open: Normal operating state
—When ENABLE is low: This hybrid IC goes to the hold state and excitation drive output (motor current) is forcibly turned off. In this mode, the hybrid IC system clock is stopped and no inputs other than the reset input have any effect on the hybrid IC state.

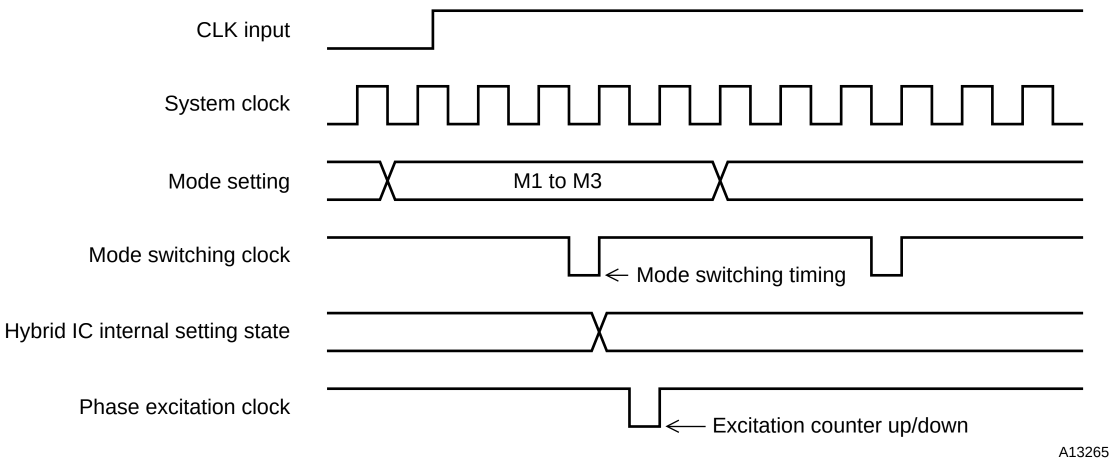
• M1, M2, and M3 (Excitation mode and CLK input edge timing selection)
Pin circuit type: Built-in pull-up resistor (20 kΩ, typical) CMOS Schmitt trigger structure

Function:

M2	0	0	1	1	Phase switching clock edge timing
M3 \ M1	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges

Valid mode setting timing: Applications must not change the mode in the period 5 µs before or after a CLK signal rising or falling edge.

Mode Setting Acquisition Timing



• $\overline{\text{RESET}}$ (Resets all parts of the system.)
Pin circuit type: Built-in pull-up resistor (20 kΩ, typical) CMOS Schmitt trigger structure
Function
—All circuit states are set to their initial values by setting the $\overline{\text{RESET}}$ pin low. (Note that the pulse width must be at least 10 µs.)
At this time, the A and $\overline{\text{B}}$ phases are set to their origin, regardless of the excitation mode. The output current goes to about 71% after the reset is released.
Notes: When power is first applied to this hybrid IC, Vref must be established by applying a reset. Applications must apply a power on reset when the $V_{CC}2$ power supply is first applied.

• Vref (Sets the current level used as the reference for constant-current detection.)
Pin circuit type: Analog input structure
Function
—Constant-current control can be applied to the motor excitation current at 100% of the rated current by applying a voltage less than the control system power supply voltage $V_{CC}2$ minus 2.5 V.
—Applications can apply constant-current control proportional to the Vref voltage, with this value of 2.5 V as the upper limit.

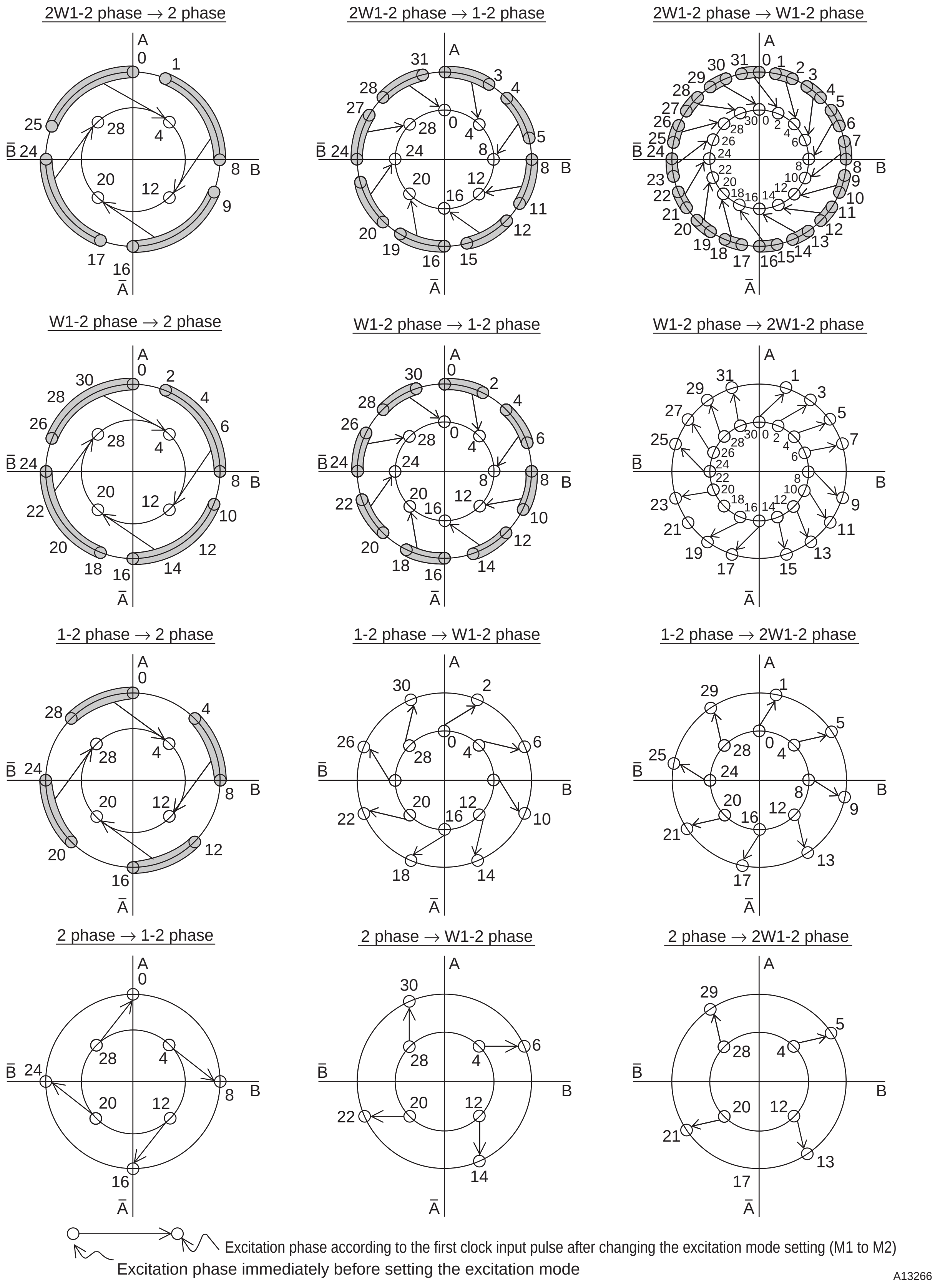
Output Pin Functions

Pin No.	Symbol	Function	Pin circuit type
14	MoI	Phase excitation monitor	Standard CMOS structure

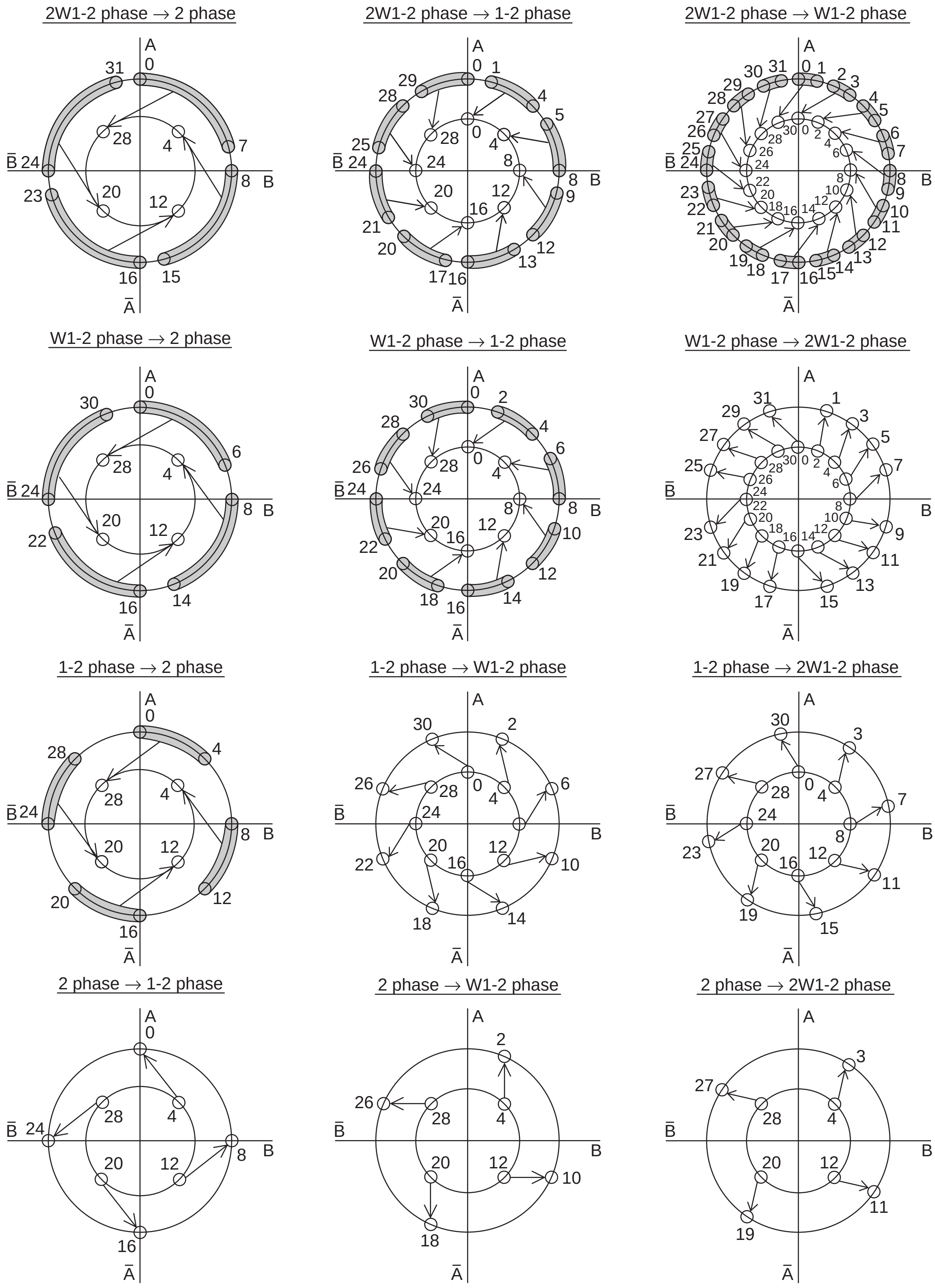
Output Signal Functions and Timing
• A, $\overline{\text{A}}$, B, and $\overline{\text{B}}$ (Motor phase excitation outputs)
Function
—In the 4 phase and 2 phase excitation modes, a 3.75 µs (typical) interval is set up between the A and $\overline{\text{A}}$ and B and $\overline{\text{B}}$ output signal transition times.

Phase States During Excitation Switching

• Excitation phases before and after excitation mode switching <clockwise direction>



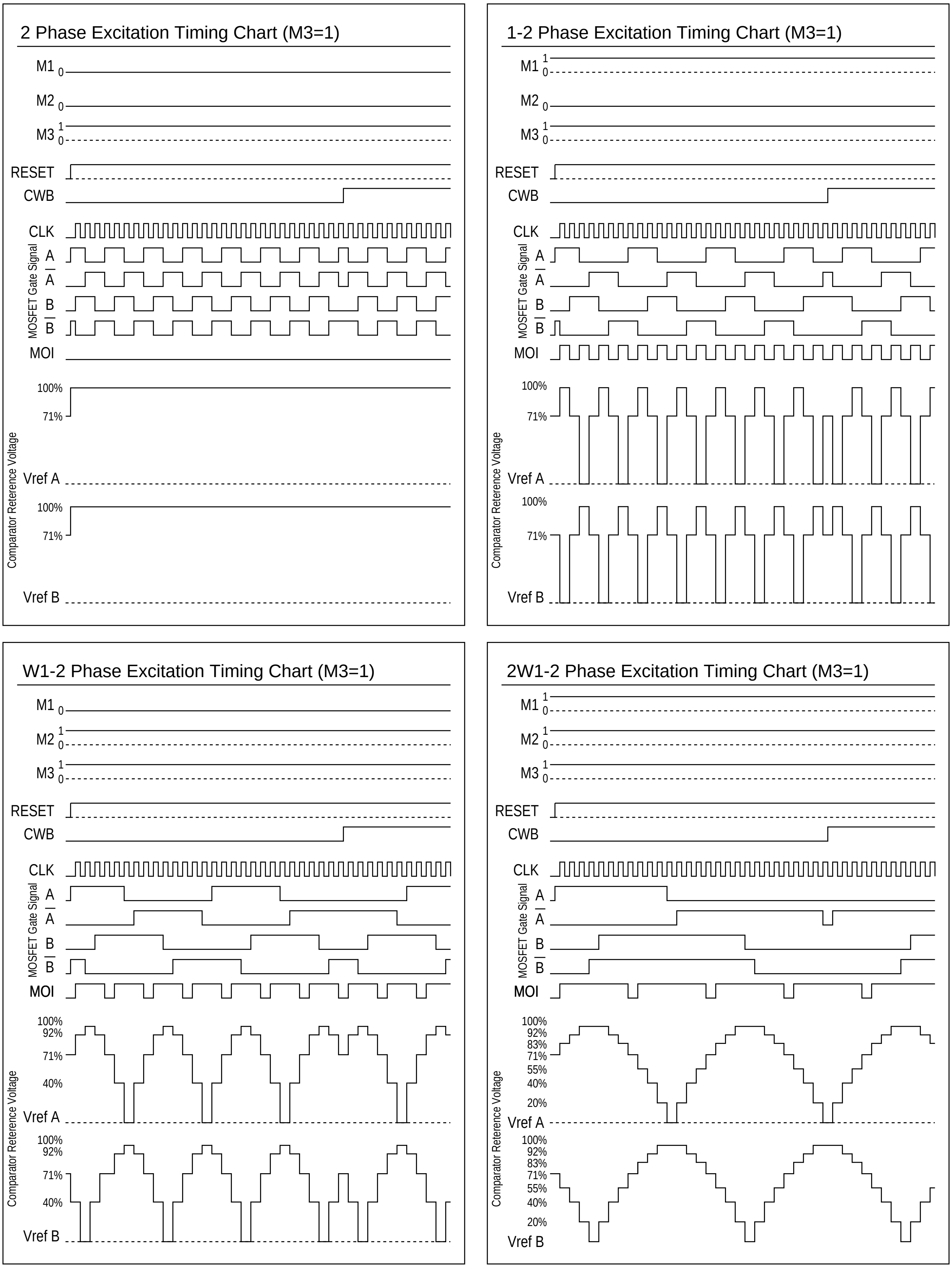
- Excitation phases before and after excitation mode switching <counterclockwise direction>



A13267

Excitation Time and Timing Charts

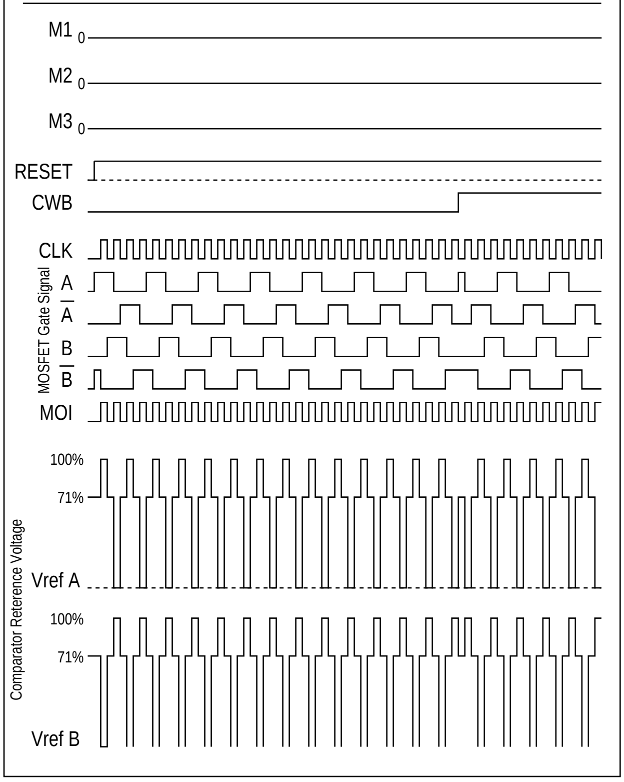
- CLK rising edge operation



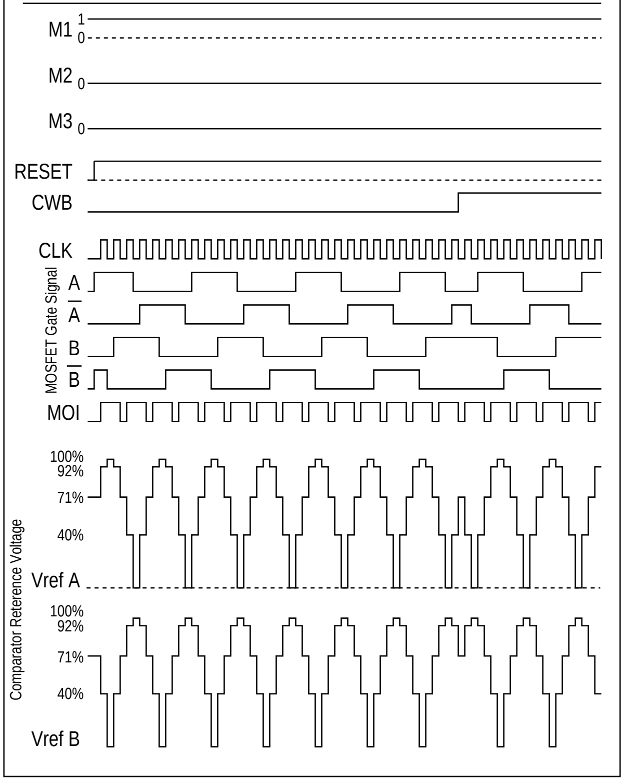
A13268

• CLK rising and falling edge operation

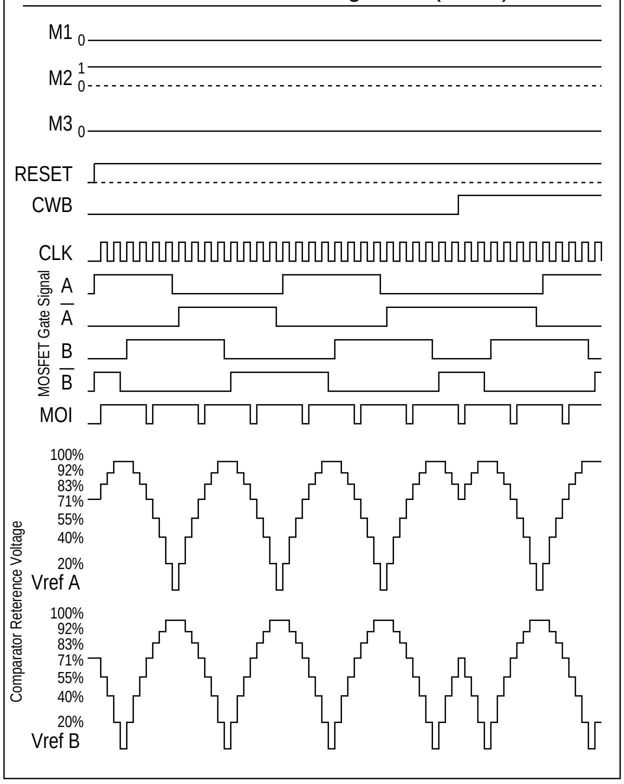
1-2 Phase Excitation Timing Chart (M3=0)



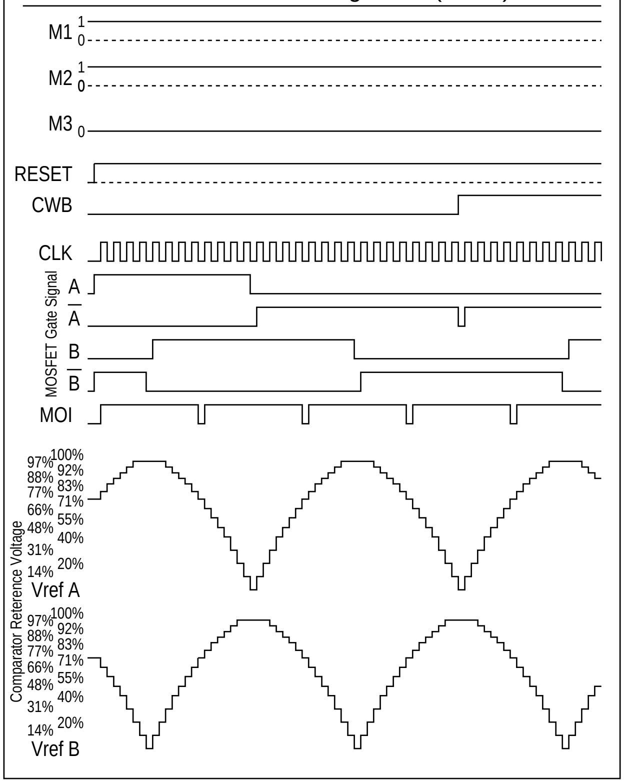
W1-2 Phase Excitation Timing Chart (M3=0)



2W1-2 Phase Excitation Timing Chart (M3=0)



4W1-2 Phase Excitation Timing Chart (M3=0)



A13269

Thermal Design

<Hybrid IC Average Internal Power Loss Pd>

The main elements internal to this hybrid IC with large average power losses are the current control devices, the regenerative current diodes, and the current detection resistor. Since sine wave drive is used, the average power loss during microstepping drive can be approximated by applying a waveform factor of 0.64 to the square wave loss during 2 phase excitation.

The losses in the various excitation modes are as follows.

2 phase excitation
$$Pd_{2EX} = (Vsat + Vdf) \cdot \frac{fclock}{2} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{2} \cdot (Vsat \cdot t1 + Vdf \cdot t3)$$

1-2 phase excitation
$$Pd_{1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{4} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{4} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

W1-2 phase excitation
$$Pd_{W1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{8} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{8} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

2W1-2 phase excitation
$$Pd_{2W1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

4W1-2 phase excitation
$$Pd_{4W1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

Here, t1 and t3 can be determined from the same formulas for all excitation methods.

$$t1 = \frac{-L}{R + 0.35} \cdot \ell n \left(1 - \frac{R + 0.35}{V_{CC}1} \cdot I_{OH}\right) \qquad t3 = \frac{-L}{R} \cdot \ell n \left(\frac{V_{CC}1 + 0.35}{I_{OH} \cdot R + V_{CC}1 + 0.35}\right)$$

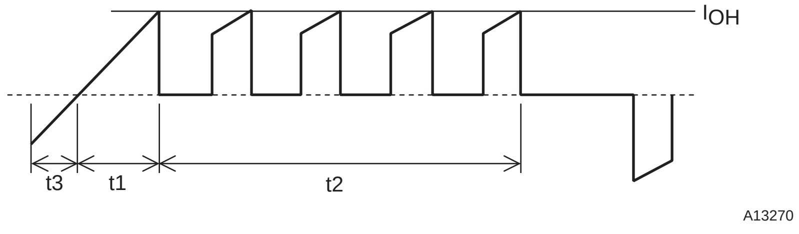
However, the formula for t2 differs with the excitation method.

2 phase excitation $t2 = \frac{2}{fclock} - (t1 + t3)$

1-2 phase excitation $t2 = \frac{3}{fclock} - t1$

W1-2 phase excitation $t2 = \frac{7}{fclock} - t1$

2W1-2 phase excitation
4W1-2 phase excitation $t2 = \frac{15}{fclock} - t1$



Motor Phase Current Model Figure (2 Phase Excitation)

fclock: CLK input frequency (Hz)
Vsat: The voltage drop of the power MOSFET and the current detection resistor (V)
Vdf: The voltage drop of the body diode and the current detection resistor (V)
I_{OH}: Phase current peak value (A)
t1: Phase current rise time (s)
t2: Constant-current operating time (s)
t3: Phase switching current regeneration time (s)
$V_{CC}1$: Supply voltage applied to the motor (V)
L: Motor inductance (H)
R: Motor winding resistance (W)

<Determining the Size of the Hybrid IC Heat Sink>

Determine θc-a for the heat sink from the average power loss determined in the previous item.

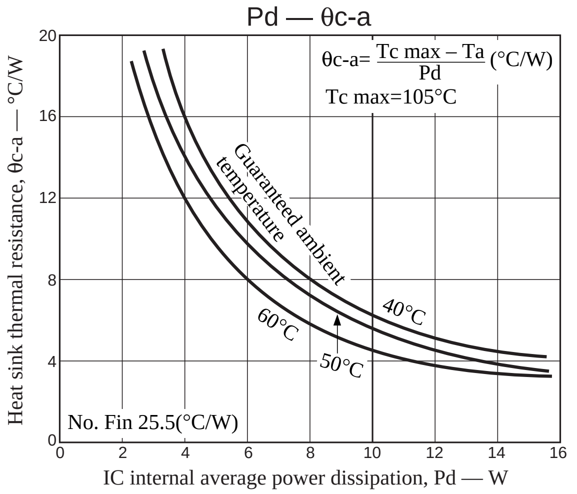
$$\theta c\text{-}a = \frac{Tc\ max - Ta}{Pd_{EX}}\ [°C/W]$$

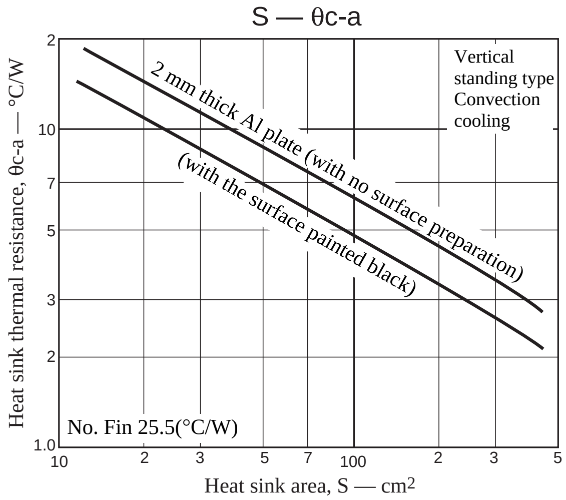
Tc max: Hybrid IC substrate temperature (°C)

Ta: Application internal temperature (°C)

Pd_{EX}: Hybrid IC internal average loss (W)

Determine θc-a from the above formula and then size S (in cm^2) of the heat sink from the graphs shown below.
The ambient temperature of the device will vary greatly according to the air flow conditions within the application. Therefore, always verify that the size of the heat sink is adequate to assure that the Hybrid IC back surface (the aluminum plate side) will never exceed a Tc max of 105°C, whatever the operating conditions are.





Next we determine the usage conditions with no heat sink by determining the allowable hybrid IC internal average loss from the thermal resistance of the hybrid IC substrate, namely 25.5 °C/W.

For a Tc max of 105°C at an ambient temperature of 50°C $\quad Pd_{EX} = \dfrac{105 - 50}{25.5} = 2.15\ W$

For a Tc max of 105°C at an ambient temperature of 40°C $\quad Pd_{EX} = \dfrac{105 - 40}{25.5} = 2.54\ W$

This hybrid IC can be used with no heat sink as long as it is used at operating conditions below the losses listed above.
(See $\Delta Tc - P_d$ curve in the graph on page 17.)

<Hybrid IC internal power element (MOSFET) junction temperature calculation>

The junction temperature, Tj, of each device can be determined from the loss Pds in each transistor and the thermal resistance θj-c.

$$Tj = Tc + \theta j\text{-}c \times Pds\ (°C)$$

Here, we determine Pds, the loss for each transistor, by determining Pd_{EX} in each excitation mode.

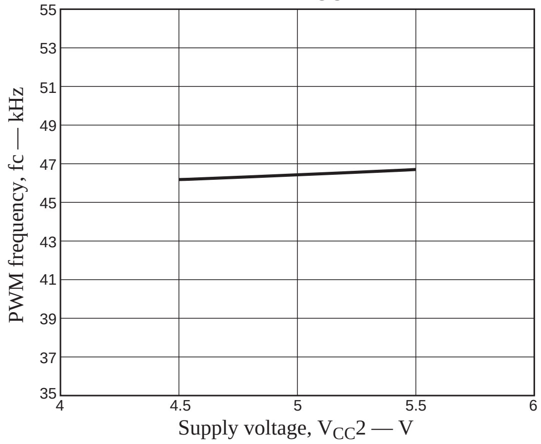
$$Pds = Pd/4$$

Since the average loss includes the loss of the current detection resistor, we take that voltage drop into consideration in the calculation.

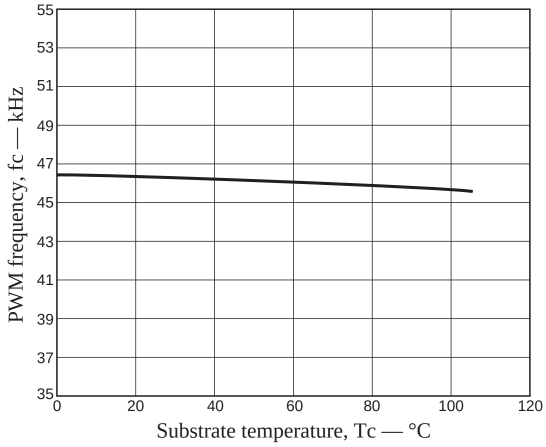
$$Vsat = I_{OH} \cdot Ron + I_{OH} \cdot Rs$$
$$Vdf = Vdf + I_{OH} \cdot Rs$$

The steady-state thermal resistance of a power MOSFET is 15.6°C/W.

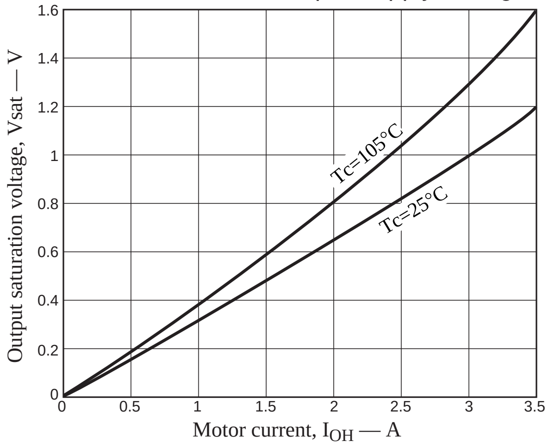
fc — $V_{CC}2$



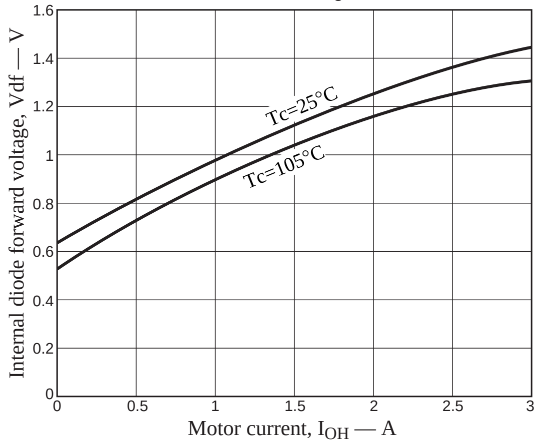
fc — Tc



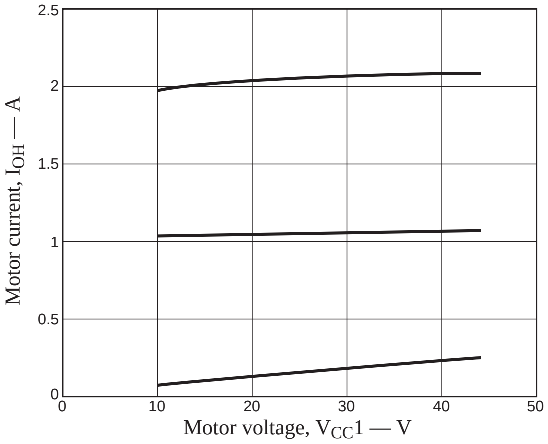
Motor Current vs. Output Supply Voltage



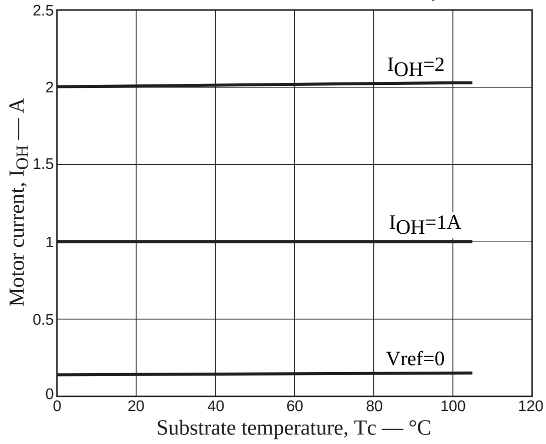
Internal Diode Forward Voltage vs. Motor Current



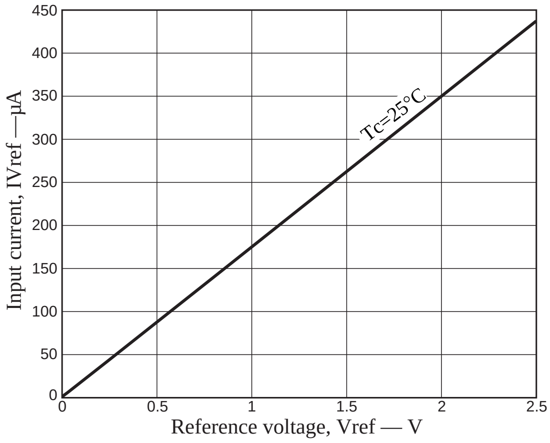
Motor Current vs. Motor Voltage



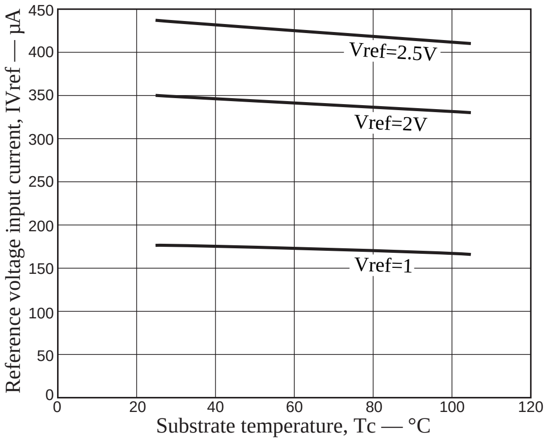
Motor Current vs. Substrate Temperature



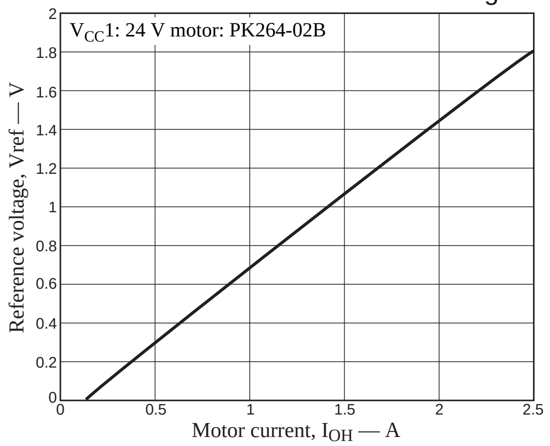
Reference Voltage vs. Input Current



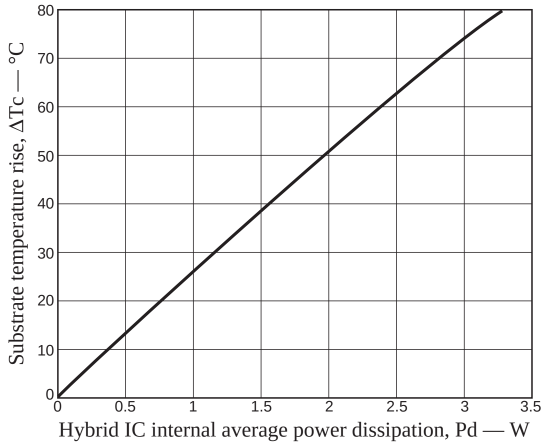
Reference Voltage Input Current vs. Substrate Temperature



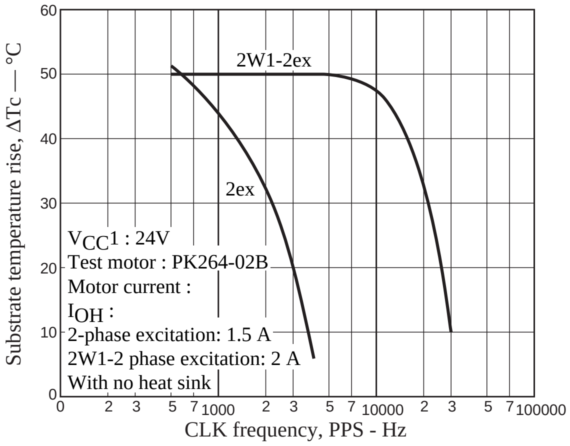
Motor Current vs. Reference Voltage



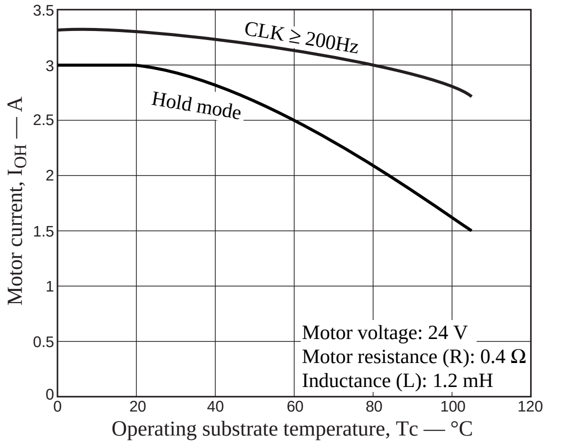
ΔTc — Pd



Substrate Temperature Rise Test



Motor Current (I_{OH}) Derating Curves for the Operating Substrate Temperature Tc



Notes • The above current ranges apply when the output voltage is not in the avalanche state.
• The above operating substrate temperatures (Tc) are measured when the motor is operating. Since Tc will vary depending on the ambient temperature (Ta), the value of I_{OH}, and whether I_{OH} is continuous or intermittent, the actual values of Tc must be verified (measured) in an actual operating end product.

This catalog provides information as of February, 2002. Specifications and information herein are subject to change without notice.