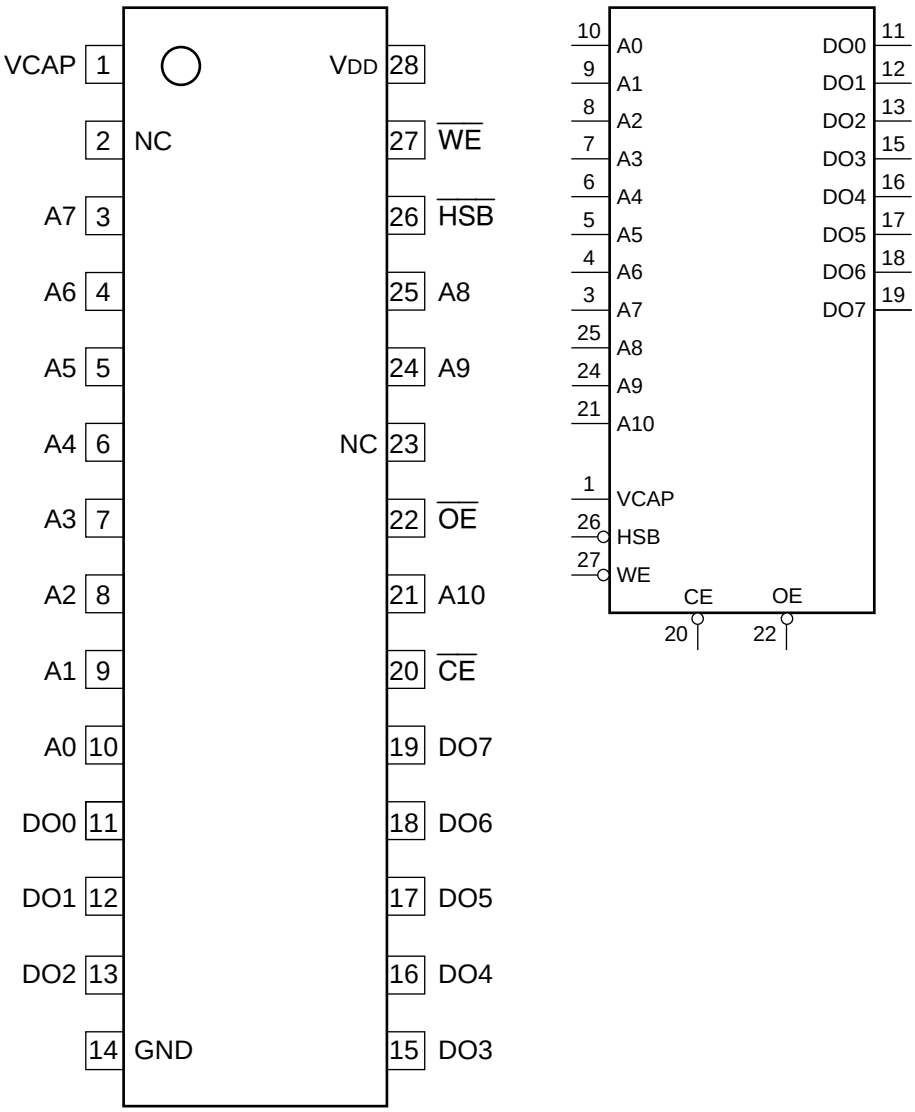
C-MOS (2 K × 8)-BIT NONVOLATILE SRAM

—TOP VIEW—



INPUT

A0 - A10 : ADDRESS
$\overline{CE}$: CHIP ENABLE
$\overline{HSB}$: HARDWARE STROBE/BUSY
$\overline{OE}$: OUTPUT ENABLE
VCAP : CAPACITOR
$\overline{WE}$: WRITE ENABLE

INPUT/OUTPUT

DO0 - DO7 : DATA