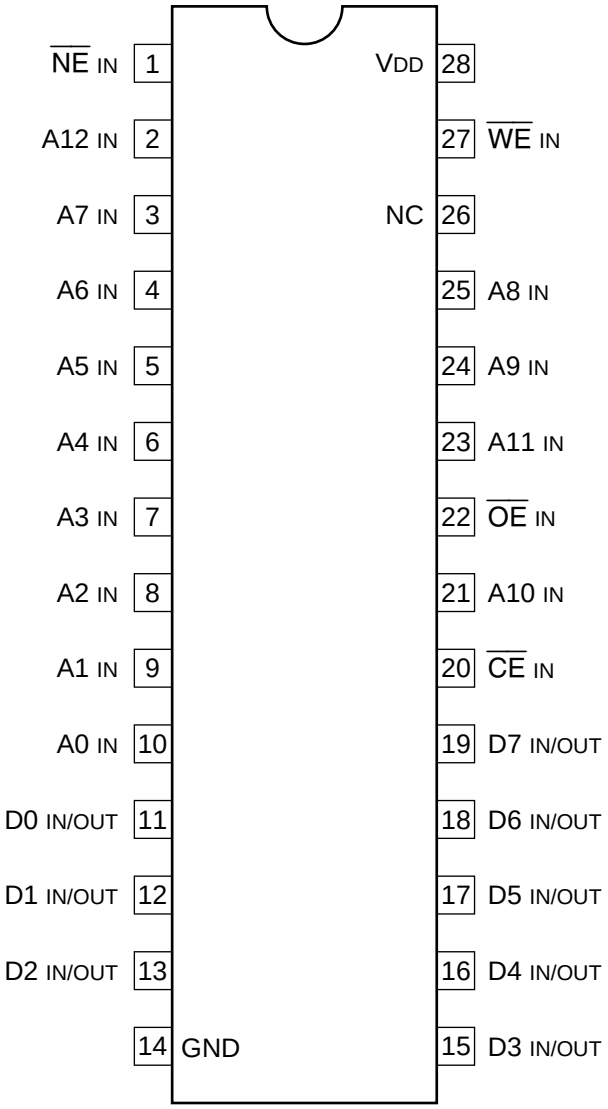
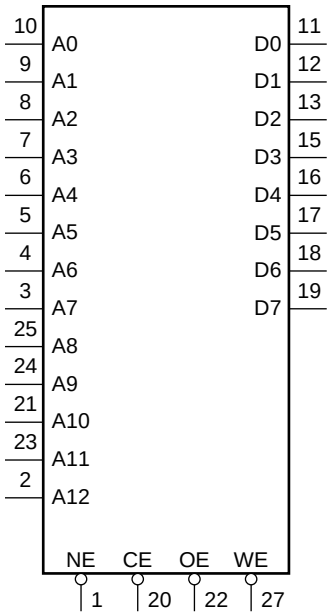
C-MOS 8 K × 8-BIT NONVOLATILE SRAM

—TOP VIEW—



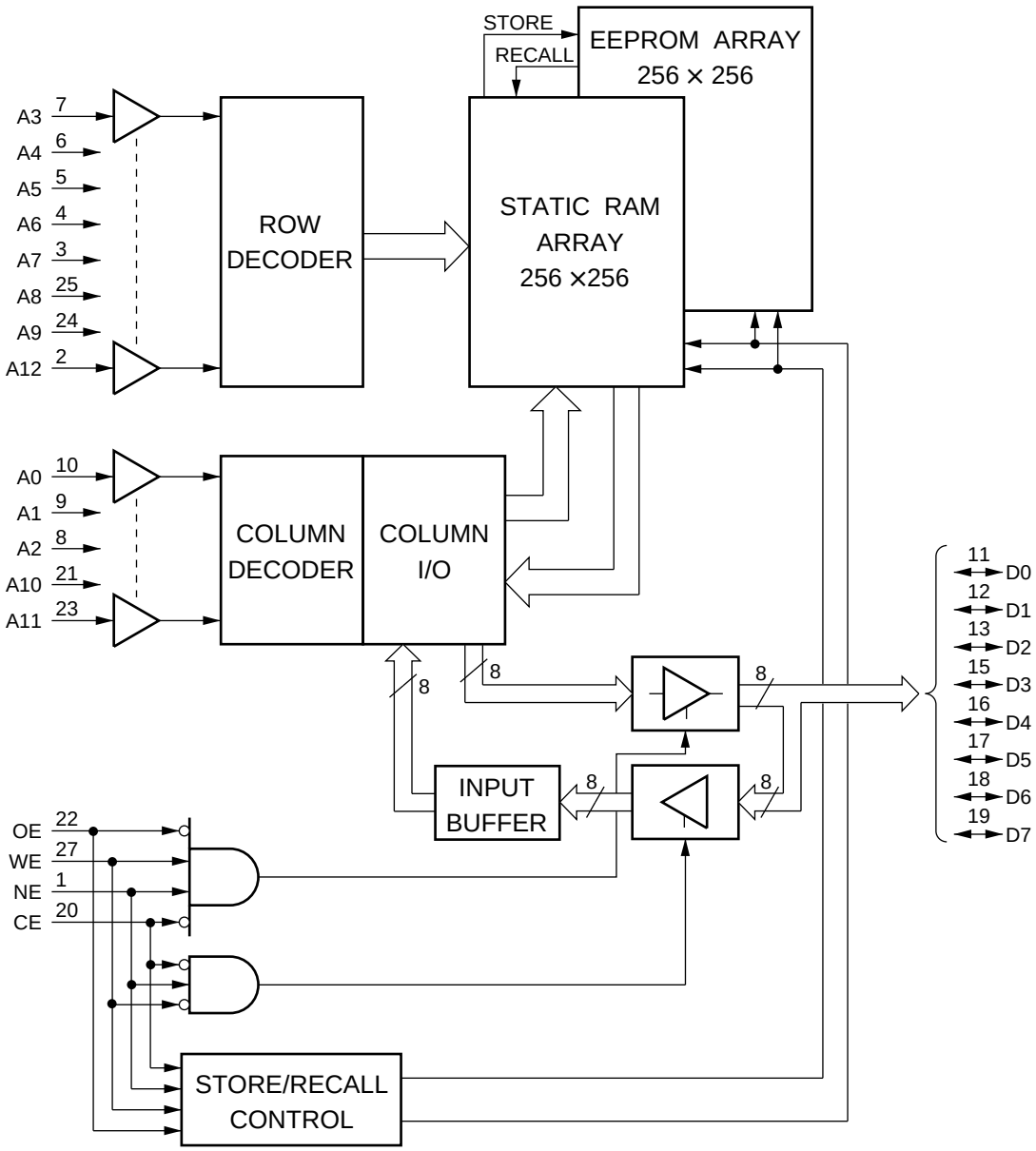


INPUT

A0 - A12 : ADDRESS
$\overline{CE}$: CHIP ENABLE
$\overline{NE}$: NONVOLATILE ENABLE
$\overline{OE}$: OUTPUT ENABLE
$\overline{WE}$: WRITE ENABLE

INPUT/OUTPUT

D0 - D7 : DATA


STORE
RECALL
EEPROM ARRAY
256 × 256
STATIC RAM
ARRAY
256 ×256
ROW
DECODER
A3
A4
A5
A6
A7
A8
A9
A12
7
6
5
4
3
25
24
2
A0
A1
A2
A10
A11
10
9
8
21
23
COLUMN
DECODER
COLUMN
I/O
8
8
8
8
INPUT
BUFFER
11
12
13
15
16
17
18
19
D0
D1
D2
D3
D4
D5
D6
D7
OE
WE
NE
CE
22
27
1
20
STORE/RECALL
CONTROL