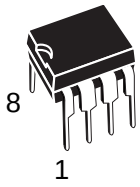
ST95040
ST95020, ST95010

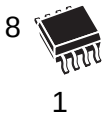
4K/2K/1K Serial SPI EEPROM with Positive Clock Strobe

DATA BRIEFING

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST950x0
  - 2.5V to 5.5V for ST950x0W
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES

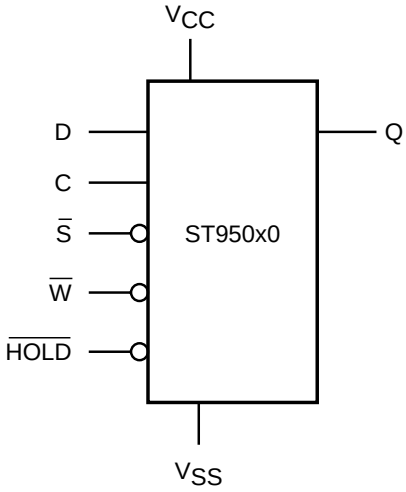


PSDIP8 (B)
0.25mm Frame



SO8 (M)
150mil Width

Logic Diagram



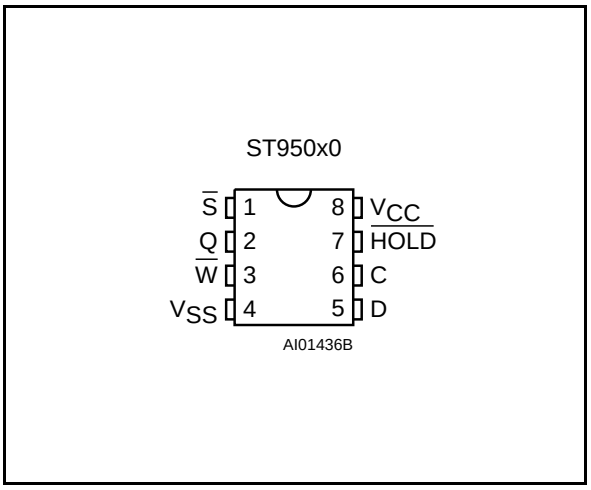
DESCRIPTION

The ST950x0 is a family of Electrically Erasable Programmable Memories (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

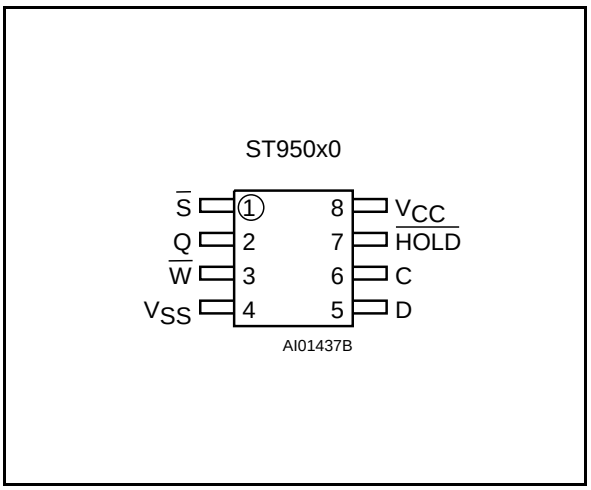
The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

DIP Pin Connections



SO Pin Connections



Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

Example: ST95xx0 W M 6 TR

Density

04 64K (8K x 8)
02 32K (4K x 8)
01 16K (2K x 8)

Data Strobe

0 Note 1

Operating Voltage

blank 4.5V to 5.5V
W 2.5V to 5.5V

Package

B PSDIP8 0.25mm Frame
M SO8 150mil Width

Temp. Range

1 0 to 70 °C
6 –40 to 85 °C
3 (2) –40 to 125 °C

Option

TR Tape & Reel Packing

Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.
2. Temperature range on request only, 5V ± 10% only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).