SGS-THOMSON MICROELECTRONICS

ST95022

2Kbit SERIAL SPI EEPROM with HIGH SPEED CLOCK

DATA BRIEFING

- HIGH SPEED CLOCK RATE:
  - 2.1 MHz Max
- 1,000,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES

SO8 (M)
150mil Width

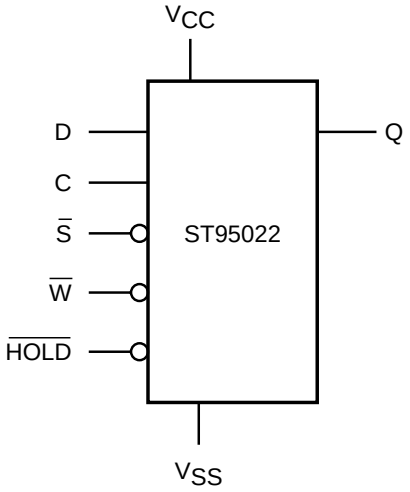
DESCRIPTION

The ST95022 is an high speed 2 Kbit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

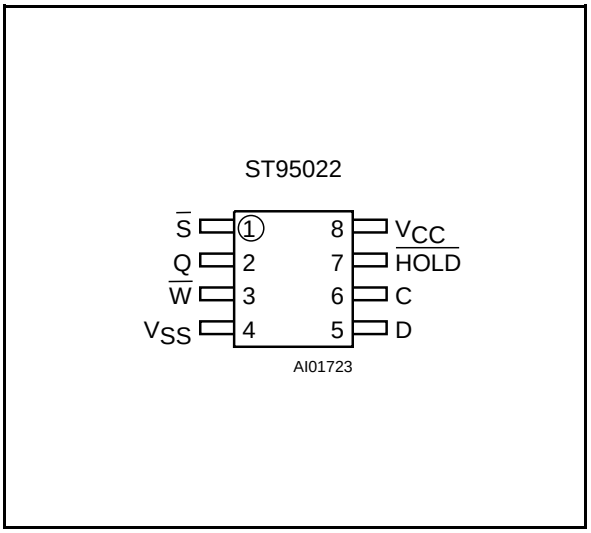
The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

Logic Diagram



SO Pin Connections



Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options or for further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: ST95022 – M 3 TR

Data Strobe

2 Note 1

Package

M SO8
150mil Width

Temp. Range

3 –40 to 125 °C

Option

TR Tape & Reel
Packing

Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).