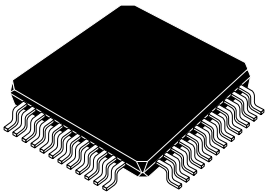
ST7597

AC97 AUDIO CODEC

PRODUCT PREVIEW

- ANALOG I/O COMPONENT OF 2-CHIP PC AUDIO SOLUTION
- STANDARD 48-PIN PACKAGE
- SPLIT DIGITAL/ANALOG ARCHITECTURE FOR IMPROVED S/N RATIO (>90dB achievable)
- 16-BIT STEREO FULL-DUPLEX CODEC WITH FIXED 48K SAMPLING RATE
- FOUR ANALOG LINE LEVEL STEREO INPUTS FOR CONNECTION FROM LINE IN, CD, VIDEO AND AUX
- TWO ANALOG LINE LEVEL MONO INPUTS FOR SPEAKERPHONE (or DLP(1)) AND PC BEEP
- MONO MIC INPUT SWITCHABLE FROM TWO EXTERNAL SOURCES
- HIGH QUALITY PSEUDO-DIFFERENTIAL CD INPUT
- STEREO LINE LEVEL OUTPUT
- MONO OUTPUT FOR SPEAKERPHONE (or DLP(1))
- POWER MANAGEMENT SUPPORT
- TONE CONTROL (TREBLE / BASS)

(1) DLP : Down Line Phone



TQFP48 (7 x 7 x 1.4mm)
(Plastic Quad Flat Pack)

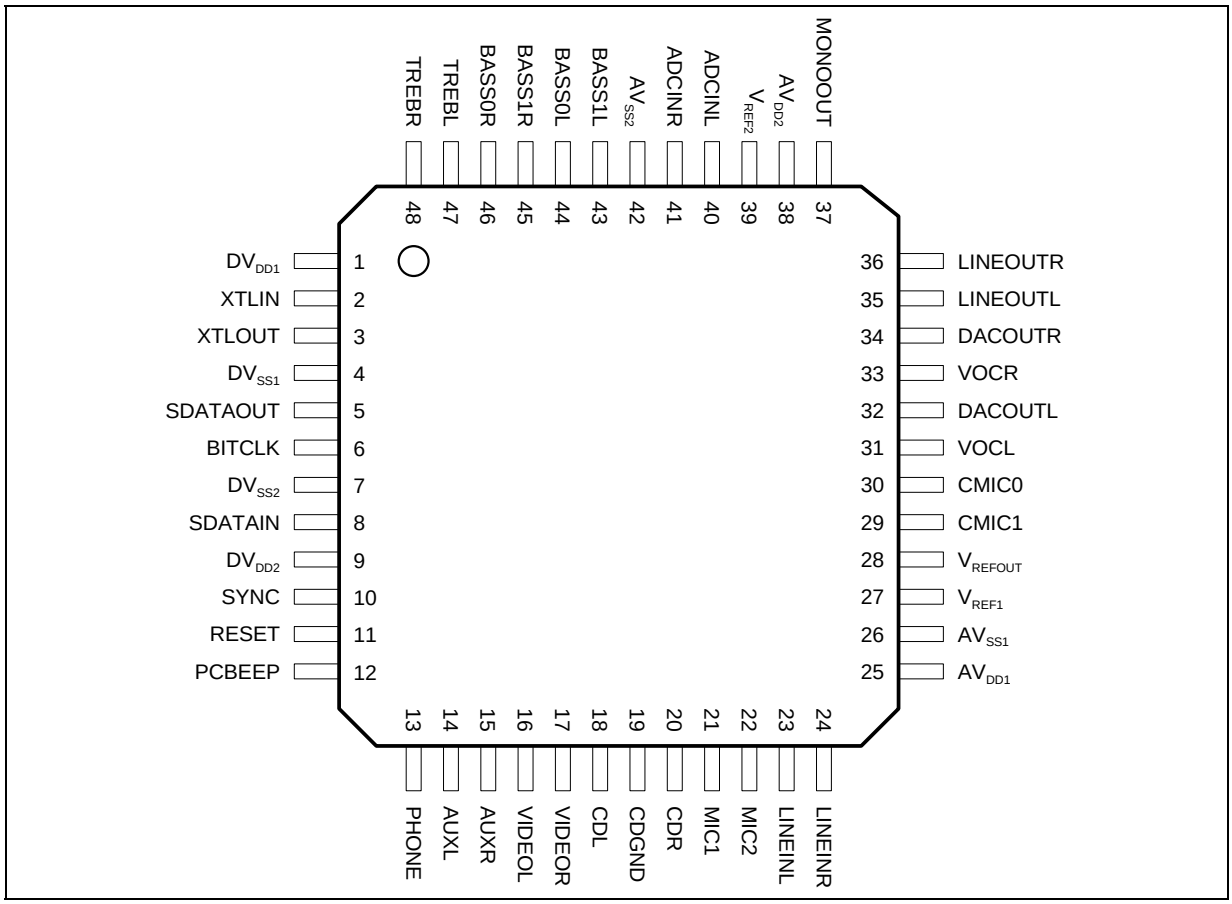
ORDER CODE : ST7597

DESCRIPTION

The ST7597 is an analog component of a 2-chip audio solution (which is not described in this specification). The two fixed 48kHz DAC's support a stereo PCM output channel which contains a mix generated in the ST7597 controller of all software sources, including the internal synthesizer and any other digital sources. PCM out is mixed with analog sources, processed with optional Stereo Enhancement and tone controls, and sent to independently controlled LINE_OUT. For speakerphone telephony, the MONO_OUT delivers either mic only or a mono mix sources to the telephony subsystem.

The ADC path support 2 channel of fixed 48kHz input. The standard stereo PCM in channel supports record of any mono or stereo source, or a mix of sources.

PIN CONNECTIONS



7597-01.EPS

PIN LIST

Pin	Type	Name	Function	Remark
01	PWR	DV_{DD1}	Digital Power Supply	PPH_CL
02	AI	XTLIN	Crystal Ocsillator Input	Connected to 15pF external capacitance
03	AO	XTLOUT	Crystal Oscillator Output	Connected to 15pF external capacitance
04	PWR	DV_{SS1}	Digital Ground	PPL_CL
05	DI	SDATAOUT	Serial AC97 Input Stream	SCHMITT_CL_5V, TTL schmitt input
06	T	BITCLK	12.288MHz Serial Data Clock	BT8CR_CL_5V, CMOS tristate 8mA wo/ SR control
07	PWR	DV_{SS2}	Digital Ground	PPL_CL
08	T	SDATAIN	Serial AC97 Output Stream	BT8CR_CL_5V, CMOS tristate 8mA w/ SR control
09	PWR	DV_{DD2}	Digital Power Supply	PPH_CL
10	DI	SYNC	48kHz fixed rate samples sync	SCHMITT_CL_5V, TTL schmitt input
11	DI	RESET	AC97 Master Hardware Reset	SCHMITT_CL_5V, TTL schmitt input
12	AI	PCBEEP	PC Speaker beep pass through	IP1X_CL
13	AI	PHONE	From Telephony Subsystem Speakerphone	IP1X_CL

7597-01.TBL

Abbreviations :

A	Analog
D	Digital
I	Input
O	Output
PWR	Power Supply
T	Tristate

PIN LIST (continued)

Pin	Type	Name	Function	Remark
14	AI	AUXL	Auxiliaire Left Channel	IP1X_CL
15	AI	AUXR	Auxiliaire Right Channel	IP1X_CL
16	AI	VIDEOL	Video Audio Left Channel	IP1X_CL
17	AI	VIDEOR	Video Audio Right Channel	IP1X_CL
18	AI	CDL	CD Audio Left Ghannel	IP1X_CL
19	PWR	CDGND	CD Audio Analog Ground	PPX_CL
20	AI	CDR	CD Audio Right Channel	IP1X_CL
21	AI	MIC1	DeskTop Microphone Input	IP1X_CL
22	AI	MIC2	Second Microphone Input	IP1X_CL
23	AI	LINEINL	Line Input Left Channel	IP1X_CL
24	AI	LINEINR	Line Input Right Channel	IP1X_CL
25	PWR	AV_{DD1}	Analog Power Supply	PPX_CL
26	PWR	AV_{SS1}	Analog Ground	PPX_CL
27	AO	V_{REF1}	Mixer Reference Voltage	OP1X_CL
28	AO	V_{REFOUT}	Reference Voltage 5mA drive	OP1X_CL
29	AI	CMIC1	MIC Mixer Input Channel	IP1X_CL, connected to CMIC0 via 0.1µF capacitor
30	AO	CMIC0	MIC20dB Output	OP1X_CL, connected to CMIC1 via 0.1µF capacitor
31	AI	VOCL	Voice Left Channel	IP1X_CL, connected to DACOUTL via 0.1µF capacitor
32	AO	DACOUTL	DAC output Left Channel	OP1X_CL, connected to VOCL via 0.1µF capacitor
33	AI	VOCR	Voice Right Channel	IP1X_CL, connected to DACOUTR via 0.1µF capacitor
34	AO	DACOUTR	DAC output Right Channel	OP1X_CL, connected to VOCR via 0.1µF capacitor
35	AO	LINEOUTL	Line Output Left Channel	OP1X_CL
36	AO	LINEOUTR	Line Output Right Channel	OP1X_CL
37	AO	MONOOUT	To Telephony Subsystem Speakerphone	OP1X_CL
38	PWR	AV_{DD2}	Analog Power Supply	PPX_CL
39	AO	V_{REF2}	Codec Reference Voltage	OP1X_CL
40	AO	ADCINL	Test Point, Record Output Left Channel	OP1X_CL
41	AO	ADCINR	Test Point, Record Output Right Channel	OP1X_CL
42	PWR	AV_{SS2}	Analog Ground	PPX_CL
43	AO	BASS1L	Bass Capacitor Left Channel	OP1X_CL, connected to BASS0L via 68nF capacitor
44	AO	BASS0L	Bass Capacitor Left Channel	OP1X_CL, connected to BASS1L via 68nF capacitor
45	AO	BASS1R	Bass Capacitor Right Channel	OP1X_CL, connected to BASS0R via 68nF capacitor
46	AO	BASS0R	Bass Capacitor Right Channel	OP1X_CL, connected to BASS1R via 68nF capacitor
47	AO	TREBL	Treble Capacitor Left Channel	OP1X_CL, connected to VREF1 via 2.2nF capacitor
48	AO	TREBR	Treble Capacitor Right Channel	OP1X_CL, connected to VREF1 via 2.2nF capacitor

7597-01.TBL

Abbreviations :

A	Analog
D	Digital
I	Input
O	Output
PWR	Power Supply
T	Tristate

PIN/SIGNAL DESCRIPTION

1 - Digital I/O

These signals connect the ST7597 component to its controller counterpart and external crystal.

Signal Name	Type	Description
RESET	I	ST7597 master H/W reset
XTLIN XTLOUT	I O	24.576MHz crystal
SYNC	I	48kHz fixed rate sample sync
BITCLK	O	12.288MHz serial data clock
SDATAOUT	I	Serial, time division multiplexed, ST7597 input stream
SDATAIN	O	Serial, time division multiplexed, ST7597 input stream

2 - Analog I/O

These signals connect the ST7597 component to analog sources and sinks, including microphones and speakers.

Signal Name	Type	Description
PCBEEP	I	PC speaker beep pass through
PHONE	I	From telephony subsystem speakerphone (or DLP)
MIC1 MIC2	I I	Desktop microphone input Second microphone input
LINEINL LINEINR	I I	Line input left channel Line input right channel
CDL CDR	I I	CD audio left channel CD audio right channel
CDGND	I	CD audio analog ground
VIDEOL VIDEOR	I I	Video audio left channel Video audio right channel
AUXL AUXR	I I	Aux left channel Aux right channel
LINEOUTL LINEOUTR	O O	Line output left channel Line output right channel
MONOOUT	O	To telephony subsystem spealerphone (or DLP)

3 - Filter/References

These signals are connected to capacitors.

Signal Name	Type	Description
V_{REF1}	O	Reference voltage - used by the Mixer, two decoupling capacitance grounded
V_{REF2}	O	Reference voltage - used by the Codec, two decoupling capacitance grounded
V_{REFOUT}	O	Reference voltage 5mA drive (intended for mic bias)
BASS0L, BASS1L	O	Bass control, 68nF connected to BASS1L
BASS0R, BASS1R	O	Bass control, 68nF connected to BASS1R
TREBL	O	Treble control, 2.2nF connected to Mixer reference
TREBR	O	Treble control, 2.2nF connected to Mixer reference
DACOUTL VOCL	O I	DAC output, decoupling capacitor, 0.1µF connected to VOCL
DACOUTR VOCR	O I	DAC output, decoupling capacitor, 0.1µF connected to VOCR
CMIC0 CMIC1	O I	MIC +20dB output, decoupling capacitor 0,1µF connected to CMIC1
ADCINL	O	Test Point , Record Output
ADCINR	O	Test point, Record Output

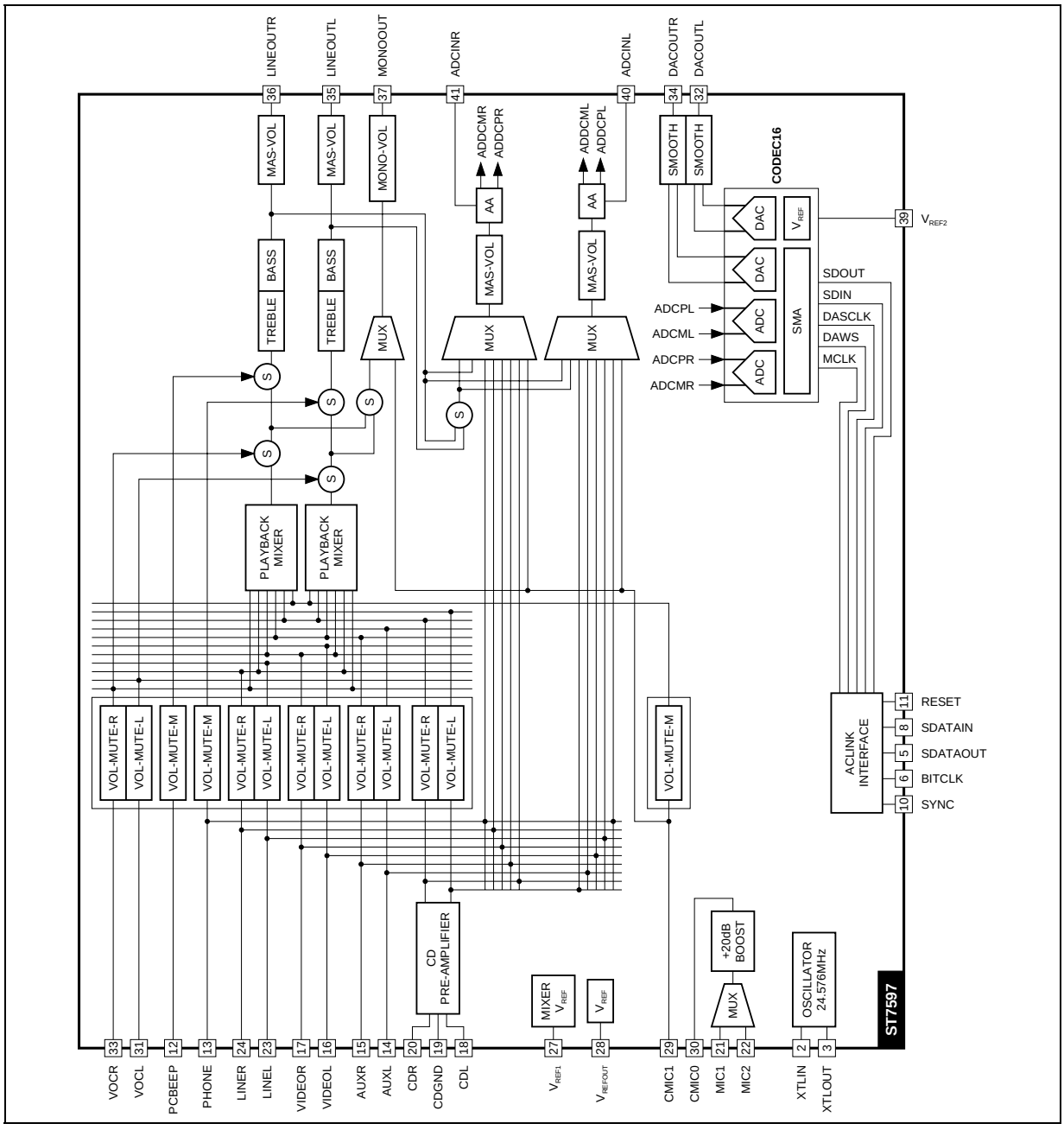
PIN/SIGNAL DESCRIPTION (continued)

4 - Power and Ground signals

This ST7597 is designed to use a 5V power supply.

Signal Name	Type	Description
AV_{DD1}, AV_{DD2}	PWR	Analog V_{DD} 5V
AV_{SS1}, AV_{SS2}	PWR	Analog ground
DV_{DD1}, DV_{DD2}	PWR	Digital V_{DD} 5V
DV_{SS1}, DV_{SS2}	PWR	Digital ground

BLOCK DIAGRAM



7597-02.EPS

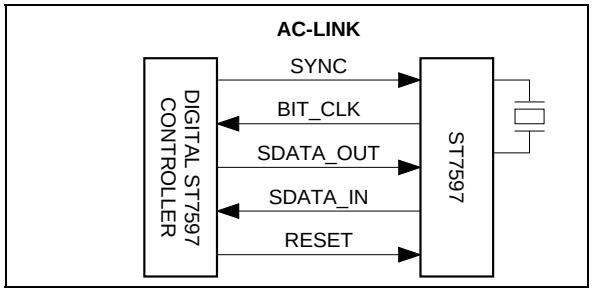
FUNCTIONAL DESCRIPTION

1 - System Usage

1.1 - ST7597 Connection to the digital controller

ST7597 communicates with its companion ST7597 controller via a digital serial link, "AC-link". All digital audio streams, and command/status information are communicated over this point to point serial interconnect. A breakout of signals connecting the two is shown below. The section 2 gives a detailed description of the AC-link.

Figure 1



1.2 - Clocking

ST7597 derives its clock internally from an externally attached 24.576MHz crystal and drives a buffered and divided down (1/2) clock to its digital companion controller over AC-link under the signal name "BITCLK". Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock provides ST7597 with a clean clock that is independant of the physical proximity of the ST7597 companion digital controller (henceforth referred to as the "ST7597 controller).

The beginning of all audio sample packets, or "Audio Frames", transferred over the AC-link is synchronized to the rising edge of the "SYNC" signal. SYNC is driven by the ST7597 controller. The ST7597 controller takes BITCLK as an input and generates SYNC by dividing BITCLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BITCLK, and subsequently sampled on the receiving side of the AC-link on each immediately following falling edge of BITCLK.

1.3 - Resetting the ST7597

There are 3 types of ST7597 reset :

1. A "cold" reset where all ST7597 logic (registers included) is initialized to its default state ;
2. A "warm" reset where the contents of the ST7597 register set are left unaltered ;
3. A "register" reset which only initializes the ST7597 registers to their default states.

After signaling a reset to the ST7597, the ST7597 controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indication from ST7597 (refer to section 2 for details).

2 - Digital Interface

2.1 - AC-link Digital Serial Interface Protocol

ST7597 incorporates a 5-pin digital serial interface that links it to the ST7597 controller. AC-link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input, and output audio streams, as well as control registers accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With the headroom that the AC-link architecture provides, the current version of ST7597 including DAC and ADC resolution of 16-bits, will be increased to 18 or 20 bits DAC/ADC resolution.

The data streams defined by the ST7597 include :

- PCM PLAYBACK data (2 output slots)
  2 channel composite PCM output stream
- PCM RECORD data (2 input slots)
  2 channel composite PCM input stream
- Control (2 output slots)
  Control register write port
- Status (2 input slots)
  Control register read port

Synchronization of all AC-link data transactions is signaled by the ST7597 controller. ST7597 drives the serial bit clock onto AC-link, which the ST7597 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48kHz, is derived by dividing down the serial bit clock (BITCLK). BITCLK, fixed at 12.288MHz, provides the necessary cloking granularity to support 12, 20-bit outgoing and incoming time slots AC-link serial data is transitioned on each rising edge of BITCLK. The receiver of AC-link data, ST7597 for outgoing data and ST7597 controller for incoming data, samples each serial bit on the falling edges of BITCLK.

The AC-link protocol provides for a special 16-bit (13-bit defined, with 3 reserved trailing bit positions) time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "tagged" invalid, it is the responsability of the source of the data (ST7597 for the input stream, ST7597 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

FUNCTIONAL DESCRIPTION (continued)

SYNC remains high for a total duration of 16 BITCLK at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power saving, all clock, sync, and data signals can be halted. For that the ST7597 is implemented as a static design to allow its register contents to remain intact when entering a power saving mode.

2.1.1 - AC-link Audio Output Frame (SDATAOUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the ST7597's DAC inputs, and control registers. As briefly mentioned earlier, each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATAOUT slot0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12-bit positions sampled by ST7597 indicate which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48kHz audio frame rate. The Figure 3 illustrates the time slot based AC-link protocol.

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BITCLK. On the immediately following falling edge of BITCLK, ST7597 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of a new audio frame. On the next rising edge of BITCLK, the ST7597 controller transitions SDATAOUT into the first bit position of slot 0 (Valid Frame Bit). Each new bit position is presented to AC-link on a rising edge of BITCLK, and subsequently sampled by ST7597 on the following falling edge of BITCLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned (see Figure 4).

SDATAOUT's composite stream is MSB justified (MSB first) with all non-valid slots'bit positions stuffed with 0's by the ST7597 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the ST7597 controller always stuffs all trailing non-valid bit positions of the 20-bit slot with 0's.

As an example, consider an 8-bit sample stream that is being played out to one of the ST7597's DACs. The first 8-bit positions are presented to the DAC (MSB justified) followed by the next 12-bit positions which are stuffed with 0's by the ST7597 contoller. This ensures that regardless of the resolution of the implemented DAC, no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the ST7597 controller it is necessary that both left and right sample stream time slots be filled with the same data.

Figure 2 : Standard Bi-directional Audio Frame

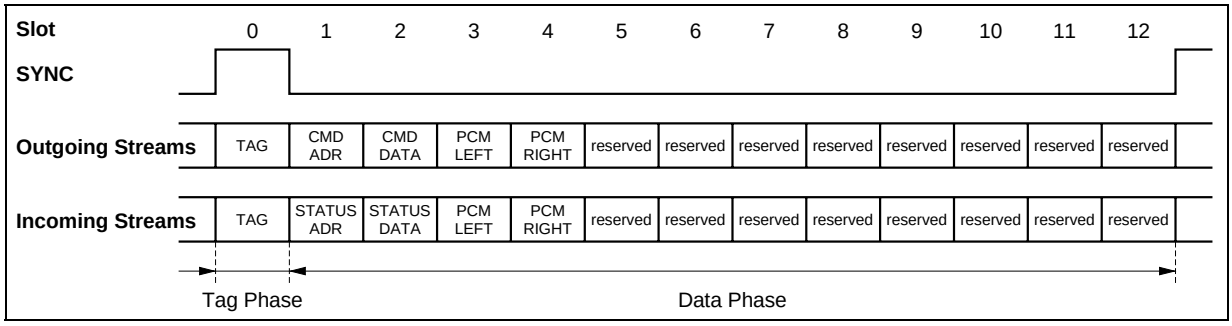
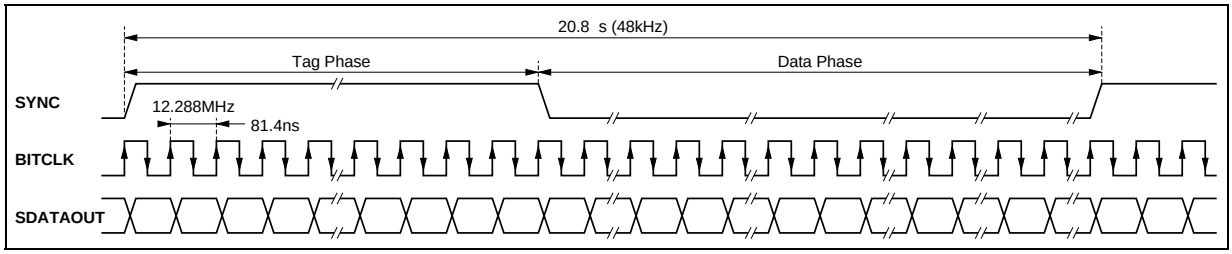
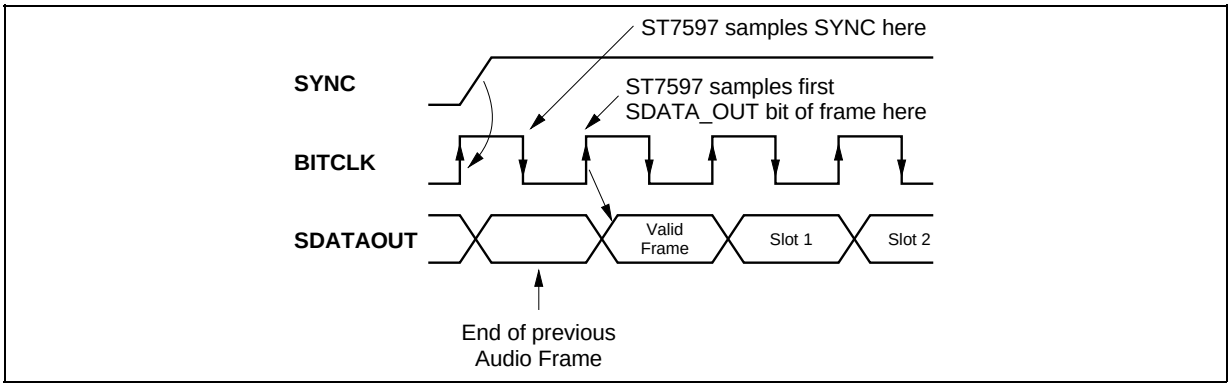


Figure 3 : AC-link Audio Output Frame



FUNCTIONAL DESCRIPTION (continued)

Figure 4 : Start of an Audio Output Frame



2.1.1.1 - Slot 1 : Command Address Port

The command port is used to control features, and monitor status (see Audio Frame Input Slot 1 and Slot 2) for ST7597 functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc) are valid, odd register (01h, 03h, etc) accesses are discouraged, the write in odd addresses will have no effect in the ST7597 and the read of ODD addresses will return a 16-bit contents of 00h. ST7597's control register file is readable and writeable in order to provide more robust testability.

Audio output frame slot 1 communicates control register address, and read/write command information to ST7597.

Command Address Port bit assignments :

Bit(19) Read/Write command (1 = read, 0 = write)

Bit(18:12) Control register index (64 16-bit locations, addresses on even byte boundaries)

Bit(11:0) Reserved (stuffed with 0's)

The first bit (MSB) sampled by ST7597 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12-bit positions within the slot are reserved and must be stuffed with 0's by the ST7597 controller.

2.1.1.2 - Slot 2 : Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by slot 1 bit 19).

Bit(19:4) Control register write data (stuffed with 0's if current operation is a read)

Bit(3:0) Reserved (stuffed with 0's)

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the ST7597 controller.

2.1.1.3 - Slot 3 : PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical 'Games Compatible' PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the ST7597 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the ST7597 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

2.1.1.4 - Slot 4 : PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical 'Games Compatible' PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the ST7597 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the ST7597 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

2.1.1.5 - Slots 5-12 : Reserved

Audio output frame slots 5-12 are reserved for future use and are always stuffed with 0's by the ST7597 controller.

FUNCTIONAL DESCRIPTION (continued)

2.1.2 - AC-link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the ST7597 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot0, bit 15) which flags is in the ST7597 is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that the ST7597 is not ready for normal operation. This condition is normal following the deassertion of power on reset for example, while ST7597's voltage reference settle. When the AC-link "Codec Ready" indicator bit is a 1 it indicates that the AC-link and the ST7597 control and status registers are in fully operational state. The ST7597 controller must futher probe the Powerdown Control/Status Register (section 6.3) to determinate exactly which subsections, if any, are ready.

Prior to any attempts at putting ST7597 into operation the ST7597 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the ST7597 has gone "Codec Ready". Once ST7597 is sampled "Codec Ready" then the next 12-bit positions sampled by the ST7597 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data.
The Figure 5 illustrates the time slot based AC-link protocol.

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, ST7597 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of a new audio frame. On the next rising edge of BIT_CLK, ST7597 transitionss SDATA_IN into the first bit position of slot 0 (Codec Ready Bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by ST7597 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned (see Figure 6).

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid slots'bit positions stuffed with 0's by the ST7597.

Figure 5 : AC-link Audio Input Frame

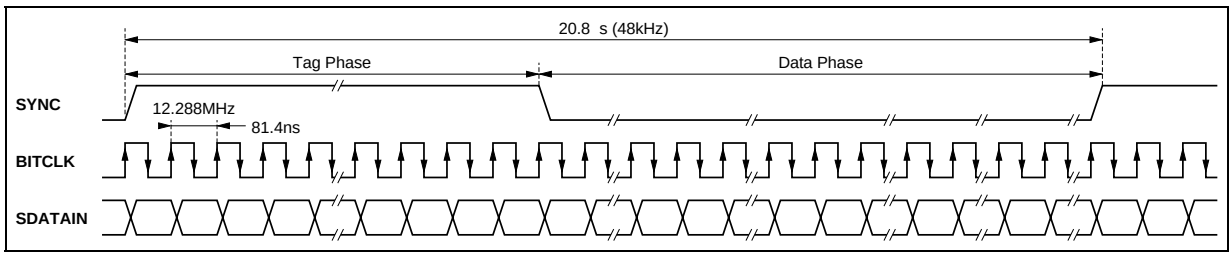
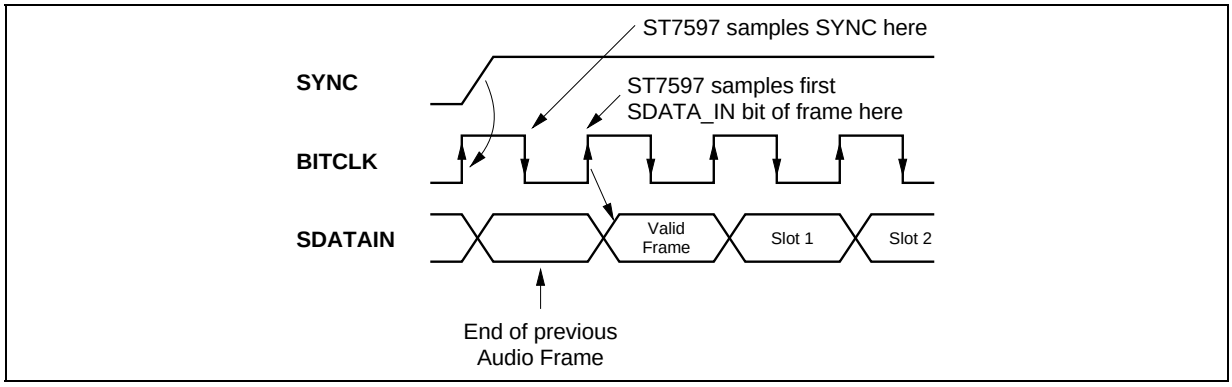


Figure 6 : Start of an Audio Input Frame



FUNCTIONAL DESCRIPTION (continued)

2.1.2.1 - Slot 1 : Status Address Port

The status port is used to monitor status for ST7597 functions including, but not limited to, mixer settings, and power management (refer to the control register section 6.3 of this specification).

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots1 and 2 has been tagged "valid" by ST7597 during slot 0).

Status Address Port bit assignments :

Bit(19) Reserved (stuffed with 0)

Bit(18:12) Control register index (Echo of the register index for which data is being returned)

Bit(11:0) Reserved (stuffed with 0's)

The first bit (MSB) generated by ST7597 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12-bit positions are stuffed with 0's by ST7597.

2.1.2.2 - Slot 2 : Status Data Port

The status data port delivers 16-bit control register read data.

Bit(19:4) Control register read data (stuffed with 0's if tagged "invalid" by ST7597)

Bit(3:0) Reserved (stuffed with 0's)

If slot 2 is tagged "invalid" by ST7597, then the entire slot will be stuffed with 0's by ST7597.

2.1.2.3 - Slot 3 : PCM Record Left Channel

Audio input frame slot 3 is the left channel output of ST7597 input MUX, post-ADC.

ST7597's ADCs is a 16-bit resolution one in this version.

ST7597 out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0's (Bit(3:0)).

2.1.2.4 - Slot 4 : PCM Record Right Channel

Audio input frame slot 4 is the right channel output of ST7597 input MUX, post-ADC.

ST7597's ADCs is a 16-bit resolution one in this version.

ST7597 out its ADC output data (MSB first), and stuffs any trailing non-valid bit positions with 0's (Bit(3:0)).

2.1.2.5 - Slots 5-12 : Reserved

Audio input frame slots 5-12 are reserved for future use and are always stuffed with 0's by the ST7597.

2.2 - AC-link Low Power Mode

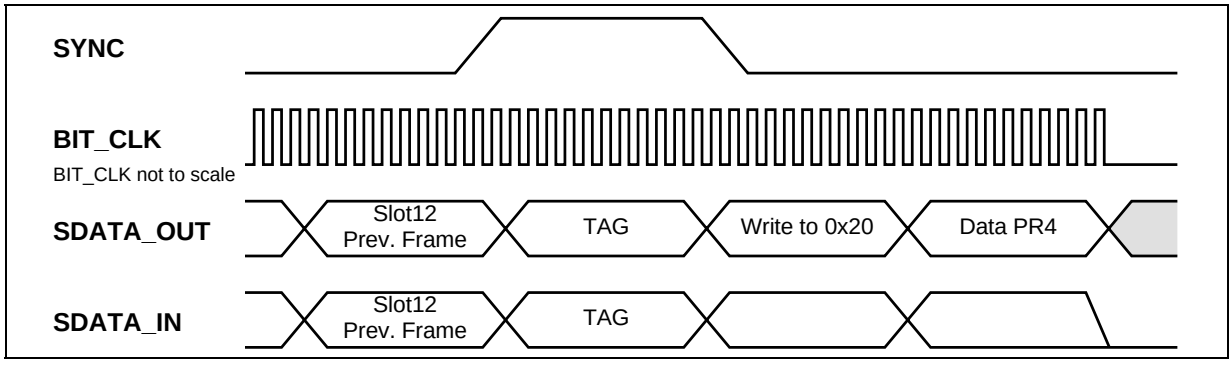
The AC-link signals can be placed in a low power mode (see section 3.3). When ST7597's general purpose register (20h) is programmed to the appropriate value, both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level (see Figure 7).

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the general purpose register (20h) with PR4. When the ST7597 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame (at this point in time it is assumed that all sources of audio input have also been neutralized).

The ST7597 controller should also drive SYNC, and SDATA_OUT low after programming ST7597 to this low power, "halted" mode.

Once the ST7597 has been instructed to halt BIT_CLK, a special "wake-up" protocol must be used to bring the AC-link to the active mode since normal audio output and input frames can not be communicated in the absence of the BIT_CLK.

Figure 7 : AC-link Powerdown Timing



FUNCTIONAL DESCRIPTION (continued)

2.2.1 - Waking up the AC-link

There are 2 methods for bringing the AC-link out of a low power, halted mode,. Regardless of the method, it is the ST7597 controller that performs the wake up task.

AC-link protocol provides for a "Cold ST7597 Reset", and a "Warm ST7597 Reset". The current power down state would ultimately dictate which form of ST7597 reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the ST7597 registers are initialized to their default values, registers will keep state during all power down modes.

Once power down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

2.2.1.1 - Cold ST7597 Reset

A cold ST7597 reset is achieved by asserting RESET for the minimum specified time. By driving RESET low, BIT_CLK, and SDATA_OUT will be activeted, or re-activated as the case may be, and all ST7597 control registers will be initialized to their default power on reset values.

RESET ia an asynchronous ST7597 input (see Figure 8).

2.2.1.2 - Warm ST7597 Reset

A warm ST7597 reset will re-activated the AC-link without altering the current ST7597 register values. A warm reset is signaled by driving SYNC high for a minimum of 1uS in the absence of BIT_CLK.

Within normal audio frames SYNC is a synchronous ST7597 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to ST7597. ST7597 will not respond with the activation of the BIT_CLK until SYNC has sampled low again by ST7597. This will preclude the false detection of a new audio frame (see Figure 9).

2.3 - ATE Test Mode

ST7597 has a ATE in circuit test mode. ST7597 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET.

It is necessary to apply a "cold reset" to resume normal operating mode (see Figure 10).

3 - ST7597 MIXER (see Block Diagram)

The ST7597 mixer is designed to manage playback and record of all digital and analog audio sources, these include :

- System audio : digital PCM input and output for business, games, and multimedia
- CD/DVD : analog CD/DVD-ROM Redbook audio with internal connections to codec mixer
- Mono microphone : choice of desktop or headset mic, with programmable boost and gain
- Speakerphone : use of system mic & speakers for telephony, DSVD, and video conferencing
- Stereo line in : analog external line level source from consumer audio, video camera, etc.
- Video : TV tuner or video capture card with internal connections to codec mixer
- AUX/synth : analog FM or wavetable synthesizer, or other internal sources

3.1 - Mixer Output

The ST7597 mixer generates two distinct outouts :

- a stereo mix of all sources to LINE_OUT.
- a mono, mic only or mix of all sources (minus PHONE and PC_BEEP) for MONO_OUT.

3.2 - Mixer Input

The mixer input is a MUX design which offers the capability to record any of the audio sources or the outgoing mix of all sources. This design is more efficient to implement than an independant input mix, allows the user to apply 3D and tone controls to recording, and offers simple monitoring when a mix is recorded: what you hear is what you get (WYHIWYG). Mono and stereo mix also provide excellent echo cancelation reference signals.

ST7597 supports the full range of input options, tha audio driver should maintain a persistent record input level for each MUX inputs :

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input with mono output reference (mic + mono mix for mono echo cancellation)

FUNCTIONAL DESCRIPTION (continued)

3.3 - Mixer Registers

The register indexes and usage are shown below. All registers not shown and bits containing an X are assumed to be reserved.

	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	default
00h	Reset	x	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	na
02h	Master Volume	mute	x	-	ML4	ML3	ML2	ML1	ML0	x	x	-	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	mute	x	x	x	x	x	x	x	x	x	-	MR4	MR3	MR2	MR1	MR0	8000h
08h	Master Tone R&L	x	x	x	x	BA3	BA2	BA1	BA0	x	x	x	x	TR3	TR2	TR1	TR0	0F0Fh
0Ah	PC_BEEP Volume	mute	x	x	x	x	x	x	x	x	x	x	PV3	PV2	PV1	PV0	x	8000h
0Ch	Phone Volume	mute	x	x	x	x	x	x	x	x	x	GN5	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	mute	x	x	x	x	x	x	x	x	20dB	GN5	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line Input Volume	mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Output Volume	mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	x	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h
1Ch	Record Gain	mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	pop	x	3D	x	x	x	MIX	MS	LPB	x	x	x	x	x	x	x	0000h
22h	3D Control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0800h
26h	Powerdow n	x	x	x	PR4	PR3	PR2	PR1	PR0	x	x	x	x	REF	ANL	DAC	ADC	na
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
7Ah	Vendor Reserved	OSCpdn	x	x	x	x	x	x	x	x	x	x	TEST3	TEST2	TEST1	DD	x	8000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	na
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0	na

Notes : 1. Any reserved bits, marked x, can be written to but are stuffed with 0 upon read back.
2. PC_BEEP default value is set to 8000h, mute on.

FUNCTIONAL DESCRIPTION (continued)

3.3.1 - Reset Register (index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code for the part and the code for the type of 3D Stereo Enhancement supported.
All DACs operate at the same resolution. All ADCs operate at the same resolution.

bit = 1	Function	Value
ID0	Dedicated Mic PCM in channel	0
ID1	Modem Line Codec support	0
ID2	Bass&Treble control	1
ID3	Simulated Stereo (Mono to Stereo)	0
ID4	Headphone output support	0
ID5	Loudness (bass boost) support	0
ID6	18-bit DAC resolution	0
ID7	20-bit DAC resolution	0
ID8	18-bit ADC resolution	0
ID9	20-bit ADC resolution	0

For ST7597 a read of the 3D control register will return 0800h.

SE4..SE0	Function	Value
00000	No 3D stereo enhancement	00000
00001	Analog devices 3D stereo enhancement	
00010	Creative labs 3D stereo enhancement	
00011	National Semiconductor 3D stereo enhancement	
00100	Yamaha 3D stereo enhancement	
00101	BBE 3D stereo enhancement	
00110	Crystal Semiconductor 3D stereo enhancement	
00111	Q-sound QX (stereo enhancement)	
01000	Spatialized (stereo enhancement)	
01001	SRS (stereo enhancement)	

3.3.2 - Play Master Volume Registers (index 02h and 06h)

These registers manage manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels). Register 06h controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set to <-80dB. ML5 through ML0 is for the left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

The MSB of the level is not supported by this version of ST7597. When the MSB is set to 1 then the ST7597 will set the 5 LSBs to 1. Example: if the driver writes a 1xxxxx, the ST7597 will interpret that as x11111. It will also respond when read with x11111 rather than 1xxxxx, the value written to it. The driver can use this feature to detect if the 6th bit is there or nor.
The default value is 8000h, which corresponds to 0dB attenuation with mute on.

Mute	Mx5..Mx0	Function
0	00 0000	0dB attenuation
0	01 1111	46.5dB attenuation
0	1x xxxx	46.5dB attenuation
1	xx xxxx	<-80dB gain

3.3.3 - Master Tone Control Register (index 08h)

A tone function (treble-bass) is available in this chip, to use this function four external capacitors have to be used and have to be connected to the six pins provided (see block diagram/pinout/list of external components).

The characteristics of this function are described herebelow.

TR3..TR0 BA3..BA0	Gain/Attenuation in dB
0000	+10.5
0001	+09.0
0010	+07.5
0011	+06.0
0100	+04.5
0101	+03.0
0110	+01.5
0111	00.0
1000	-01.5
1001	-03.0
1010	-04.5
1011	-06.0
1100	-07.5
1101	-09.0
1110	-10.5
1111	bypass (default)

The default value is 0F0Fh, which corresponds to Bypass of Bass and Treble gain.

FUNCTIONAL DESCRIPTION (continued)

3.3.4 - PC Beep Register (index 0Ah)

This controls the level for the PC BEEP input. Each step corresponds to approximatively 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set to <-80dB.

The default value is 8000h, which corresponds to 0dB attenuation with mute on.

Mute	PV3..PV0	Function
0	0000	0dB gain
0	1111	45dB gain
0	xxxx	<-80dBdB gain

3.3.5 - Analog Mixer Input Gain Registers (index 0Ch - 18h)

This controls the gain/attenuation for each of the analog inputs. Each step corresponds to approximatively 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set to <-80dB.
Register 0Eh (Mic volume register) has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008h, which corresponds with 0dB gain with mute on.
The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

Mute	Gx4..Gx0	Function
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	<-80dB gain

3.3.6 - Record Select Control Register (index 1Ah)

Used to select the record source independently for right and left. See table for legend. The default value is 0000h, which corresponds to mic in.

SR2..SR0	Right Record Source
0	Mic
1	CD in (R)
2	Video in (R)
3	Aux in (R)
4	Line in (R)
5	Stereo mix (R)
6	Mono mix
7	Phone

SL2..SL0	Left Record Source
0	Mic
1	CD in (L)
2	Video in (L)
3	Aux in (L)
4	Line in (L)
5	Stereo mix (L)
6	Mono mix
7	Phone

3.3.7 - Record Gain Register (index 1Ch)

1Ch is for the stereo input. Each step corresponds to 1.5dB, +22.5dB corresponds to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channels is set < -80dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

Mute	Gx3..Gx0	Function
0	00000	0dB gain
0	1111	+22.5dBgain
1	xxxx	<-80dB gain

3.3.8 - General Purpose Register (index 20h)

This register is used to control several miscellaneous functions of the ST7597 component. Below is a summary of each bit and its function. The POP bit controls the PCM out 3D bypass path (the pre and post 3D PCM out paths are mutually exclusive). The MS bit controls the mic selector.

This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h which is all off. The LPB bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

Bit	Function
MIX	mono output select, 0 = mix, 1 = mic
MS	mic select, 0 = mic1, 1 = mic2
LPB	ADC/DAC loopback mode

3.3.9 - 3D Control Register (index 22h)

This register is not used by the 3D enhancement implemented in this version of ST7597. A write to this register has no effect and a read of this register will give a 0800h.

FUNCTIONAL DESCRIPTION (continued)

3.3.10 - Powerdown Control/Status Register (index 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a "1" indicating that the subsection is "ready". READY is defined as the subsection able to perform in its nominal state. When this register is written the bit value that come in on AC-link will have no effect on read only bits 0-7.
When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1 indicates that the AC-link and ST7597 control and status registers are in a fully operational state. The ST7597 controller must further probe this powerdown Control/Status register to determine exactly which subsections, if any, are ready.

Bit	Function
REF	Vref's up to nominal level
ANL	Analog mixer, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

The Power down modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADC's and DAC's only, PR6 and PR7 are not used.

Bit	Function
PR0	PCM in ADC's & input mux powerdown
PR1	PCM out DACs powerdown
PR2	Analog mixer powerdown (V_{REF} still on)
PR3	Analog mixer powerdown (V_{REF} off)
PR4	Digital interface (AC-link) powerdown (external clk off)
PR5	Internal Clock disable
PR6	Not used
PR7	Not used

3.3.11 - Reserved Registers (index 28h-58h)

These are reserved. Do not write to these registers.

3.3.12 - Vendor Reserved Registers (index 5Ah - 7Ah)

These are reserved for future use.
Do not write to these registers.

3.3.13 - Vendor Specific Test Register (index 7Ah)

This register is for Vendor Specific Test Mode.
Donot write to this register for normal use.

Osc PDN	TEST3	TEST2	TEST1	DD	Function
1	0	0	0	0	Normal mode (default)
1	x	x	x	1	DAC SDOUT = ADC SDIN
1	1	0	0	x	Digital loop back test
1	0	1	1	x	Analog loop back test
0	x	x	x	x	Oscillator set in powerdown mode (*)

Notes : The default value is 8000h.
Once the oscillator is in power down through the MSB bit, the AClink protocol can only be woken up by applying a negative pulse on RESET pin.

3.3.14 - Vendor ID Registers (index 7ch - 7Eh)

These registers, as shown below, contains the SGS-THOMSON Microelectronics Identification Code.

The ID method is Microsoft's Plug and Play Vendor ID code.

Reg	Default
7Ch	5354h
7Eh	4D02h

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Digital Power Supply	-0.3, 7.0	V
	Analog Power Supply	-0.3, 7.0	V
T_{oper}	Operating Ambient Temperature	0, +70	°C
T_j	Junction Temperature	+125	°C

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
DV_{DD}	Digital Power Supply	4.75	5	5.25	V
AV_{DD}	Analog Power Supply	4.75	5	5.25	V
I_{CC}	Power Supply Current in Normal Mode		55		mA
I_{CC}	Power Supply Current in Low Power Mode		50	100	µA

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DIGITAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage - TTL				0.8	V
V_{IH}	High Level Input Voltage - TTL		2.0			V
Schmitt Trigger TTL Hysteresis						
V_{OL}	Low Level Output Voltage				0.4	V
V_{OH}	High Level Output Voltage		2.4		Supply	V
I_{OH}	Logic 1 Output Current	V_{OH} = 2.4V			8	mA
I_{OL}	Logic 0 Output Current	V_{OL} = 0.4V			8	mA
C_{IN}, C_{OUT}	Pin Capacitance on Input and Output Pins (seen looking intothe chip)				10	pF
$I_{LATCHUP}$	Maximum Admissible Current per pin (latch-up)				±100	mA
V_{ESD}	Electrostatic Discharge Protection (ESD)		±2000			V

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Note : For more informations about all digital I/O refer to STKM5000 reference manual.

MASTER TONE CONTROL

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input Impedance for Treble Block	140	180		kΩ
	Input Impedance for Bass Block	30	38		kΩ
	Attenuation/Gain Step		1.5		dB
	Accuracy by Step	-0.5		+0.5	dB
	Bass Zero Frequency (68nF) (see Note 1)		350		Hz
	Treble Zero Frequency (2.2nF) (see Note 1)		2165		Hz
	Center Frequency (for 2.2nF and 68nF) (see Note 1)		950		Hz

Note 1 : Design information

ANALOG CHARACTERISTICS

Standard test conditions unless otherwise specified

T_{amb} = 25°C, AV_{DD} = DV_{DD} = +5V, V_{IL} = 0.8V, V_{IH} = 2.4V, 1kHz full scale input Sine wave,
Measurement Bandwidth is 10Hz-20kHz,
Sample Frequency = 48kHz, 10kΩ/50pF load, 0dB attenuation, tone and 3D disabled.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Full scale input voltage	0dB, all inputs 20dB boost, MIC inputs (1)		1.0 0.1		V_{RMS} V_{RMS}
	Full scale output voltage	0 dB		1.0		V_{RMS}
	Analog SNR CD to LINE OUT Other to LINE OUT		90	94 93		dB dB
	Digital SNR (2) DAC ADC		85 85	89 87		dB dB
	Total Harmonic Distortion + Noise (THD+N) (3)				0.02	%
	D/A & A/D Frequency Response	±0.25dB	20		18,050	Hz
	Transition Band		18,050		28,800	Hz
	Stop Band		28,800		Infinite	Hz
	Stop Band Rejection (4)		-74			dB
	Out-of-Band Rejection (5)			-40		dB
	Group Delay				1	ms
	Crosstalk between Channels Stereo Separation Inter-channel Isolation			 -85 -90	 -72 -72	 dB dB
	Spurious Tone Reduction			-100		dB
	Left/Right Channel Gain Mismatch				0.5	dB
	Input Signal Frequency Response		-1		1	dB
	Analog Input Impedance		20			kΩ
	Analog Input Capacitance			15		pF
	Power Supply Rejection Ratio	f = 1kHz	50			dB
	Output Load refered to Analog Ground (VMC)		10			kΩ
	Output Load for LINE OUT (C)				50	pF
V_{REFOUT}	Output Voltage			2.3		V
V_{REF1}, V_{REF2}	Output Voltage			2.3		V
V_{REFOUT}	Output Current Drive			5		mA
	Offset Voltage (6)			15	30	mV
	Delta Offset (7)				10	mV

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Notes : 1. With +20dB Boost On, 1.0V_{RMS} with Boost Off.
2. The ratio of the RMS output level with 1kHz full scale input to the rms output level with all zeros into the digital input. Measured with "A-weighted factor" over a 20Hz to a 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise-Ratio).
3. Analog specs. are based on a 1kHz, 0dB sine wave test signal.
4. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
5. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over 1 bandwidth 28.8 to 100kHz, with respect to a 1V_{RMS} DAC output.
6. Offset voltage refers to the deviation of the output from mid-scale with input shorted over the entire playback path. Offset from zero refer to the deviation of the output from mid-scale with input shorted over the entire recording path.
7. Delta offset refers to the variations in offset under different operating conditions, especially with different sampling rates & without re-calibration.

TIMING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
COLD RESET (see Figure 8)					
$t_{RST2CLK}$	RESET inactive to BIT_CLK startup delay	162.8			ns
t_{RES_LOW}	RESET Low Pulse Width	1.0			µs
WARM RESET (see Figure 9)					
$t_{SYNC2CLK}$	SYNC inactive to BIT_CLK startup delay	162.8			ns
$t_{SYNCHIGH}$	SYNC High Pulse Width		1.3		µs
ATE TEST MODE (see Figure 10)					
$t_{SETUP2RST}$	Setup to trailing Edge of Reset	15.0			ns
t_{OFF}	Rising edge of RESET to Hi_Z delay			25.0	ns
t_{RES_LOW}	RESET Low Pulse Width	1.0			µs

Figure 8

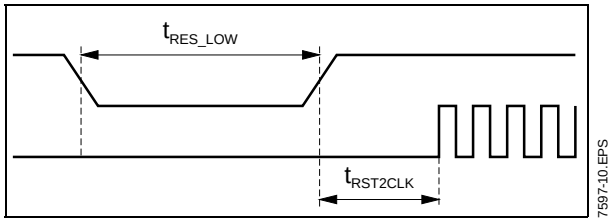


Figure 9

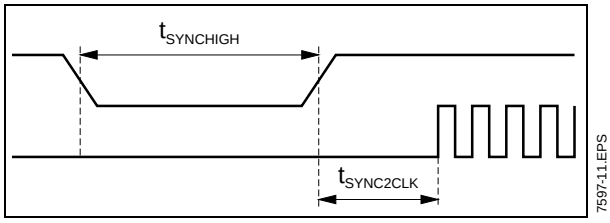
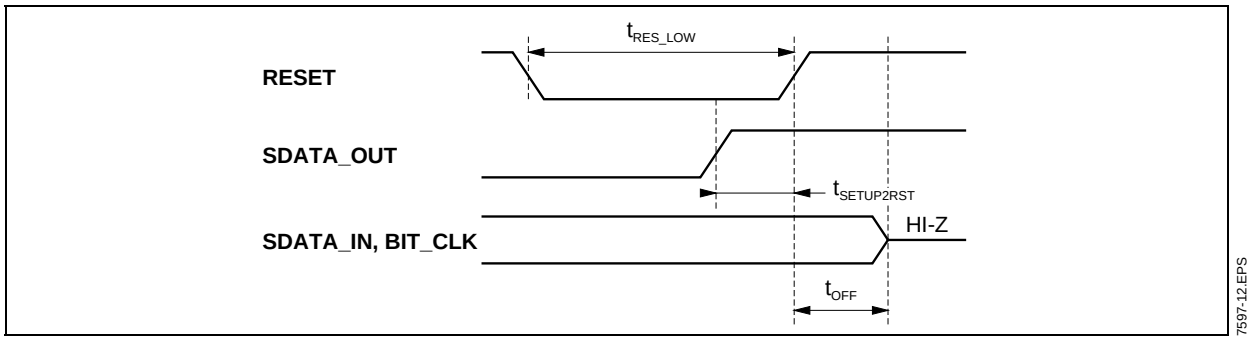


Figure 10



PARAMETER DEFINITIONS

THD+N : (Total Harmonic Distortion + Noise) is the ratio of the rms value of the input signal to the RMS sum of all other spectral components within the measurement bandwidth 10Hz to 20kHz). Units in %.

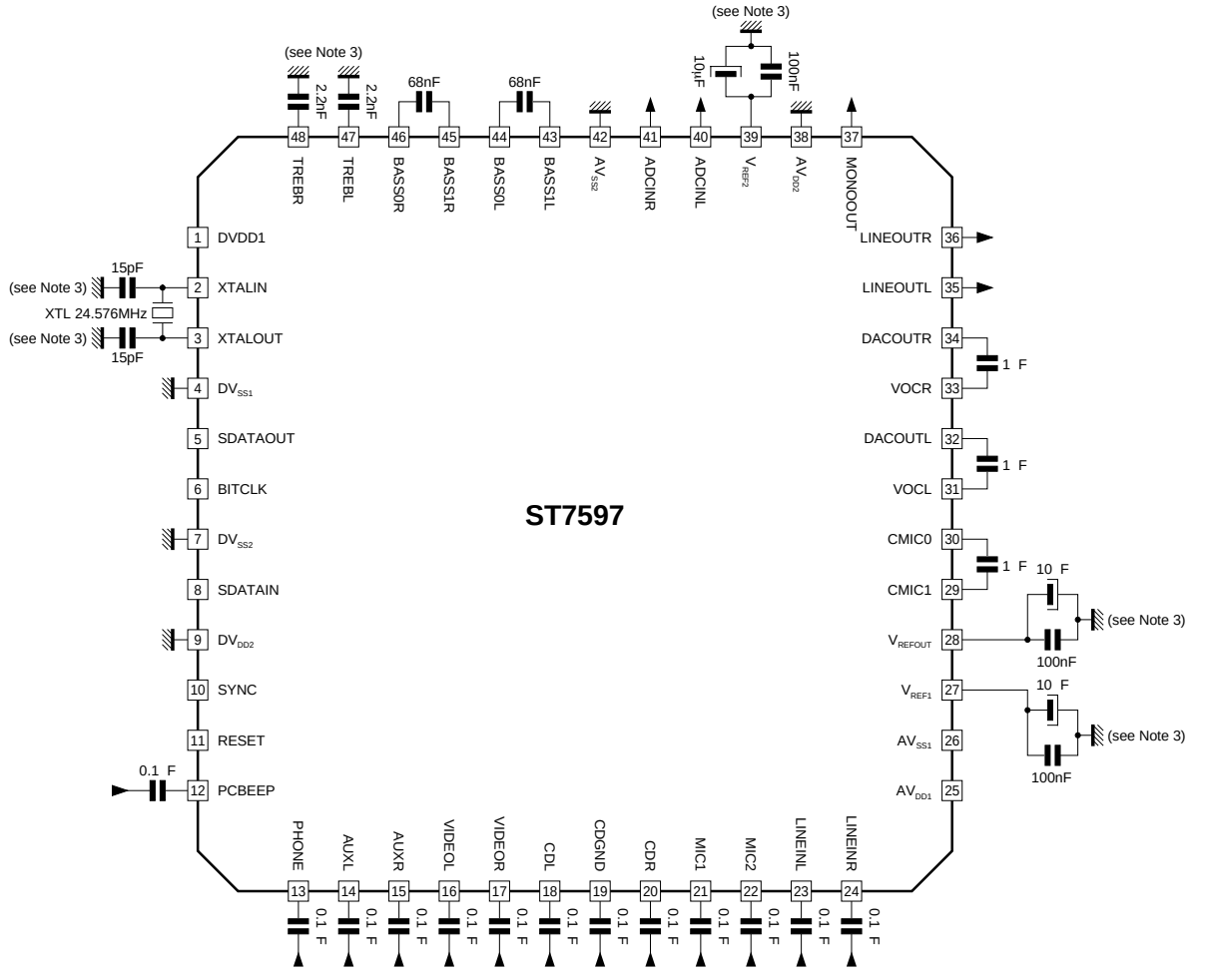
Dynamic Range : The THD+N with a 1kHz, -60dB input signal, with 60dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components of the noise to insignificance. Units in dB.

Signal to Noise : The ratio of the RMS output level with 1kHz full scale input to the rms output level with all zeros into the digital input. Measured with "A-weighted factor" over a 20Hz to a 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise-Ratio). Units in dB.

Signal to Peak Harmonics (-3dB) : The Signal to Peak Harmonics is the difference between the input signal (a 1kHz, -3dB input signal) to the peak of the harmonics components within the measurement bandwidth 10Hz to 20kHz. Units in dB.

Frequency Response : The worst case variation in output signal level versus frequency over 10Hz to 20KHz. Units in dB.

APPLICATION DIAGRAM

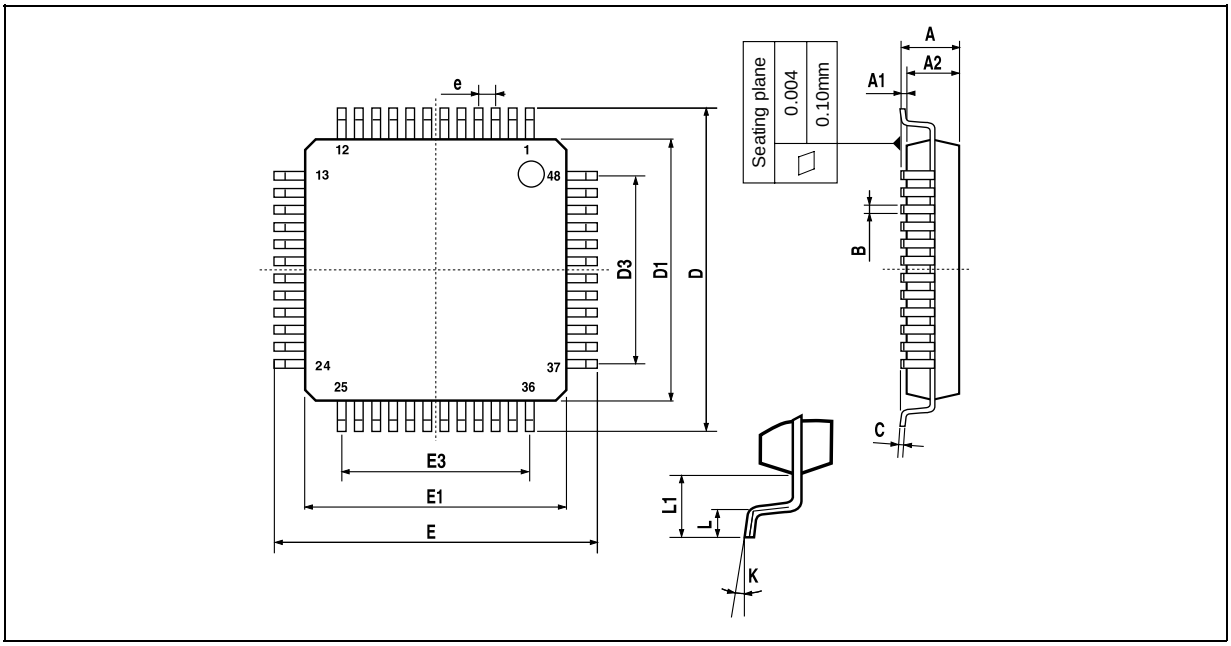


Notes : ***1. With 0.1 F > low cut-off frequency 50Hz (capacitor value to be increased)***
2. Requested decoupling capacitor
3. V_{SS} ground, as short as possible, start routing

7597-13.EPS

PACKAGE MECHANICAL DATA

48 PINS - THIN PLASTIC QUAD FLAT PACK (TQFP)



PMTQFP48.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.216	
e		0.50			0.0197	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.216	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

TQFP48.TBL