SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7544 - UNIVERSAL ANALOG FRONT-END

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SUMMARY **Page**

I - ST7544

I.1 - FEATURES

- FULL ECHO CANCELLING CAPABILITY
- FULLY COMPATIBLE WITH THE ST7543 (7543 mode)
- 16-BIT OVERSAMPLING A/D AND D/A CONVERTERS
  - Programmable down-sampling frequency from 7200 to 16000Hz
  - Sampling frequency can be 3, 4, 6, 8, 12, 16 x Symbol rate
  - Programmable Over sampling frequency (128 or 160 x Sampling frequency)
  - The ST7544 can work with external oversampling clocks
  - Programmable Symbol rate (600, 1200, 1600, 2400, 2560, 2743, 2800, 2954, 3000, 3200, 3429 and 3491)
  - Bit rates of 300 bps, 600bps, 1200 and all multiples of 2400 bps up to 28800 bps can be generated
  - Dynamic range : 92dB with a sampling frequency 9600Hz, Oversampling ratio 160
  - Total harmonic distortion : -89dB
- ON CHIP REFERENCE VOLTAGE
- THREE PROGRAMMABLE DIGITAL FILTERS SECTIONS :
  - Tx interpolation filter
  - Rx decimation filter
    Up to 14th order each
  - Rx reconstruction filter
    Coefficients loaded into RAM
- ANCILLARY CONVERTERS FOR EYE-DIAGRAM MONITORING
- CLOCK SYSTEM BASED ON DIGITAL PHASE LOCKED LOOPS
  - Separate Tx DPLL and Rx DPLL
  - Terminal clock input for Tx synchronization on all multiples of 2400Hz (V.Fast synchronization mode) or on sub-multiple of baud rate (7543 synchronization mode)
  - Bit, Baud, Sampling and Highest synchronous clock outputs
  - Maximum master clock frequency is 38MHz
- SINGLE OR DUAL SYNCHRONOUS SERIAL INTERFACE TO DSP
- SINGLE POWER SUPPLY VOLTAGE : +5V
- LOW POWER CONSUMPTION :
  - 260mW operating power at the nominal crystal frequency of 36.864MHz
  - 160mW operating power at the crystal frequency of 18.432MHz
  - Less than 5mW in the LOW-POWER RESET MODE
- 1.2MM CMOS PROCESS
- 44-PIN PLCC OR
  44-PIN TPQFP (1.4mm body thickness)

I.1 - GENERAL DESCRIPTION

The ST7544 is a single chip Analog Front-End (AFE) designed to implement high speed voice-grade Modems up to 28800 bps with echo cancelling capability.

Associated with one or several Digital Signal Processors (DSP), such as the ST189XX family, it provides a powerful solution for the implementation of multi-mode Modems meeting CCITT (V.21, V.22, V.22 bis, V.23, V.26, V.27, V.29, V.32,V.32 bis and V.33) and BELL (103, 202, 212A...) recommendations. It is fully compatible with the ST7543 in 7543 mode and is also well suited emerging applications involving bit rates up to 28800 bps (in the VFast synchronization mode).

The transmit section includes a 16-bit over-sampling D/A converter with a programmable interpolating filter. The receive section includes a 16-bit oversampling A/D converter with two programmable filters (one for decimation and the other for reconstruction). Oversampling ratio is selectable to either 128 or 160. Two additional 8-bit D/A converters allow eyediagram monitoring on a scope for modem performance adjustment.

Two independant clock generator systems are provided, one synchronized on the Tx rate and the other on the Rx rate.

In External Clock Mode, external oversampling clocks can be provided to the chip.

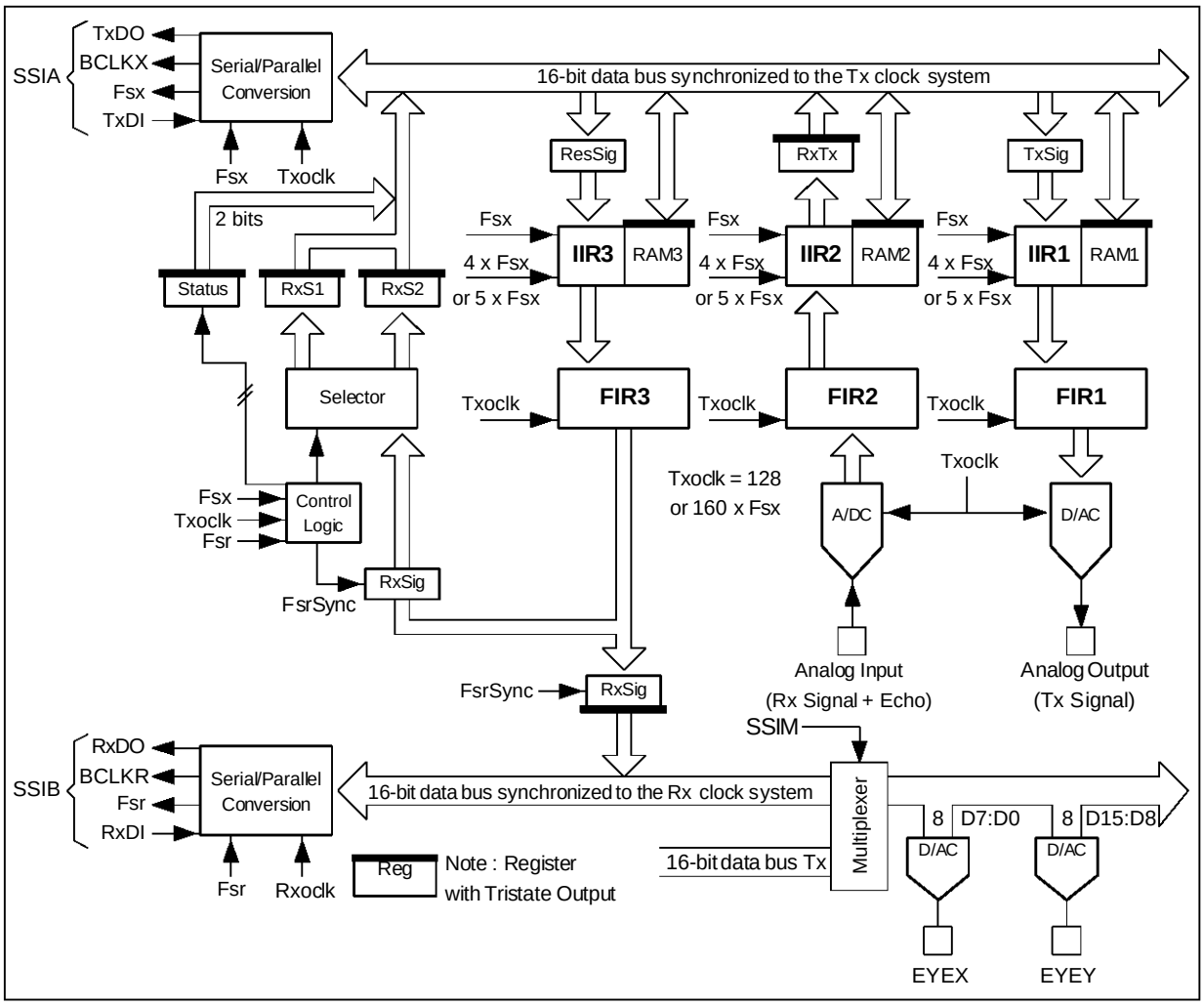
Two independant synchronous serial interfaces (SSI) allow several versatile ways of communicating with standard DSPs.

To save power, e.g. in lap-top modem applications, the lowpower reset mode can be used to reduce the power consumption to less than 5mW.

I.3 - SIGNAL TRANSFER BLOCK DIAGRAM

The ST7544 Block Diagram (Figure 1) illustrates three paths as follows : The Transmit D/A Section, the Receive A/D section and the Receive Reconstruction section.

Figure 1



I.4 - IIR FILTER OPERATION

Each IIR filtering section included in the ST7544 can perform up to seven biquadratic transfer functions in cascade, operating at four times the sampling frequency (see Figure 2).

Each biquad is defined by five coefficients, A, B, C, D and E (see Figure 3). An additional coefficient F, scales the IIR filter output.

Unused biquads are made transparent by programming A to one and the four remaining coefficients to zero. Such biquads should preferably be located in the first sections of the IIR filter in order to reduce the calculation noise.

I.4.1 - Coefficient Rounding

Initially, coefficients of the filter to be implemented must be exclusively between +2 and -2. To derive the actual usable 12+1 bit coefficients, the rounding process described in Figure 4 must be performed.

Each 13 bit coefficient K is split into its doubling factor K2, and its 12 bit basic value K1, as the IIR architecture works with 12 bit coefficients and uses an extra accumulation when coefficient doubling is needed.

$$K2 \in [0,1] \text{ and } -2^{12} < K1 < +2^{12}$$

The coefficients are loaded into the different IIR filters through 16 bit wide time slots. The format to be used is as follows :

MSB	K1	LSB
K2	(12-bit)	0 0 0
(1 bit)		(3-bit)

<--------- 16 bit word -------->

To programme one IIR filter it is necessary to send five words per biquad followed by two additional words set to zero and the F coefficient word :

B(1), C(1), A(1), D(1), E(1), B(2),..., E(7), 0000_H, 0000_H, F

The total number of words sent is therefore 38.

I.4.2 - Detailed Operation

The architecture of the device supporting the IIR filter is based on 28 bit data path. The basic function is as follows: one coefficient K(N) is multipled by one sample X(N) followed by one accumulation with value clampling. It can be precisely described as follows :

FUNCTION PAC K(N), X(N), S
LOCAL P
  P = **TRUNC** (K1(N) x X(N)/2^{12})
  S = S + P
  IF ABS(S) > 2^{27} **THEN**
    IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
    ELSE CLAMP S **TO** 2^{27}

  IF K2(N) = 1 **THEN** S = S + P
  IF ABS(S) > 227 **THEN**
    IF SIGN(S) > 0 **THEN CLAMP** S **TO** 2^{27}-1
    ELSE CLAMP S **TO** 2^{27}

END OF FUNCTION

The TRUNC function is a two's complement truncature.

As previously mentionned, the second accumulation is controlled by the doubling factor K2(N).

The complete process of computing 16 bit output samples (V_{OUT}) from 16 bit input samples (V_{IN}) appears in Figure 5.

Figure 2 : IIR Filter Diagram

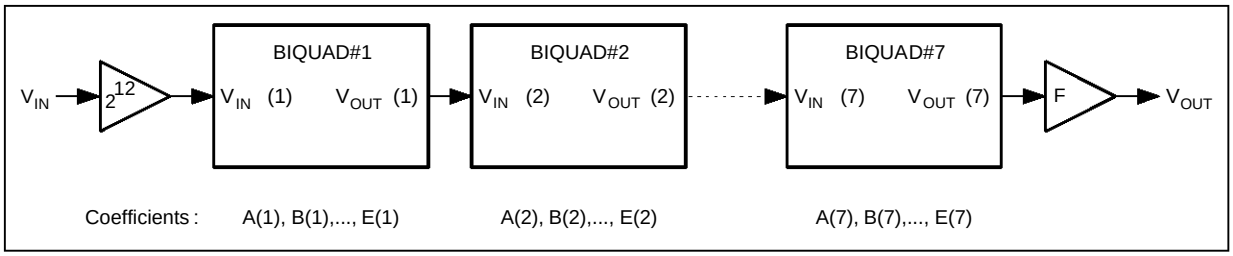
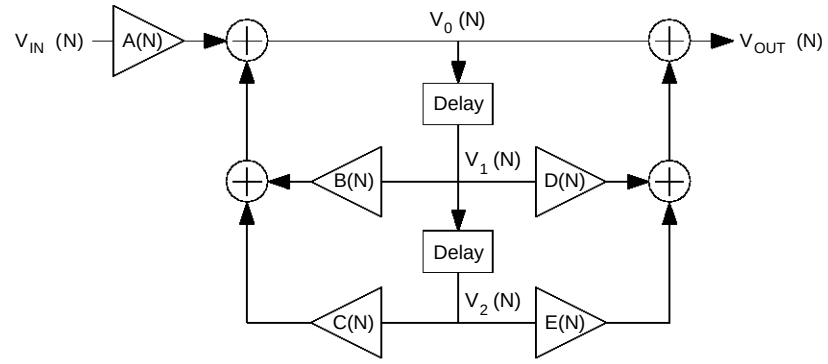


Figure 3 : BIQUAD Structure



$$Hn(Z) = A\frac{1 + DZ^{-1} + EZ^{-2}}{1 - BZ^{-1} - CZ^{-2}}$$

Equation Set : $V_0(N) = B(N) \times V_1(N) + C(N) \times V_2(N) + A(N) \times V_{IN}(N)$ N = BIQUAD NUMBER (1:7)

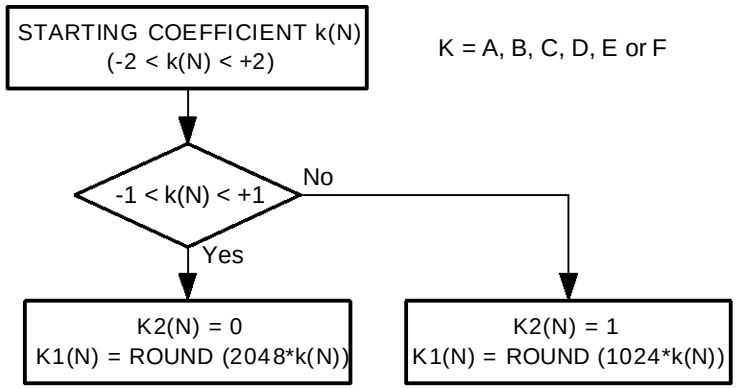
$V_{OUT}(N) = V_0(N) + D(N) \times V_1(N) + E(N) \times V_2(N)$

Next Step with : $V_2(N) = V_1(N)$

$V_1(N) = V_0(N)$

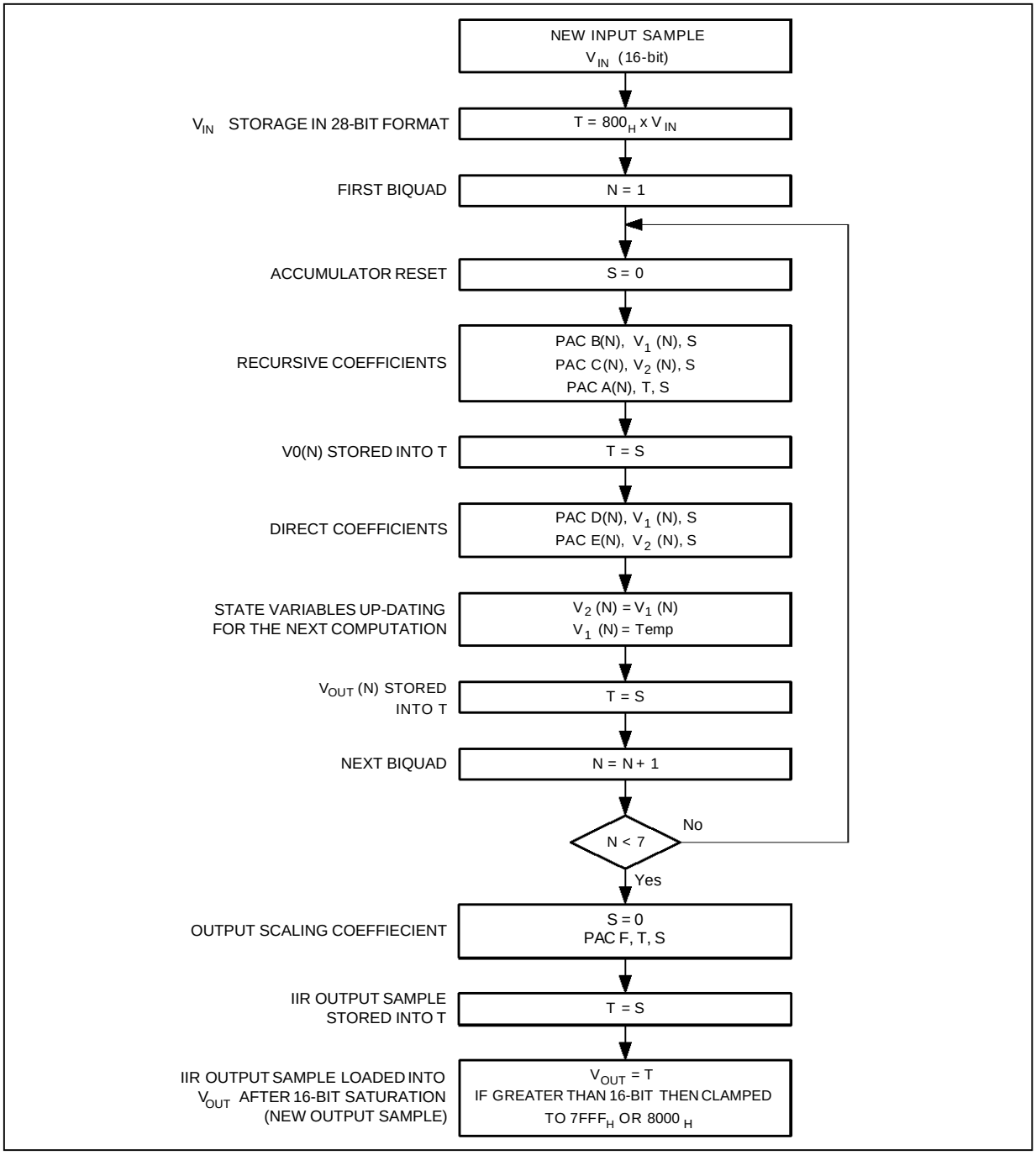
7544-23.EPS

Figure 4 : IIR Coefficients Rounding



7544-24.EPS

Figure 5 : IIR Operating Sequence



I.5. - IIR FILTER PROGRAMMING EXAMPLE

I.5.1 - Example of Configuration

- one external clock : 36.864MHz
- serial port mode : dual
- transmit sampling frequency : 9600Hz
- receive sampling frequency : 9600Hz
- bit frame clock frequency : 160*Fsx(r)
- transmit bit clock frequency : 14400Hz
- receive bit clock frequency : 14400Hz
- transmit baud clock frequency : 2400Hz
- receive baud clock frequency : 2400Hz
- transmit filter : low-pass (spec table 48)
- receive filter : banp-pass spec table 50)
- interpolation filter : low-pass (spec table 43)

I.5.2 Hardware Configuration

- XTAL10 and XTAL11 hard-wired to the external clock
- TxDI and RxDI must be tied to Vdd while the serial interface is not managed by the host processor.
- RC network on NLPR pin.Typically RC=10ms (R=100kΩ ,C=100nF) (This time must include the external clock start-up time,and the ST7544 set up time).
- SSIM pin tied to DV_{DD} : dual serial port mode.
- BFRS pin tied to DV_{DD} : bit frame frequency set to 160 time Fsx(r).

I.5.3 - Software Configuration

Writing convention :

'x'	frame number
FRAME x,1	frame for RAM 1 loading
FRAME x,2	frame for RAM 2 loading
FRAME x,3	frame for RAM 3 loading
'#"	delimits a programmer's remark (comments)
'b'	indicates a binary number
'h'	indicates an hexadecimal number
'XXXX'	user defined

 # SYNCHRONOUS SERIAL INTERFACE A

```
#FRAME 0.1. Select the correct sampling frequency and set Stb bit in order to select a RAM
B9A4h #TxI0     MS =1       coefficient loading mode selected
#               Stb=0       start bit coefficient loading activated
#               QS =1       XTAL 10 selected
#               RAi=11b     no RAM accessed
#               ADi=001b    TxCR1 selected
#               Di =A4h     Fsx=9600Hz, Txrclk=2400Hz
#                           TxHSCLK=12.288MHz
#                           Band split mode inactive
FFFFh#TxI1
FFFFh#TxI2
FFFFh#TxI3
#
#FRAME 1.1 Select RAM 1 and start the coefficient loading of the low-pass filter,and select TxCLK
E0F1h#TxI0      MS =1
#               stb=1
#               QS =1
#               RAi=00b     RAM 1 selected.
#               ADi=000b    TxCR0 selected.
#               Di =F1h     TxCLK = 14400Hz
FFFFh#TxI1      unused
0000h#TxI2      word 1 RAM 1 ( first IIR coefficient)
0000h#TxI3      word 2 RAM 1
#
FRAME 2.1 RAM 1 coeff loading,fcomp and fshift prog and Stb ready to select another RAM
A340h #TxI0     MS =1
#               stb=0
#               QS =1
#               RAi=00b     RAM 1 selected.
#               ADi=011b    TxCR3 selected.
#               Di =40h     fcomp = 2400Hz, fshift=Fsx/2
A000h #TxI1     word 3 RAM 1
0000h #TxI2     word 4 RAM 1
0000h #TxI3     word 5 RAM 1
#
#
#FRAME 3.1 RAM 1 coefficient loading, no control register access
A7FFh #TxI0
B7D8h #TxI1     word 6 RAM 1
42B0h #TxI2     word 7 RAM 1
0118h #TxI3     word 8 RAM 1
#
#FRAME 4.1 to 12.1 RAM 1 coefficient loading, no control register access
A7FFh #TxI0
XXXXh
XXXXh
XXXXh
```

```
#FRAME 13.1 Last RAM 1 loading frame
A7FFh #TxI0
0000h #TxI1      word 36 RAM 1
0000h #TxI2      word 37 RAM 1
0008h #TxI3      word 38 RAM 1
#
#
#RAM 2 COEFFICIENT LOADING
#FRAME 1.2 Select RAM 2 and start the coefficient loading of BP filter
EFFFh #TxI0      MS =1
#                Stb=1
#                QS =1
#                RAi=01b     RAM 2 selected
#                ADi=111b
FFFFh #TxI1      unused
0000h #TxI2      word 1 RAM 2
0000h #TxI3      word 2 RAM 2
#
#FRAME 2.2 RAM 2 coefficient loading,no control register access and rest Stb
AFFFh #TxI0      MS =1
#                Stb=0
#                QS =1
#                RAi=01b     RAM 2 selected
#                ADi=111b
A000h #TxI1      word 3 RAM 2
0000h #TxI2      word 4 RAM 2
0000h #TxI3      word 5 RAM 2
#
#FRAME 13.2 Last RAM 2 loading frame
A7FFh #TxI0
0000h #TxI1      word 36 RAM 2
0000h #TxI2      word 37 RAM 2
0008h #TxI3      word 38 RAM 2
#
#
#
#RAM 3 COEFFICIENT LOADING
#FRAME 1.3 select RAM 3 and start coeff loading
F7FFh #TxI0      MS =1
#                Stb=1
#                QS =1
#                RAi=10b     RAM 3 selected
#                ADi=111b
FFFFh #TxI1      unused
0000h #TxI2      word 1 RAM 3
0000h #TxI3      word 2 RAM 3
#
#
```

```
#FRAME 2.3 RAM 3 coefficient loading,no control register access and rest Stb
#
#
B7FFh #TxI0
A000h #TxI1     word 3 RAM 2
0000h #TxI2     word 4 RAM 2
0000h #TxI3     word 5 RAM 2
#
#
#FRAME 3.3 to 12.3 RAM 3 coefficient loading, no control register access
B7FFh #TxI0
XXXXh
XXXXh
XXXXh
#
#
#FRAME 13.3 Last RAM 3 loading frame
B2C4h #TxI0     MS =1
#               Stb=0
#               QS =1
#               RAi=10b     RAM 3 selected
#               ADi=010b    TxCR2 selected
#               Di =C4h     0dB attenuation on XMIT channel and synchronize the TxCLK clock on
                            TxRCLK
0000h #TxI1     word 36 RAM 2
0000h #TxI2     word 37 RAM 2
0008h #TxI3     word 38 RAM 2
#
#
# FRAME 14
3FFFh #TxI0     MS =0       Data mode
#               Stb=0       ready to read ram
#               QS =1
#               RAi=11b     No RAM access
#               ADi=111b    No Control register access
XXXXh #TxI1     Txsig
XXXXh #TxI2     Ressig
XXXXh #TxI3     unused
#
#
```

 # SYNCHRONOUS SERIAL INTERFACE B

```
#
#FRAME 0. Select the correct sampling frequency
01A4h #TrI0      ADi=001b   RxCR1 selected
#                Di =A4h    Fsr=9600Hz, Rxrclk=2400Hz
#                           RxHSCLK=12.288MHz
FFFFh #TrI1
FFFFh #TrI2
FFFFh #TrI3
#
#FRAME 1. Select the correct receive bit clock (RxCLK) frequency
00F1h #TrI0      ADi=000b   RxCR0 selected
#                Di =F1h    RxCLK=14400Hz
FFFFh #TrI1
FFFFh #TrI2
FFFFh #TrI3
#
#FRAME 2. No phase shift selected
0200h #TrI0      ADi=010b   RxCR2 selected
#
#                Di =00h    no phase shift
FFFFh #TrI1
FFFFh #TrI2
FFFFh #TrI3
#
#
#FRAME 3. select interpolation factor
0340h #TrI0      ADi=011b   RxCR3 selected
#                Di =40h    interpolation factor = 160
FFFFh #TrI1
FFFFh #TrI2
FFFFh #TrI3
#
#
#FRAME 4
FFFFh #TrI0      ADi=111b   no control register access
XXXXh #TrI1      EYEX-EYEY
FFFFh #TrI2      reserved
FFFFh #TrI3      reserved
#
#
```

I.6 - FILTER COEFFICIENT CODING IN ST7544 TIME-SLOT FORMAT

I.6.1 FILTER CHARACTERISTICS

Type	:	band-pass filter
Order	:	11
Sampling frequency	:	9.6kHz*5 = 48kHz
passband edge HP	:	300Hz (3dB , butterworth)
stopband edge HP	:	200Hz
stopband loss HP	:	8dB
passband edge LP	:	3200Hz (Cauer)
stopband edge LP	:	4200Hz
stopband loss LP	:	60dB
passband ripple	:	0.1dB
coefficient wordlength	:	11 bits + sign

I.6.2 - Filter Coefficients Table

B	C	A	D	E
0	0	0.9	- 1	0
0.9614815	0	0.8414686	- 1	0
1.706978	- 0.7952128	0.1985583	- 1	0
1.959984	- 0.961496	0.1774637	- 1.33996	1
1.675779	- 0.7113152	0.0346	0.35224561	1
1.747247	- 0.8925031	0.1021413	- 1.698336	1
1.789548	- 0.967721	0.4543867	- 1.627507	1
0	0	0.0025201	0	0

I.6.3 - Coefficient Coding in ST7544 Time-slot Format

Example of subroutine to code the coefficients in the ST7544 time-slot format.

```
SUB CODE(A(),NbBiquad,AA())
LOCAL i,EXTRABIT()
  FOR i=1 TO NbBiquad
     IF ABS(A(i))=1 THEN
        EXTRABIT(i)=-32768
        AA(i)=CINT((A(i)/2)*2048)
     ELSE
        EXTRABIT(i)=0
        AA(i)=CINT(A(i)*2048)
     END IF
        AA(i)=(AA(i)<3)AND 32767
        AA(i)=(AA(i) OR EXTRABIT(i))
     NEXT
END SUB
```

with :

INPUT :
NbBiquad number of biquadratic function.
A() Coefficient in decimal format

OUTPUT:
AA() Coefficient in ST7544 time-slot format.

writing convention:
ABS() return an absolute value
CINT() convert its argument to an integer.
(if the fractional part of an argument is equal to 0.5, it is rounded toward the even number).

≤ **n** left shift of n bit.

Note : It is not possible to code -1 or 1 , we therefore do as following
+1 = 2 * +0.5
-1 = 2 * -0.5
So IT IS NOT POSSIBLE TO CODE +/- 2

Filter table in Hexadecimal format.

B	C	A	D	E
000	0000	3C88h	E000h	0000
3D88h	0000	37E0h	E000h	0000
B6A0h	4D18h	CE0h	E000h	0000
BEB8h	4278h	B58h	C9A8h	A000h
B940h	4210h	E68h	CBE8h	A000h
B7E8h	46E0h	F98h	D520h	A000h
B5A0h	5278h	238h	1690h	A000h
0000	0000	20H	0000	0000

I.6.4 - Transfer Function

Figure 6

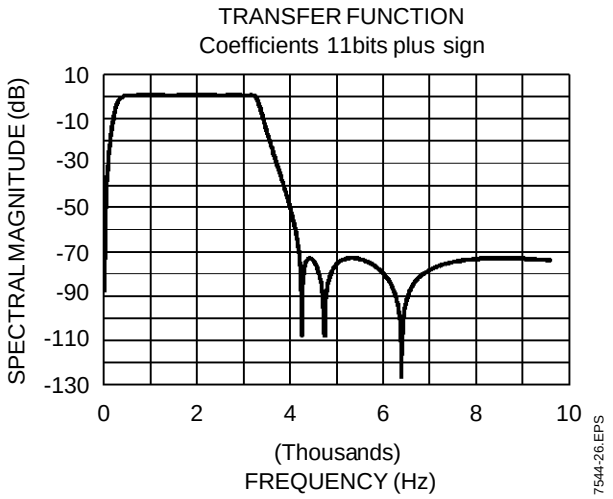


Figure 7

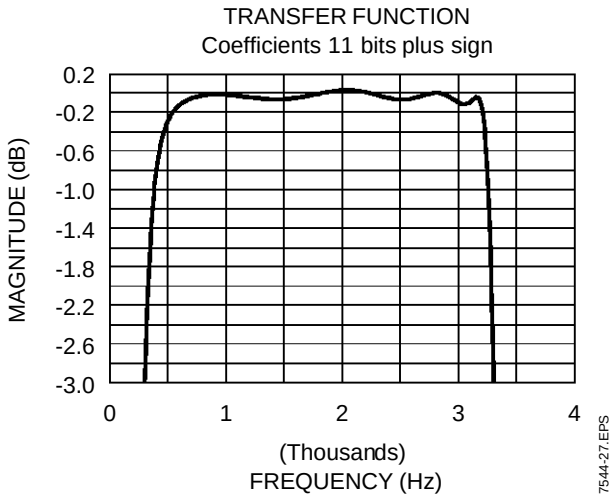
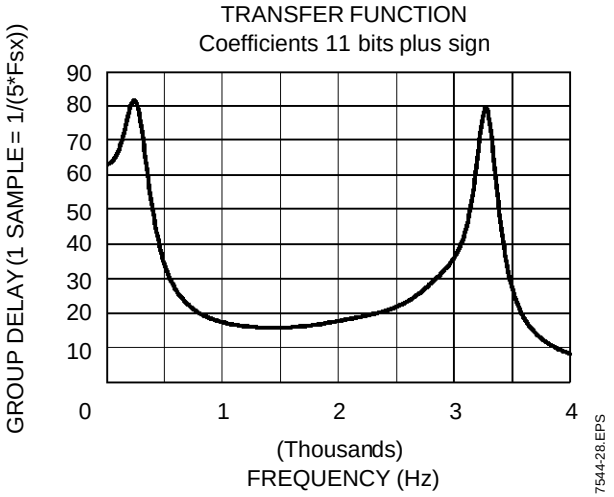


Figure 8



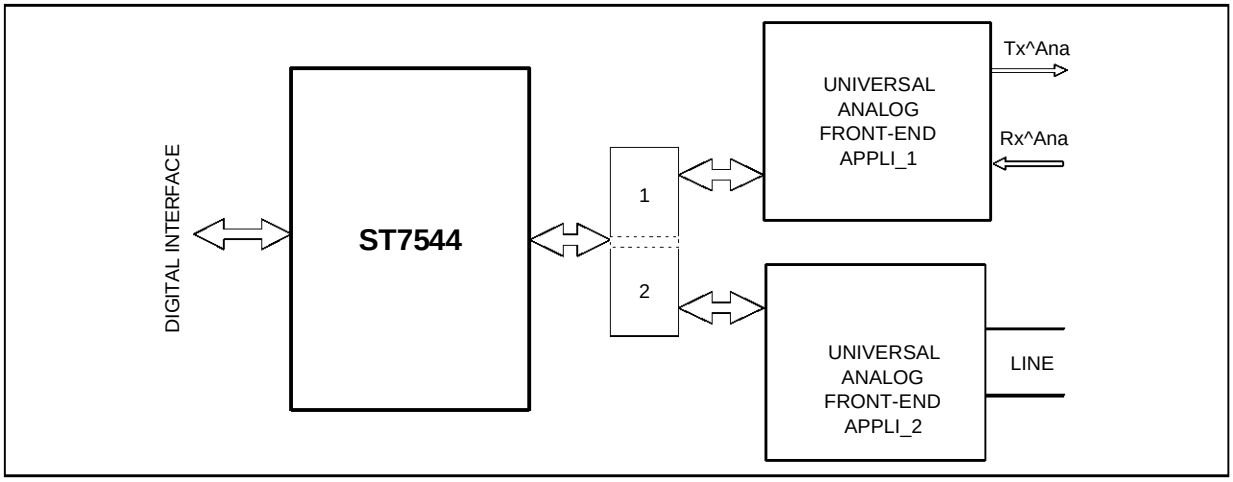
II - ST7544 APPLICATION BOARD

The ST7544 application board will give you a powerful analog front-end evaluation/development tool.

Two applications are available on board :

- Appli 1 : Analog front-end,
- Appli 2 : Modem analog front-end.

Figure 9



- Digital interface gives all necessary signals in order to control and program the ST7544.
- The Digital interface connector is fully compatible with **ST18933** development tools.
- Functionality with 2 crystals available on board,
- Eye diagram monitoring,
- Single-ended application.
- Full differential duplexer application.

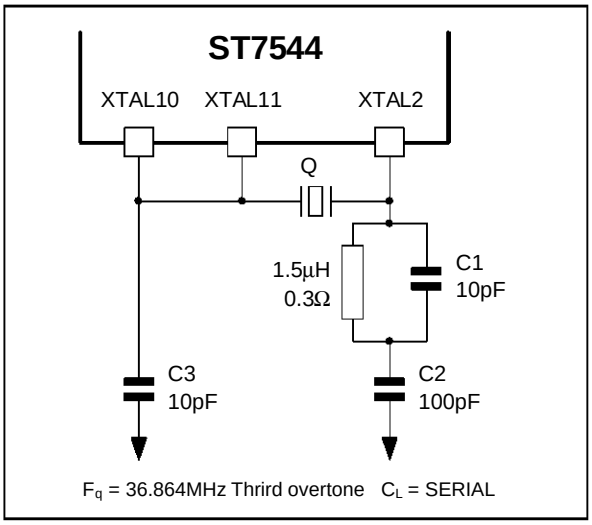
II.1 - CRYSTAL OSCILLATOR

XTAL10 and XTAL11 inputs must be tied to external crystal(s) or external clock(s).These inputs are selected from the TxCtrl register.The maximum clock rate is 38MHz.XTAL10 is the default external clock/crystal input.It is mandatory to short-circuit XTAL10 and XTAL11 when a single external crystal or clock generator is used.The nominal master clock frequency is 36.864MHz but the onchip amplifier is designed for a parallel crystal oscillator with a frequency equal to 18.432MHz.

XTAL2 output is to be tied to one or two external crystal (Figures 10 and 11). If an external clock is used, XTAL2 should be left open.

II.1.1 - Single Crystal Oscillator

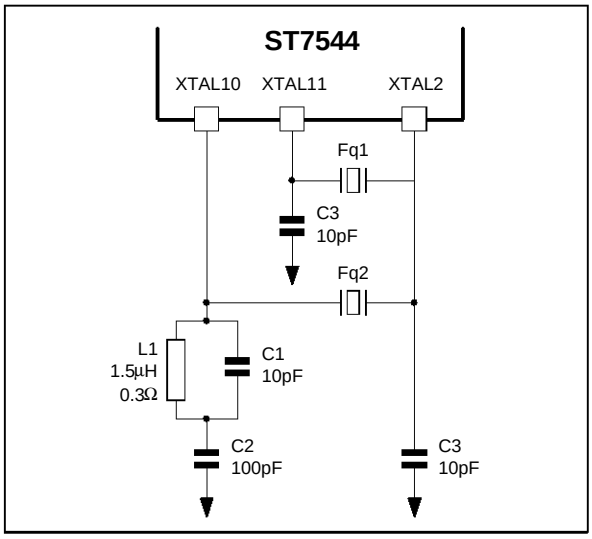
Figure 10



Operating range : 0 - 70 deg, 5V ± 5%
Start-up : Max. = 10mS
Typ. = 3.7 mS

II.1.2 - Double Crystal Oscillator

Figure 11



Operating range : 0 - 70 deg, 5V ± 5%
Start-up : Max. = 10mS
Typ. = 1.5 mS

II.1.3 - Quartz Specification

When you order a quartz, you have to specify the following parameters :
- Nominal frequency (e.g 36.864MHz ,25.848MHz)
- MODE (3rd overtone, Fundamental)
- Load capacitance (SERIAL, 30pF)
- Frequency tolerance (50 ppm from 0 to 70°C)

II.2 - APPLICATION 1 (single-ended)

II.2.1 - Transmit

The transmit part is a differential single-ended with low-pass filter realised by R6//C12 and R7//C13.The resistors R6 and R7 must be equal as must the capacitor C12 and C13.

The 3dB cut-off frequency of the 1st order filter inside the ST7544 is :

$$Fc = TxOCLK / (2 \cdot \pi \cdot 10)$$

E.g : 1st LP : Fsx = 7.2kHz over=4
then Fc = 14.7kHz
2nd LP : R =15kΩ C=680pF
then Fc = 15.6kHz

As the transfer function of the filters are known,the digital signal can be compensated if needed.

The C14=1µF gives on BNC J5 a signal referenced to AGND.

II.2.2 - Receive

The receive part is single-ended to differential.There is a low-pass filter realised by R13,R14 and C16.

Fc = 1 / (2 * PI * 1.2E03 * 2E-12) = 66kHz

Having a Fc at 66kHz, we have a flat transfer function in working Band (0-4kHz).

We DO NOT recommend the use of OP-AMP based filter as OP-AMP will present high impedance at high frequencies.This low-pass filter **must be implemented as close as posssible to the pins RxA1 and RxA2.**

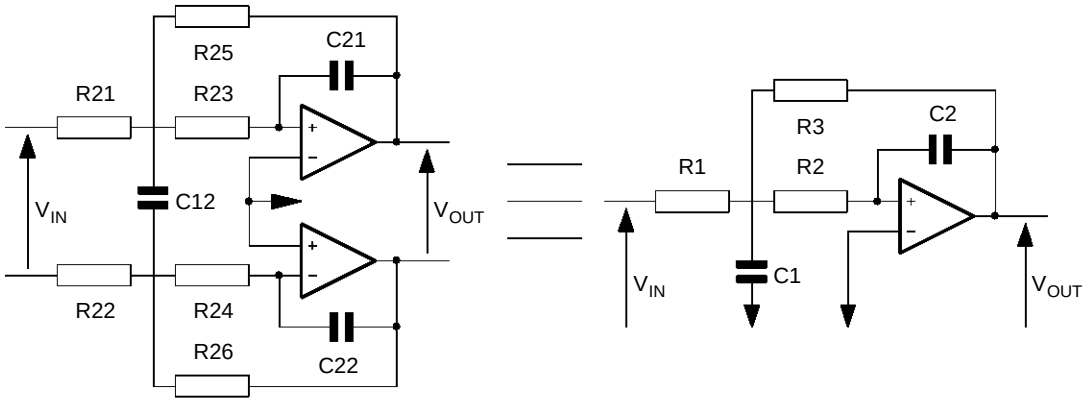
II.3 - APPLICATION 2 (duplexer)

II.3.1 - Transmit

We have a full differential low-pass filter on transmit the side before the DAA (see Figure 12)

R1 = R21 = R22 = 13.2kΩ
R2 = R23 = R24 = 22kΩ
R3 = R25 = R26 = 22kΩ
C1 = 2 * C12 = 2*680pF = 1360pF
C2 = C21 = 100pF
Fc = 19.6kHz
Ao = - R3/R1 = -1.66
X = 5 - Q= 0.1

Figure 12



$$F_C = \frac{1}{2 \cdot \pi \cdot \sqrt{R2 \cdot R3 \cdot C1 \cdot C2}}$$

$$Q = \frac{1}{2 \cdot X}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R3}{R1} \cdot \frac{1}{1 + \left(R2 + R3 + \frac{R2 \cdot R3}{R1} \right) \cdot C2 \cdot P + R2 \cdot R3 \cdot C1 \cdot C2 \cdot P^2}$$

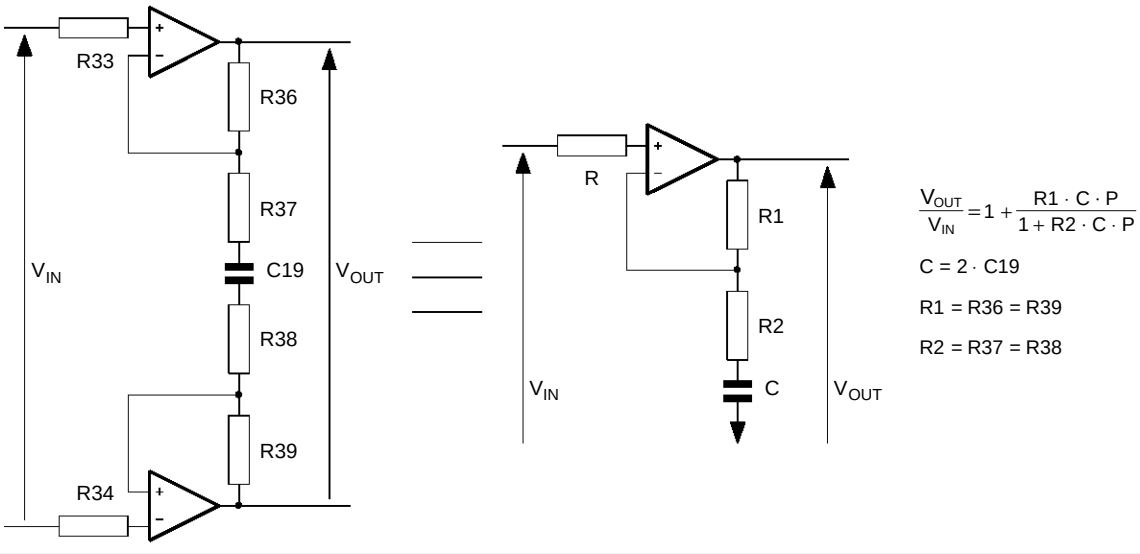
$$X = \frac{1}{2\sqrt{2}} \cdot \left[\sqrt{\frac{R2}{R3}} + \sqrt{\frac{R3}{R2}} + \sqrt{\frac{R2 \cdot R3}{R1}} \right] \cdot \sqrt{\frac{C2}{C1}}$$

7544-32.EPS

II.3.2 - Receive

We have 2 filters as in application 1 (LPF, Fc = 66kHz) and describe below (DC offset suppress, Fc = 85Hz)

Figure 13



$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R1 \cdot C \cdot P}{1 + R2 \cdot C \cdot P}$$

$C = 2 \cdot C19$

$R1 = R36 = R39$

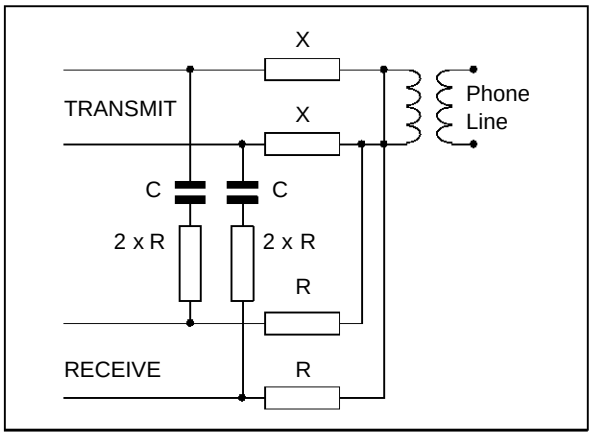
$R2 = R37 = R38$

7544-33.EPS

II.3.3 - Duplexer

R,C : Improves the low frequency response. These values depend on the transfer function of the transformer. Filter transfer function realised by R,C must compensate for the loss in transformer at low frequency.

Figure 14



Z0 : Nominal line impedance.(e.g : Z0 = 600Ω)

TRANSFO : M = 1 , Rs = Rp = 100Ω

$2 * X = Z0/M^2 - Rp - Rs/M^2$

2 * X = Z0 - 2 * Rp = 600 - 200 = 400

X = 200Ω

II.4 - PERFORMANCE MEASUREMENT

II.4.1 - Configuration

The following measurements have been made with ST7544 application board on application (1) with crystal 36.864MHz. The analog transmit signal (J5) is connected to analog receive signal (J4).

The IIR1 filter (low-pass) file is the following :

FFFF	0000	0000	A000	0000	0000
B7D8	42B0	0118	CA08	A000	B570
48A0	2838	CB68	A000	B268	5070
3508	CFA0	A000	AED8	59D0	2898
DD90	A000	AC18	6118	07A0	3368
A000	ADF0	5338	0858	4098	A000
0000	0000	0008			

The IIR2 and IIR3 filter (band-pass filter) files are the following :

FFFF	0000	0000	3C88	E000	0000
3D88	0000	37E0	E000	0000	B6A0
4D18	0CE0	E000	0000	BEB8	4278
0B58	C9A8	A000	B940	4210	0E68
CBE8	A000	B7E8	46E0	0F98	D520
A000	B5A0	5278	0238	1690	A000
0000	0000	0020			

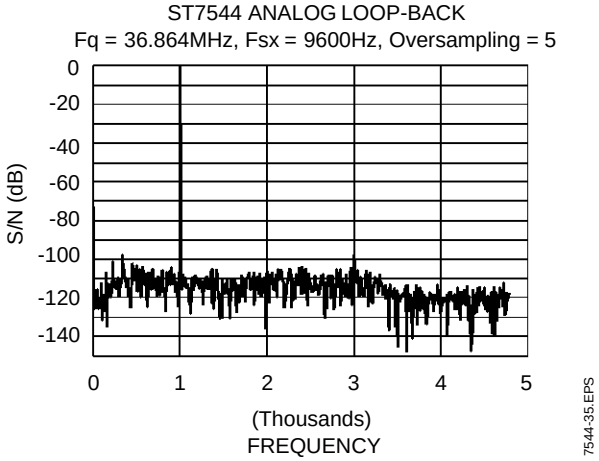
The control registers are programmed as following :

F9A4	TxCR1	M*Q=4*6 U=4 P0=3 and BS=0, Fsx = 9600Hz, Symbol rate = 2400 baud, Txhsclk = 12.288MHz, Band split Mode inactive
F8F1	TxCR0	NRST=F1h, Bit rate clock frequency = 14400Hz
FB40	TxCR3	V=010b , W=0 , Ts=000 , DL=0, Fcomp = Txrclk, Oversampling ratio = 160, Phase shift freq (Fsx/2 (Fq ± Fsx/2))normal mode
FAC4	TxCR2	AT=11b, LTX=0, LC=0, SST=0, VF=0, R2=0, attenuation = 0dB, mode 7543, synchronize TxCLK on TxRCLK, Normal mode synchronization
01A4	RxCR1	idem TxCR1
00F1	RxCR0	idem TxCR0
0200	RxCR2	no phase shift
0340	RxCR3	V = 160 - Interpolation ratio

II.4.2 - Measurement

We generate a digital sinewave of 1003.125Hz (1024 samples). This signal is sent to Txsig. Then we do a FFT (1024 samples) on the digital receive signal RxTx.

Figure 15



We have S/N = 84.43 dB. The band noise is double because of analog loop-back ,so if we want to calculate the dynamic range of the ST7544 ,we add 3dB to the S/N.

S/N = 84.43+3 = 87.43 dB at Signal = -6.13dBr

S/N = 87.43 + 6.13 = **93.56dB = DYNAMIC**

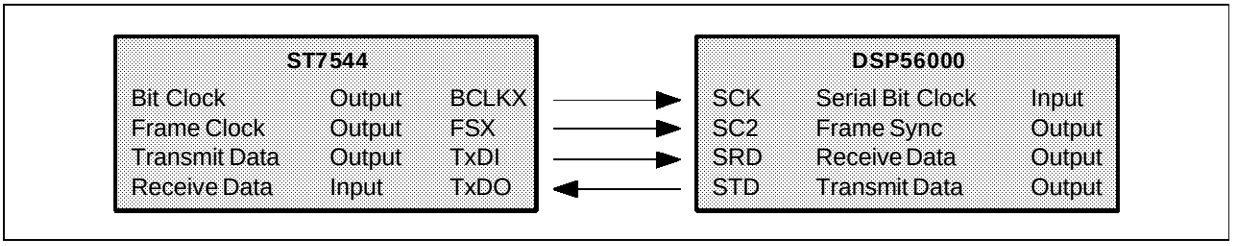
S/N = 6.02 * Nbit + 1.76

Nbit = (93.56-1.76)/6.02 = **15.25 bits**

III - INTERFACING ST7544 WITH DSP56000 (MOTOROLA)

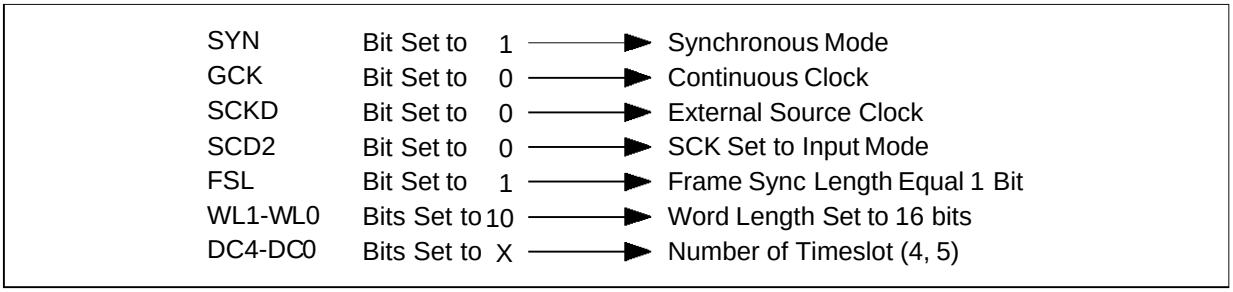
You will find below a suggested interface of our ST7544 with DSP56000 series from Motorola. We use the ST7544 in single SSI. The different connection are as following :

Figure 16



The DSP56000 control register bit has to be configured as following :

Figure 17



And you have to program the DSP in Network mode.

ANNEXE 1 : Demoboard Schematics

Figure 18

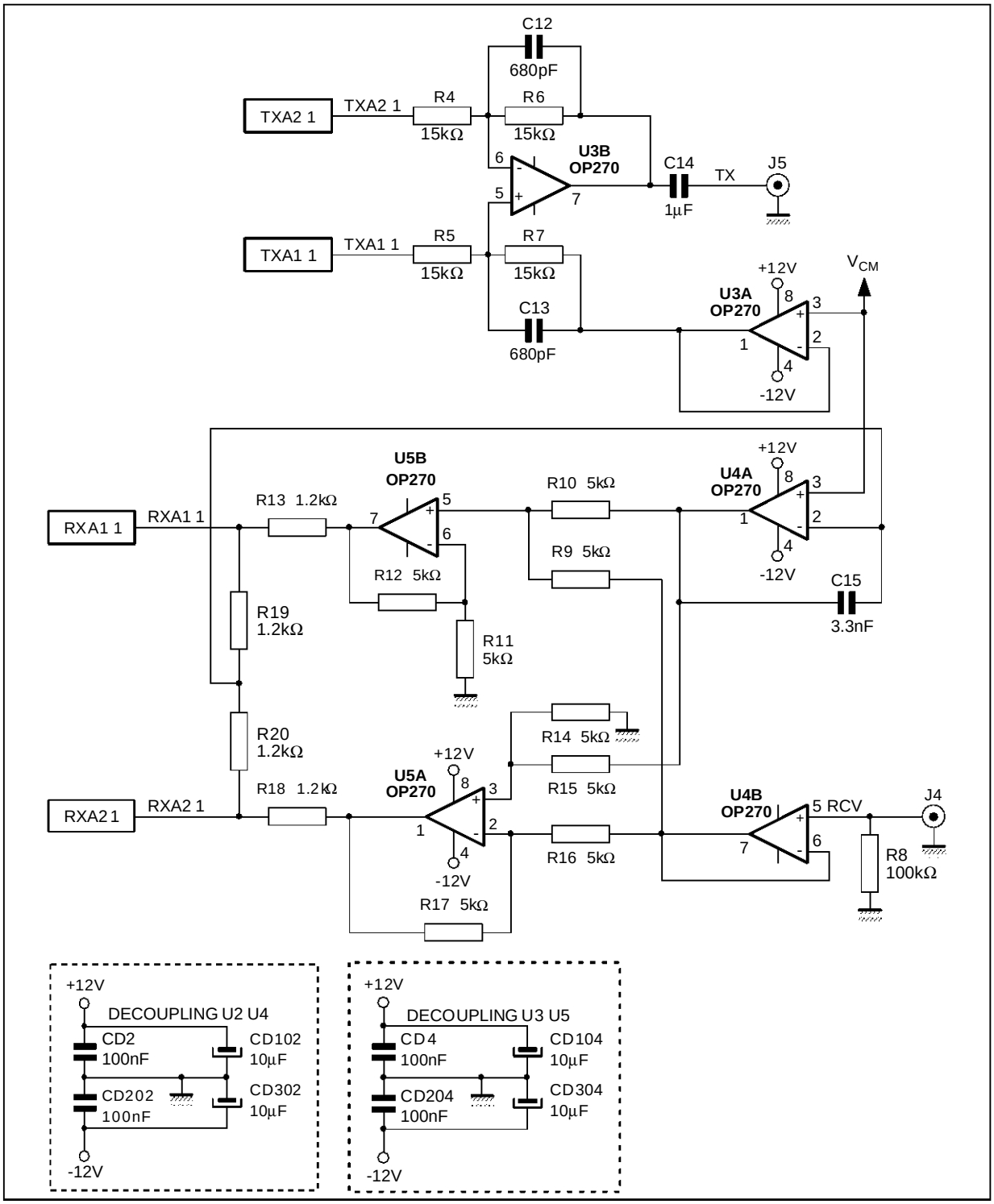


Figure 19

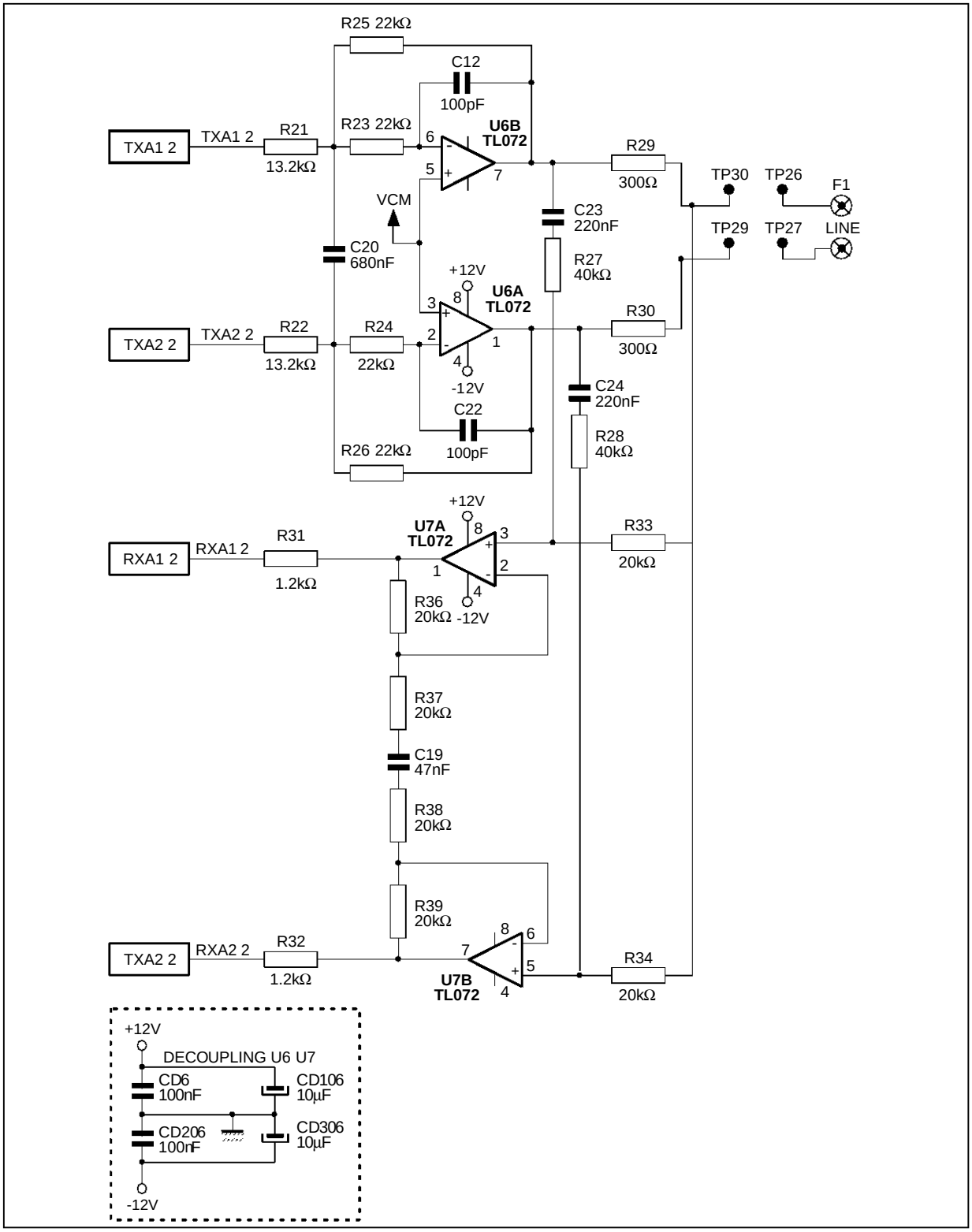
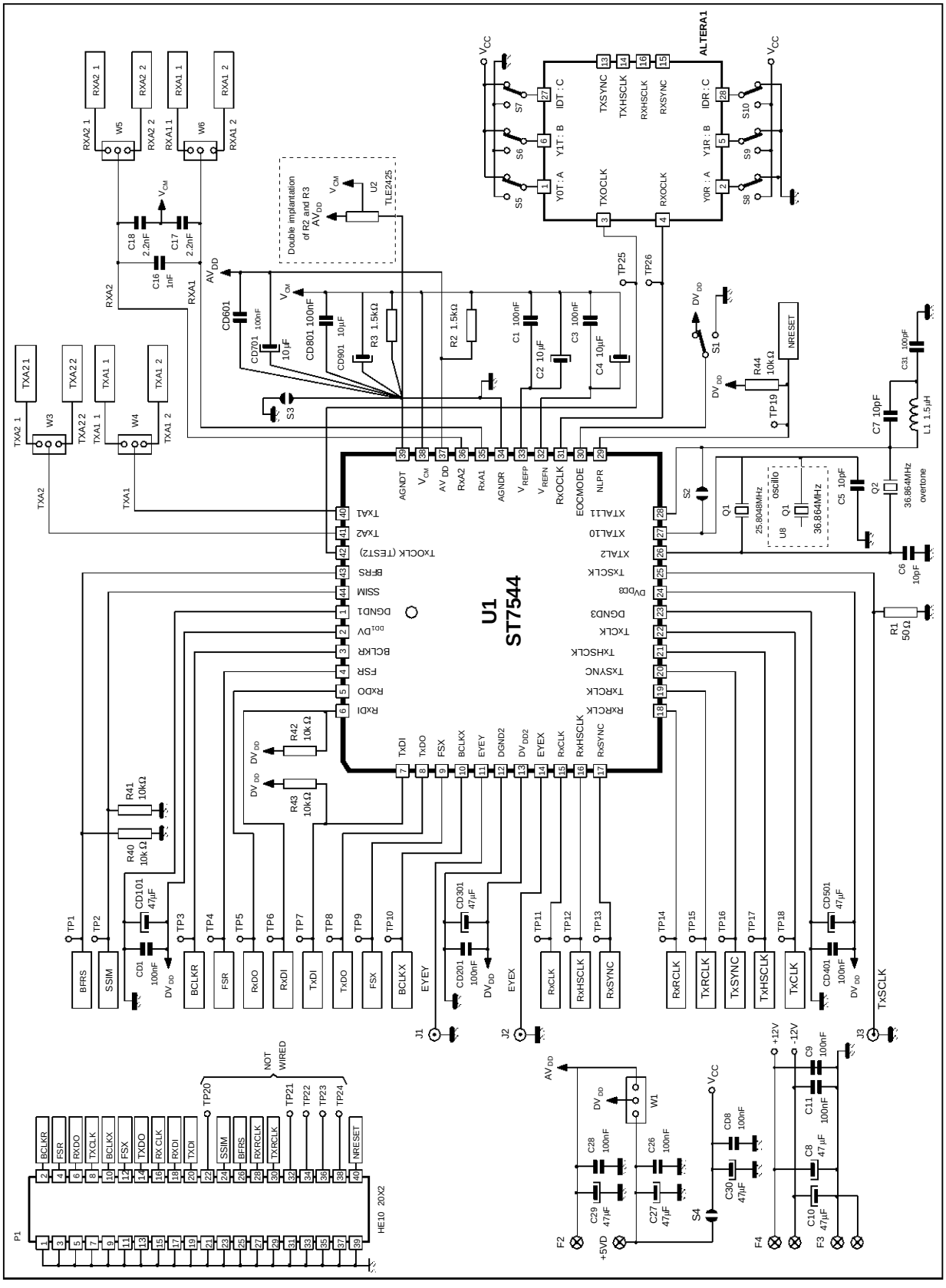

R25 22kΩ
C12
100pF
R23 22kΩ
U6B
TL072
TXA1 2
TXA1 2
R21
13.2kΩ
R29
300Ω
TP30
TP26
F1
VCM
C23
220nF
TP29
TP27
LINE
C20
680nF
R27
40kΩ
+12V
U6A
TL072
R30
300Ω
TXA2 2
TXA2 2
R22
13.2kΩ
R24
22kΩ
-12V
C24
220nF
C22
100pF
R28
40kΩ
R26 22kΩ
+12V
U7A
TL072
R33
20kΩ
RXA1 2
RXA1 2
R31
1.2kΩ
R36
20kΩ
-12V
R37
20kΩ
C19
47nF
R38
20kΩ
R39
20kΩ
TXA2 2
RXA2 2
R32
1.2kΩ
U7B
TL072
R34
20kΩ
+12V
DECOUPLING U6 U7
CD6
100nF
CD106
10µF
CD206
100nF
CD306
10µF
-12V
7544-37.EPS

Figure 20


U1
ST7544
ALTERA1
Double implantation of R2 and R3
NOT WIRED
7544-38.EPS

ANNEXE 2 : Layout

Figure 21

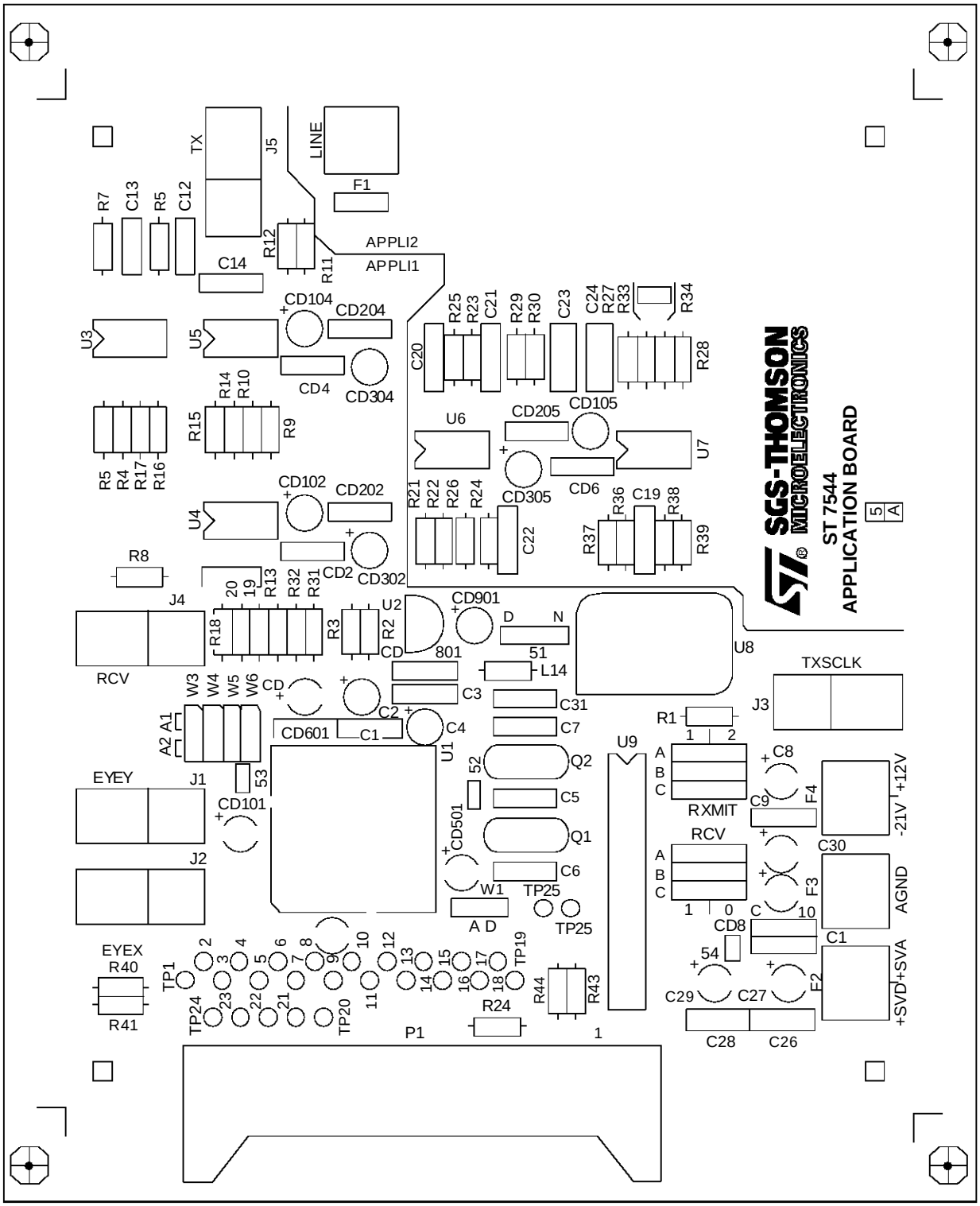
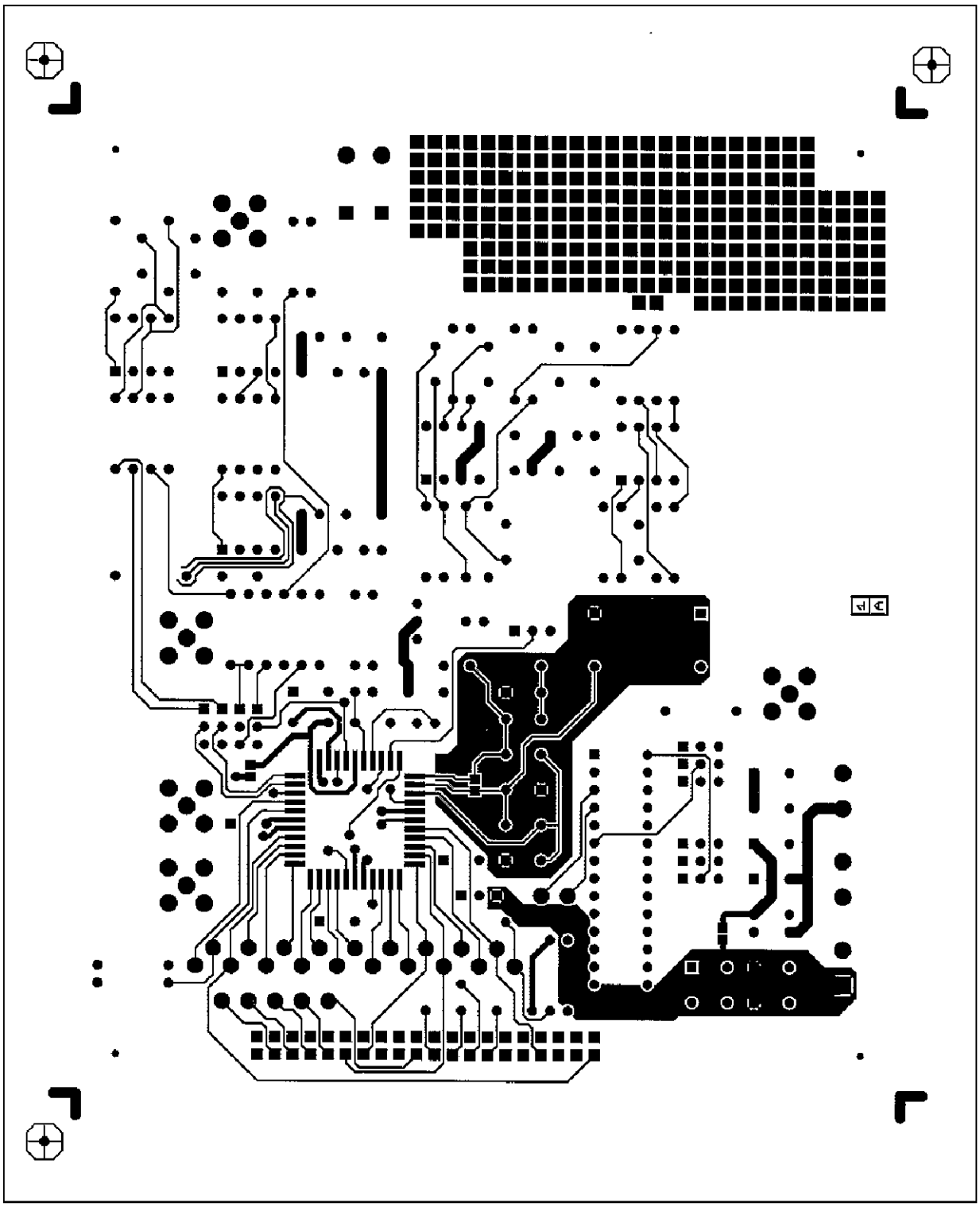
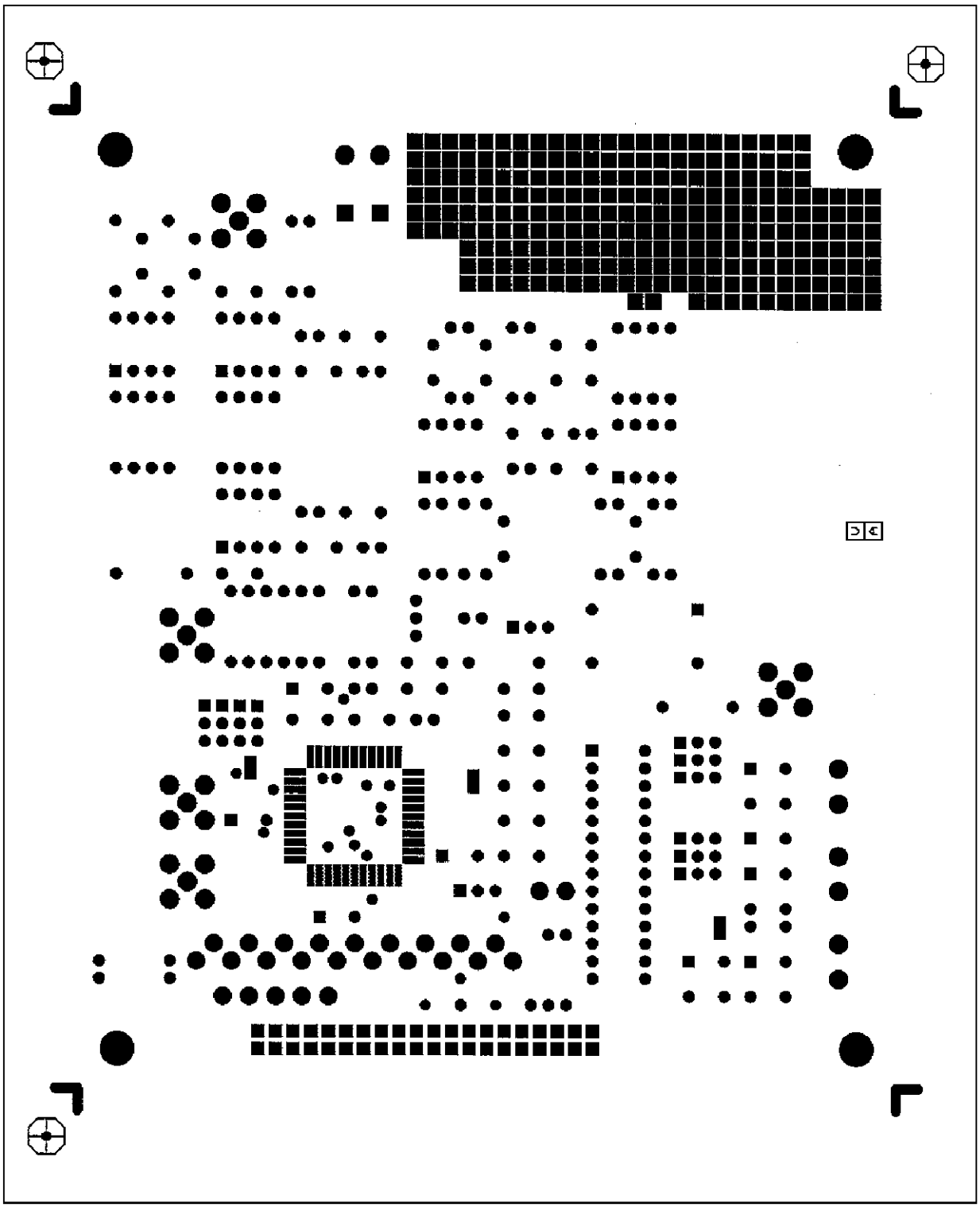


Figure 22 : Layer 1 - Components Side



7544-40.TIF

Figure 23 : Layer 1



7544-41.TIF

Figure 24 : Layer 2 - GNDD, AGND

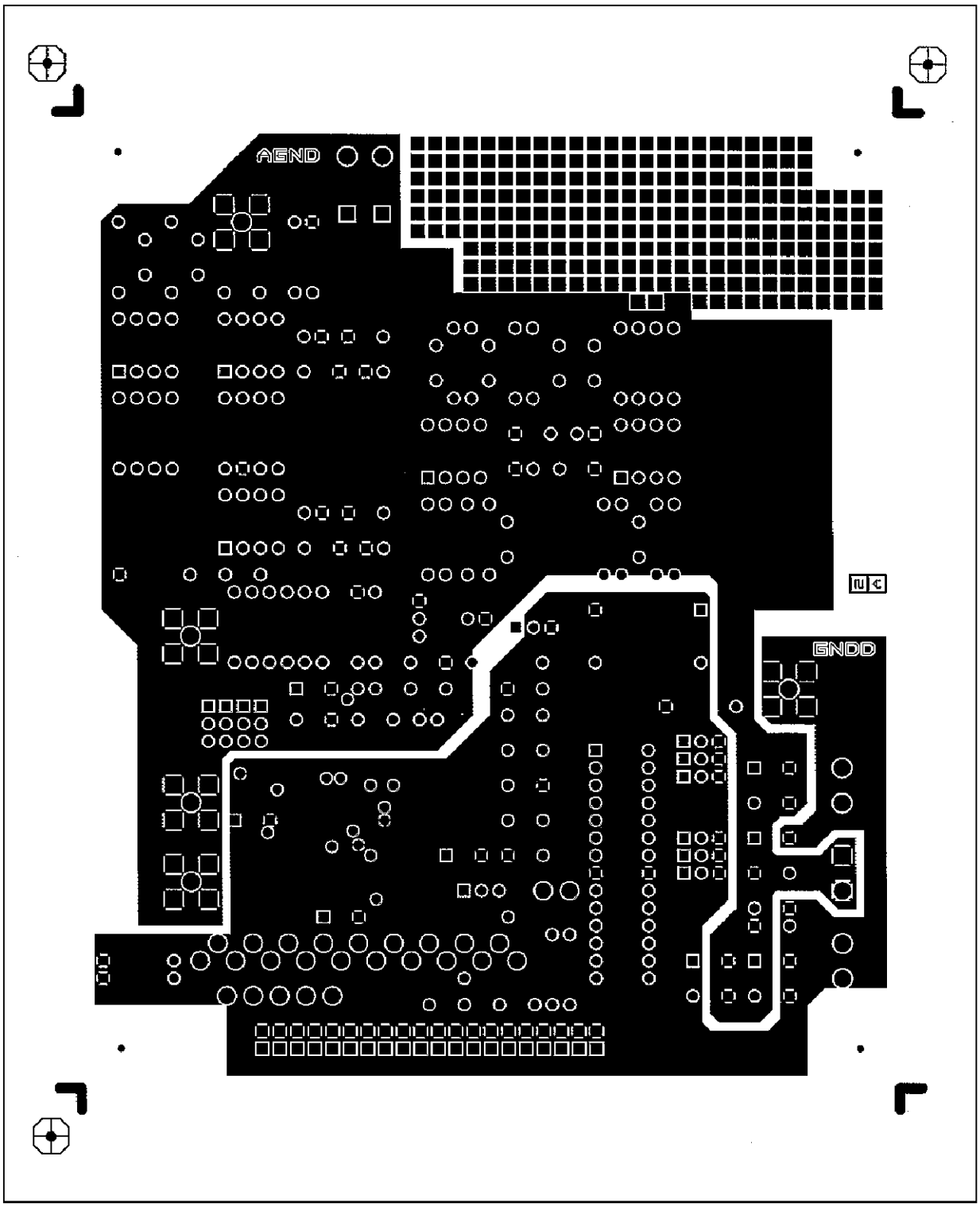


Figure 25 : Layer 3 - DV_{DD}, AV_{DD}

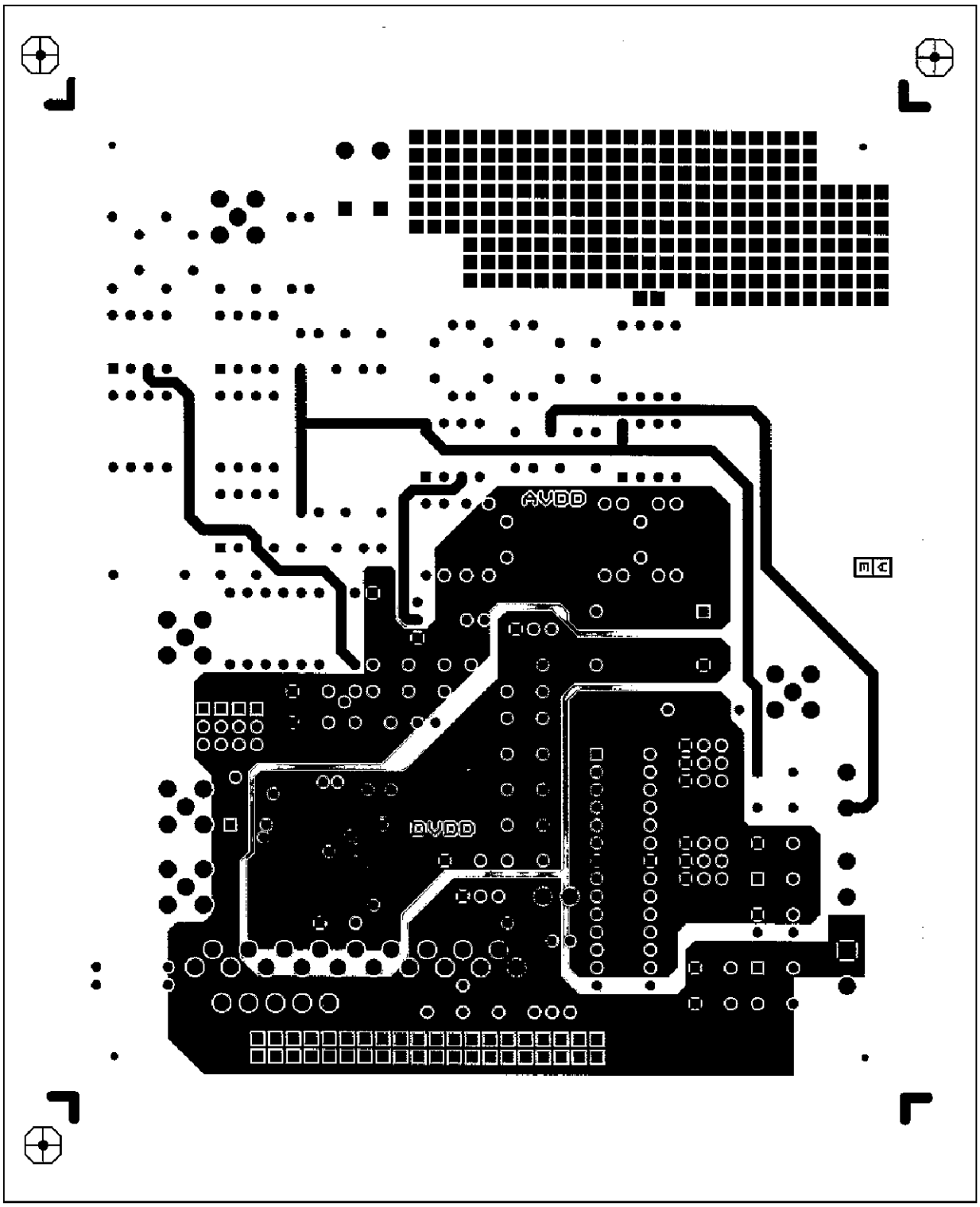
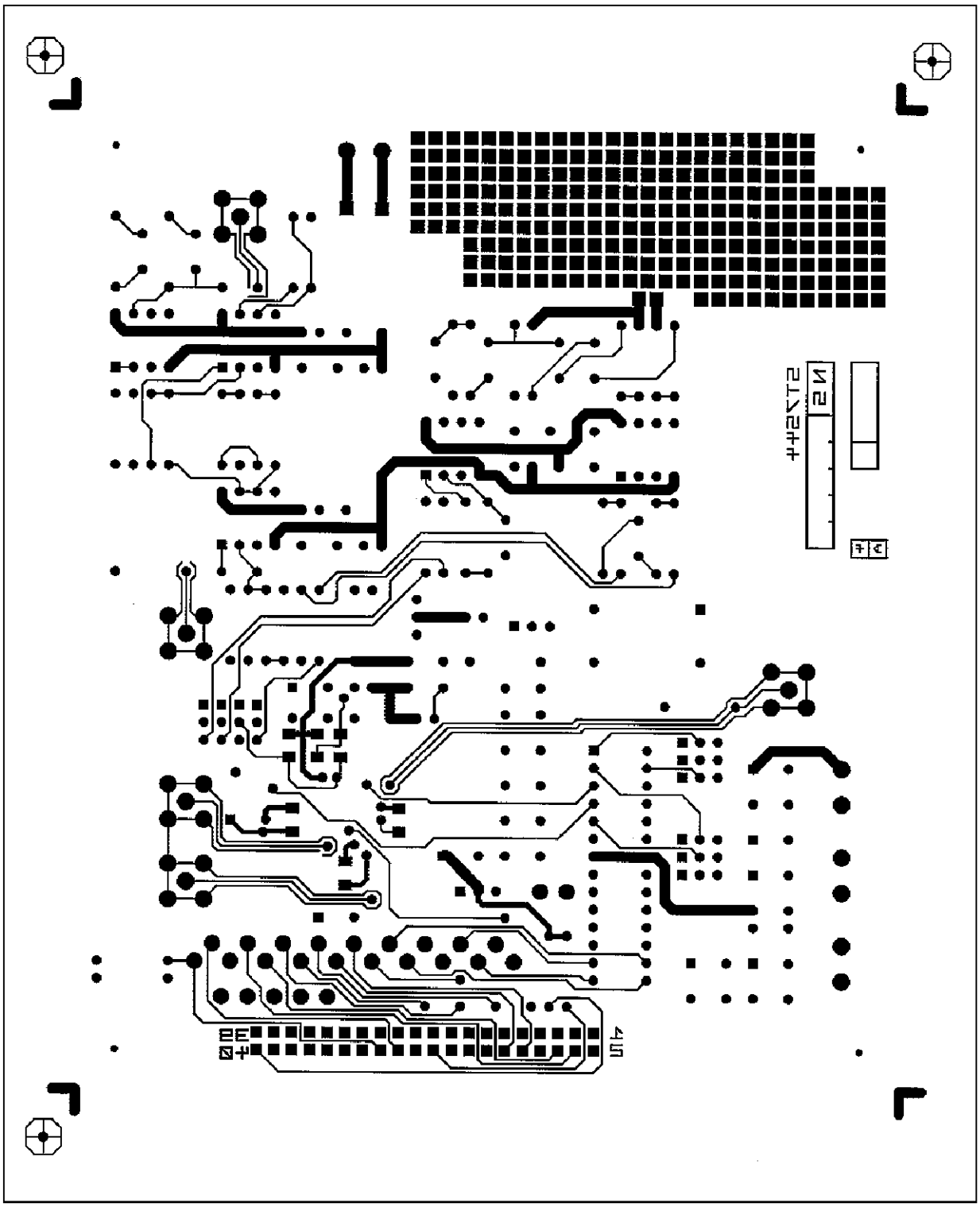
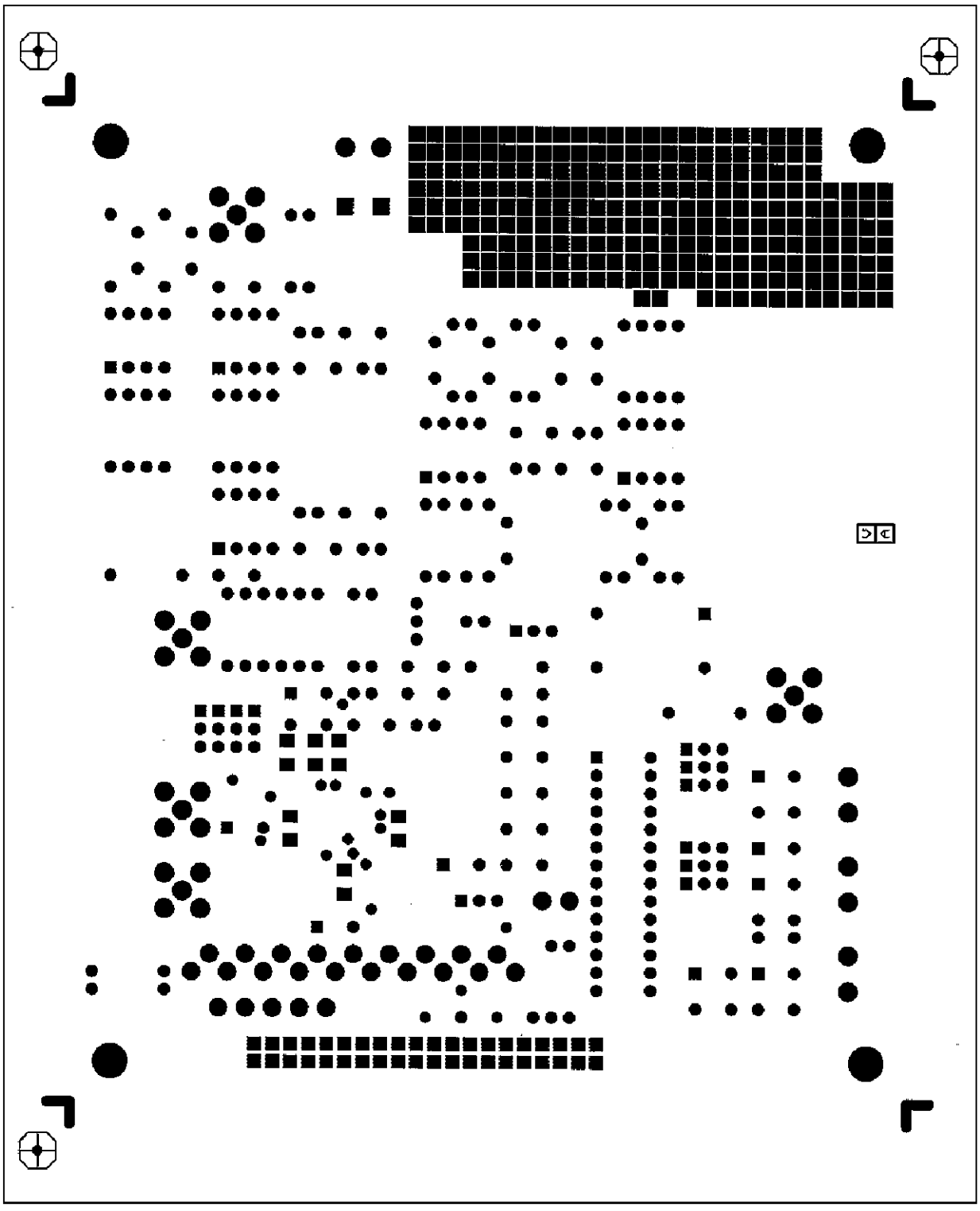


Figure 26 : Layer 4



7544-44.TIF

Figure 27 : Layer 4



7544-45.TIF