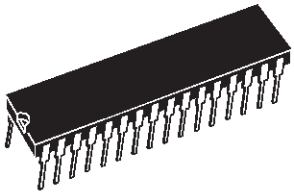
ST72141

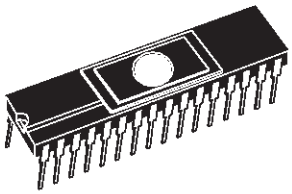
8-BIT MCU WITH 8K ROM/OTP/EPROM, 256 BYTES RAM, ELECTRIC-MOTOR CONTROL, ADC, WDG, SPI AND 2 TIMERS

PRODUCT OVERVIEW

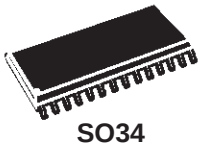
- User Program Memory (ROM/OTP/EPROM): 8K bytes
- Data RAM: 256 bytes including 64 bytes of stack
- Master Reset and Power-On Reset
- Run and Power Saving modes
- Low Voltage Detector (LVD) Reset
- 14 multifunctional bidirectional I/O lines:
  - 14 interrupt inputs on 2 independent lines
  - 8 analog alternate inputs
  - 3 high sink outputs
  - 13 alternate functions
  - EMI filtering
- Software or Hardware Watchdog (WDG)
- Motor Control peripheral featuring:
  - 6 PWM output channels
  - Emergency pin to force outputs to HiZ state
  - 3 analog inputs for rotor position detection with no need of additional sensors
  - Comparator for current control or limitation
- Two 16-bit Timers, each featuring:
  - 2 Input Captures
  - 2 Output Compares
  - External Clock input
  - PWM and Pulse Generator modes
- Synchronous Serial Peripheral Interface (SPI)
- 8-bit ADC with 8 channels
- 8-bit Data Manipulation
- 63 basic Instructions
- 17 main Addressing Modes
- 8 x 8 Unsigned Multiply Instruction
- True Bit Manipulation
- Complete Development Support on DOS/ WINDOWS™ Real-Time Emulator
- Full Software Package on DOS/WINDOWS™ (C-Compiler, Cross-Assembler, Debugger)



PSDIP32



CSDIP32W



SO34

Device Summary

Features	ST72141K2
Program Memory - bytes	8K
RAM (stack) - bytes	256 (64)
Peripherals	MotorControl, Watchdog, Timers, SPI, ADC
Operating Supply	4.5 to 5.5 V
CPU Frequency	8 or 4 MHz (16 **or** 8MHz oscillator)
Temperature Range	- 40°C to + 85°C
Package	SO34 - PSDIP32

Rev. 1.1

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST72141 Microcontroller Unit (MCU) is a member of the ST7 family of Microcontrollers. The device is based on an industry-standard 8-bit core and features an enhanced instruction set. The device is operated at an 8 or 16MHz oscillator frequency. Under software control, the ST72141 may be placed in either Wait, Slow or Halt modes, thus reducing power consumption. The enhanced instruction set and addressing modes afford real programming potential. In addition to standard 8-bit data management, the ST72141 features true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The device includes a low consumption and fast start on-chip oscillator, CPU, ROM/OTP/EPROM, RAM, 14 I/O lines and the following on-chip peripherals: Analog-to-Digital converter (ADC) with 8 multiplexed analog inputs, Motor Control (MTC) peripheral, industry standard synchronous SPI serial interface, digital Watchdog, two independent 16-bit Timers featuring Clock Inputs, Pulse Generator capabilities, 2 Input Captures and 2 Output Compares.

The MTC peripheral is designed to control electric brushless motors, with or without sensors. An example of application is given Figure 2 for 6-step control of Permanent Magnet Direct Current (PMDC) motor.

Figure 1. ST72E14 Block Diagram

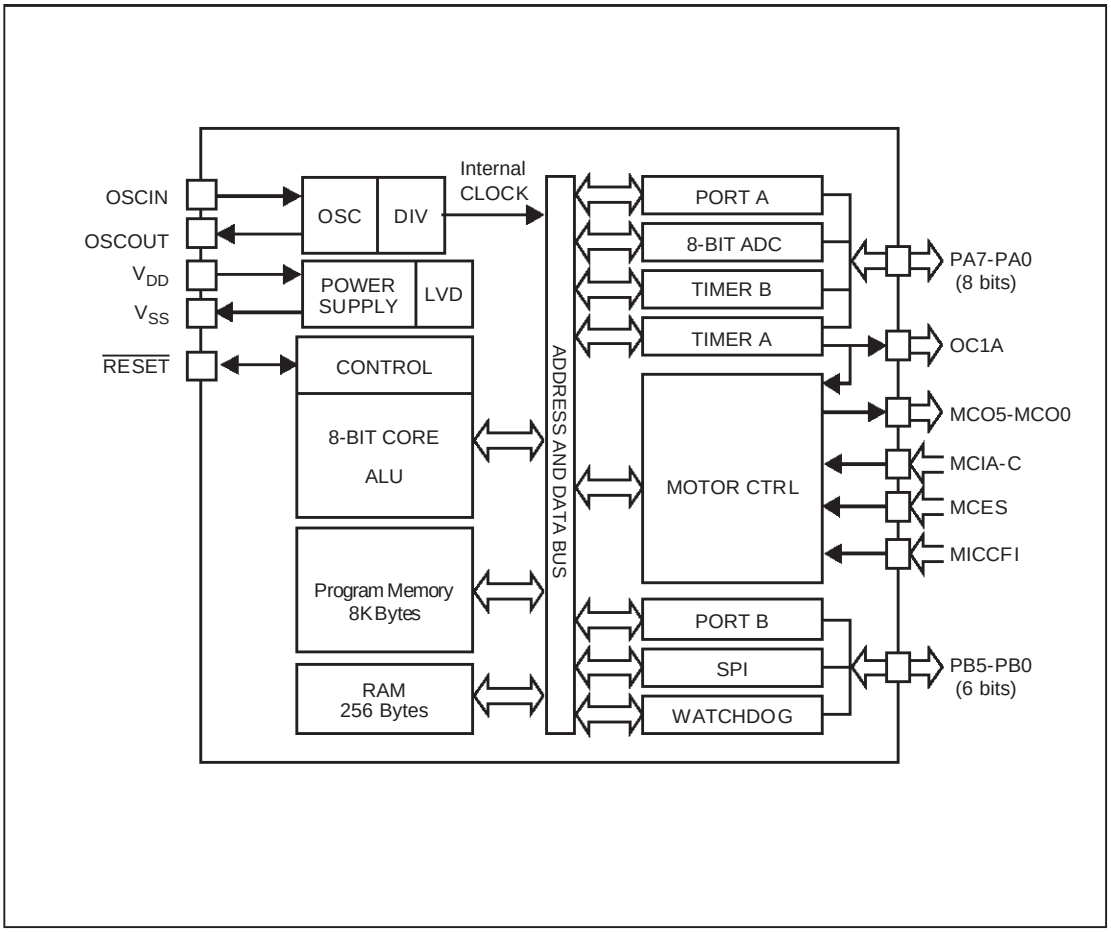
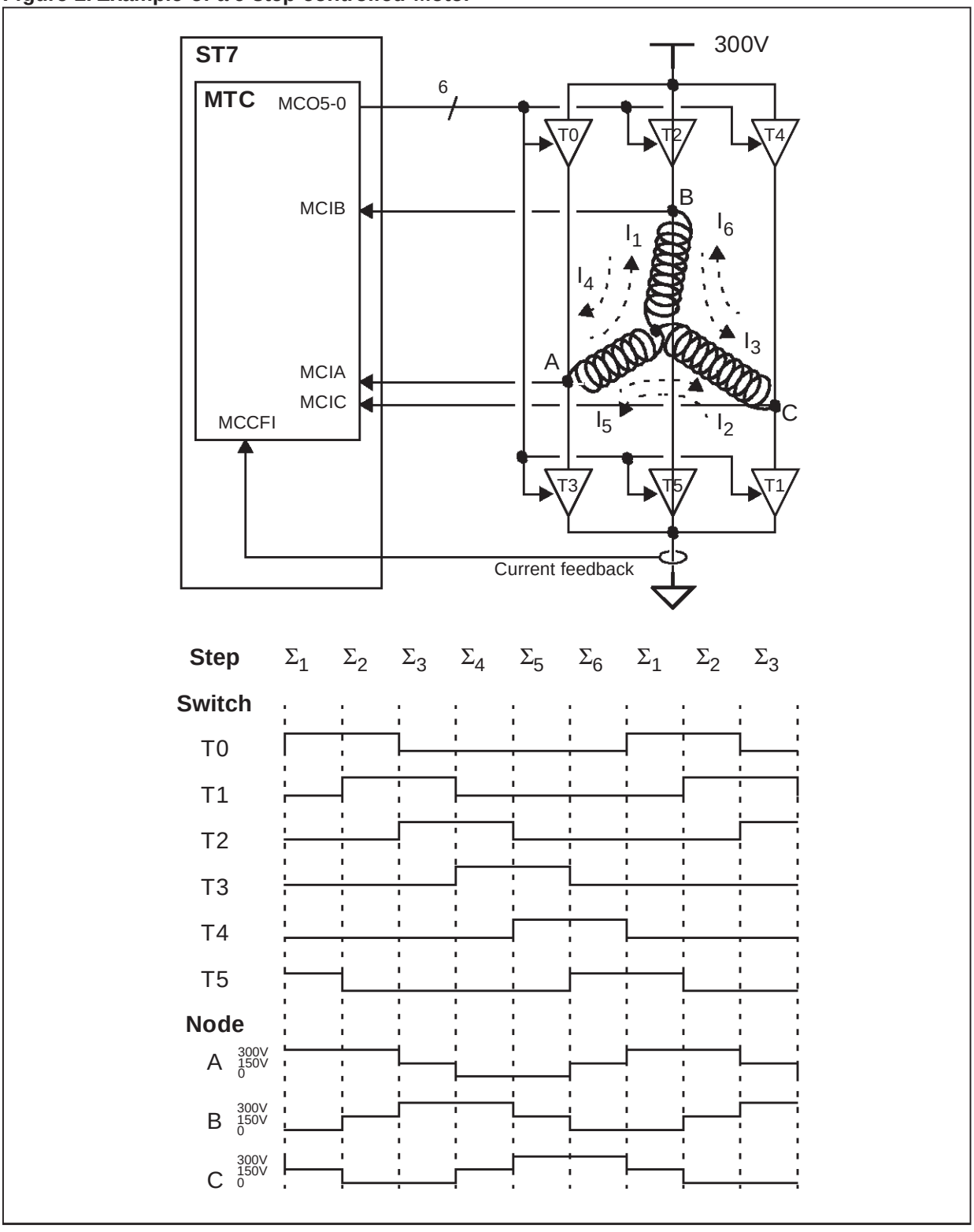


Figure 2. Example of a 6-step-controlled Motor



1.2 PIN DESCRIPTION

Figure 3. 34-Pin SO Package Pinout

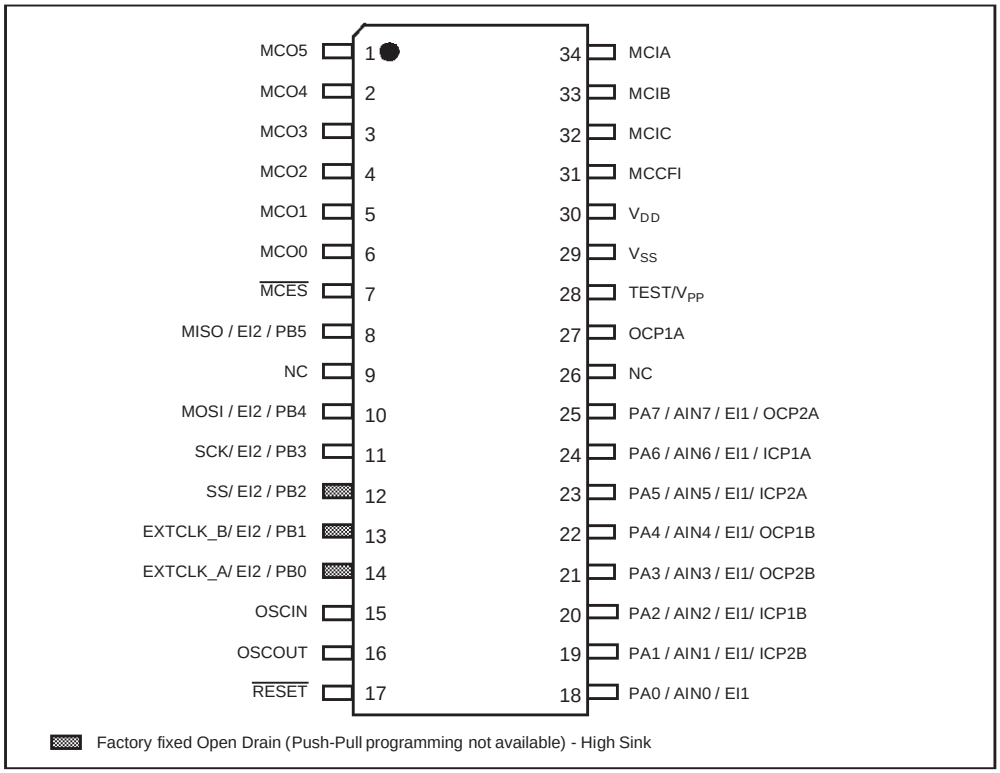


Figure 4. 32-Pin SDIP Package Pinout

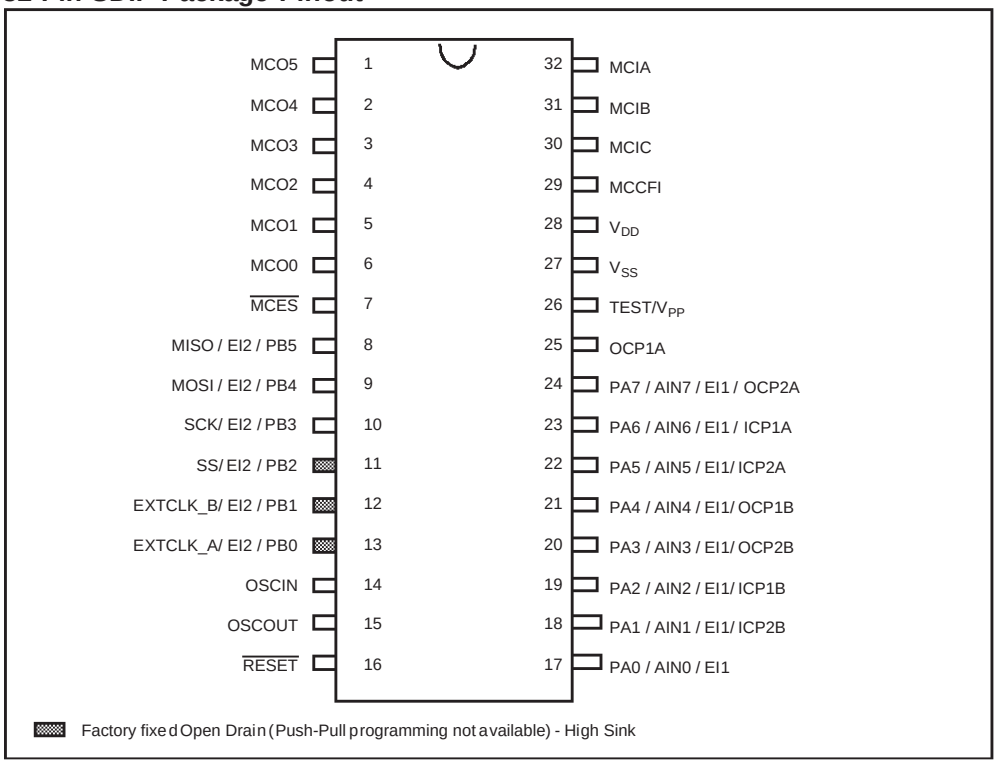


Table 1. ST72E141 Pin Description

Pin n° SO34	Pin n° SDIP32	Pin Name	Type	Levels		Description	Remarks
				In	Out		
1	1	MCO5	O		C	MTC Output Channel 5	
2	2	MCO4	O		C	MTC Output Channel 4	
3	3	MCO3	O		C	MTC Output Channel 3	
4	4	MCO2	O		C	MTC Output Channel 2	
5	5	MCO1	O		C	MTC Output Channel 1	
6	6	MCO0	O		C	MTC Output Channel 0	
7	7	$\overline{\text{MCES}}$	I	C		MTC Emergency Stop	
8	8	MISO/EI2/PB5	I/O	C	C	Port B5 or SPI Master In / Slave Out Data	External Interrupt: EI2
9		NC				Not Connected	
10	9	MOSI/EI2/PB4	I/O	C	C	Port B4 or SPI Master Out / Slave In Data	External Interrupt: EI2
11	10	SCK/EI2/PB3	O	C	C	Port B3 or SPI Serial Clock	External Interrupt: EI2
12	11	SS/EI2/PB2	I/O	C	C	Port B2 or SPI Slave Select (active low)	Ext. Int.: EI2, High Sink
13	12	EXTCLK_B/EI2/PB1	I/O	C	C	Port B1 or Timer B Input Clock	Ext. Int.: EI2, High Sink
14	13	EXTCLK_A/EI2/PB0	I/O	C	C	Port B0 or Timer A Input Clock	Ext. Int.: EI2, High Sink
15	14	OSCIN	I			Input/Output Oscillator pin. These pins connect a parallel-resonant crystal, or an external source to the on-chip oscillator.	
16	15	OSCOUT	O				
17	16	$\overline{\text{RESET}}$	I/O	C	C	Bidirectional. Active low. Top priority non maskable interrupt.	
18	17	PA0/AIN0/EI1	I/O	C/A	C	Port A0 or ADC Analog Input 0	External Interrupt: EI1
19	18	PA1/AIN1/EI1/ ICP2B	I/O	C/A	C	Port A1 or TimerB Input Capture 2 or ADC Analog Input 1	External Interrupt: EI1
20	19	PA2/AIN2/EI1/ ICP1B	I/O	C/A	C	Port A2 or TimerB Input Capture 1 or ADC Analog Input 2	External Interrupt: EI1
21	20	PA3/AIN3/EI1/ OCP2B	I/O	C/A	C	Port A3 or TimerB Output Compare 2 or ADC Analog Input 3	External Interrupt: EI1
22	21	PA4/AIN4/EI1/ OCP1B	I/O	C/A	C	Port A4 or TimerB Output Compare 1 or ADC Analog Input 4	External Interrupt: EI1
23	22	PA5/AIN5/EI1/ ICP2A	I/O	C/A	C	Port A5 or TimerA Input Capture 2 or ADC Analog Input 5	External Interrupt: EI1
24	23	PA6/AIN6/EI1/ ICP1A	I/O	C/A	C	Port A6 or TimerA Input Capture 1 or ADC Analog Input 6	External Interrupt: EI1
25	24	PA7/AIN7/EI1/ OCP2A	I/O	C/A	C	Port A7 or TimerA Output Compare 2 or ADC Analog Input 7	External Interrupt: EI1
26		NC				Not Connected	
27	25	OCP1A	O		R	TimerA Output Compare 1	
28	26	TEST/V_{PP}[1)]	I/S			Test mode pin (should be tied low in user mode). In the EPROM programming mode, this pin acts as the programming voltage input V_{PP}	
29	27	V_{SS}	S			Ground	
30	28	V_{DD}	S			Main power supply	
31	29	MCCFI	I	A		MTC Current Feed Back	
32	30	MCIC	I	A		MTC Input C	
33	31	MCIB	I	A		MTC Input B	
34	32	MCIA	I	A		MTC Input A	

Note 1: V_{PP} on EPROM/OTP only.

– C = CMOS levels ($0.3V_{DD}$ / $0.7V_{DD}$)

– R = 70kΩ/100kΩ Ratio of CMOS Levels ($0.2V_{DD}$ / $0.5V_{DD}$)

– A = Analog levels

1.3 MEMORY MAP

Figure 5. Program Memory Map

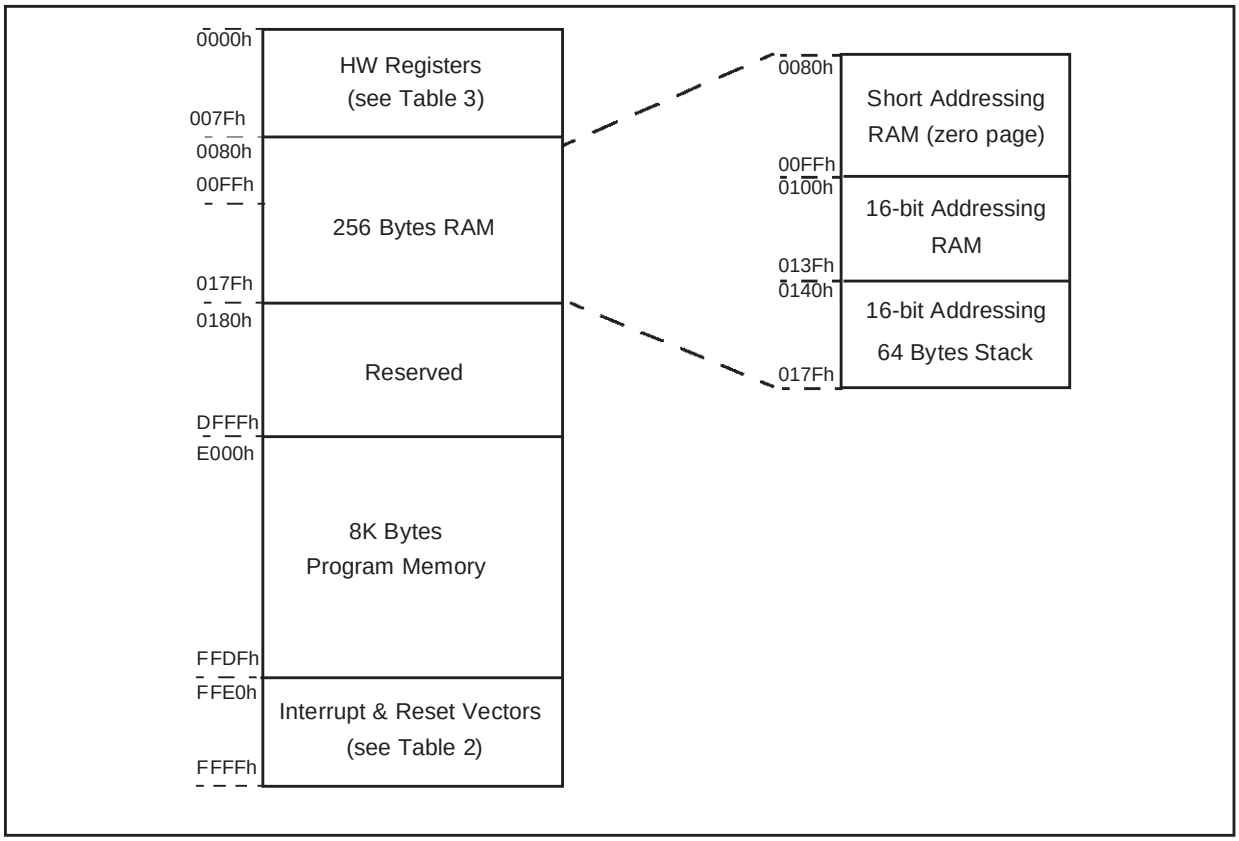


Table 2. Interrupt Vector Map

Vector Address	Description	Remarks
FFE0-FFE1h	Not Used	
FFE2-FFE3h	Not Used	
FFE4-FFE5h	Not Used	
FFE6-FFE7h	Not Used	
FFE8-FFE9h	Not Used	
FFEA-FFEBh	TIMER B Interrupt Vector	Internal Interrupt
FFEC-FFEDh	TIMER A Interrupt Vector	Internal Interrupt
FFEE-FFEFh	SPI Interrupt Vector	Internal Interrupt
FFF0-FFF1h	MTC Interrupt Vector 3 (D, O, R & E events)	Internal Interrupt
FFF2-FFF3h	MTC Interrupt Vector 2 (C event)	Internal Interrupt
FFF4-FFF5h	MTC Interrupt Vector 1 (Z event)	Internal Interrupt
FFF6-FFF7h	External Interrupt Vector EI2 (PB0:PB5)	External Interrupt
FFF8-FFF9h	External Interrupt Vector EI1 (PA0:PA7)	External Interrupt
FFFA-FFFBh	Not Used	
FFFC-FFFDh	TRAP (software) Interrupt Vector	CPU Interrupt
FFFE-FFFFh	RESET Vector	

Table 3. Hardware Register Memory Map

Address	Block	Register Label	Register Name	Reset Status	Remarks
0000h	Port A	PADR	Data Register	00h	R/W
0001h		PADDR	Data Direction Register	00h	R/W
0002h		PAOR	Option Register	00h	R/W
0003h	Reserved Area (1 byte)				
0004h	Port B	PBDR	Data Register	00h	R/W
0005h		PBDDR	Data Direction Register	00h	R/W
0006h		PBOR	Option Register	00h	R/W
0007h to 001Fh	Reserved Area (25 bytes)				
0020h		MISCR	Miscellaneous Register	00h	
0021h	SPI	SPIDR	SPI Data I/O Register	xxh	R/W
0022h		SPICR	SPI Control Register	0xh	R/W
0023h		SPISR	SPI Status Register	00h	Read Only
0024h	WDG	WDGCR	Watchdog Control Register	7Fh	R/W
0025h		WDGSR	Watchdog Status Register	x0h	Read Only
0026h to 0030h	Reserved Area (11 bytes)				
0031h	Timer A	TACR2	Control Register2	00h	R/W
0032h		TACR1	Control Register1	00h	R/W
0033h		TASR	Status Register	xxh	Read Only
0034h-0035h		TAIC1HR	Input Capture1 High Register	xxh	Read Only
		TAIC1LR	Input Capture1 Low Register	xxh	Read Only
0036h-0037h		TAOC1HR	Output Compare1 High Register	80h	R/W
		TAOC1LR	Output Compare1 Low Register	00h	R/W
0038h-0039h		TACHR	Counter High Register	FFh	Read Only
		TACLR	Counter Low Register	FCh	Read Only
003Ah-003Bh		TAACHR	Alternate Counter High Register	FFh	Read Only
		TAACLR	Alternate Counter Low Register	FCh	Read Only
003Ch-003Dh		TAIC2HR	Input Capture2 High Register	xxh	Read Only
		TAIC2LR	Input Capture2 Low Register	xxh	Read Only
003Eh-003Fh		TAOC2HR	Output Compare2 High Register	80h	R/W
		TAOC2LR	Output Compare2 Low Register	00h	R/W
0040h	Reserved Area (1 byte)				

Address	Block	Register Label	Register Name	Reset Status	Remarks
0041h	Timer B	TBCR2	Control Register2	00h	R/W
0042h		TBCR1	Control Register1	00h	R/W
0043h		TBSR	Status Register	xxh	Read Only
0044h-0045h		TBIC1HR	Input Capture1 High Register	xxh	Read Only
		TBIC1LR	Input Capture1 Low Register	xxh	Read Only
0046h-0047h		TBOC1HR	Output Compare1 High Register	80h	R/W
		TBOC1LR	Output Compare1 Low Register	00h	R/W
0048h-0049h		TBCHR	Counter High Register	FFh	Read Only
		TBCLR	Counter Low Register	FCh	Read Only
004Ah-004Bh		TBACHR	Alternate Counter High Register	FFh	Read Only
		TBACLR	Alternate Counter Low Register	FCh	Read Only
004Ch-004Dh		TBIC2HR	Input Capture2 High Register	xxh	Read Only
		TBIC2LR	Input Capture2 Low Register	xxh	Read Only
004Eh-004Fh		TBOC2HR	Output Compare2 High Register	80h	R/W
		TBOC2LR	Output Compare2 Low Register	00h	R/W
0050h to 005Fh	Reserved Area (16 bytes)				
0060h	Motor Control	MCNT	Counter Register	00h	R/W
0061h		MZPRV	Zn-1 Capture Register	00h	R/W
0062h		MZREG	Zn Capture Register	00h	R/W
0063h		MCREG	C_{n+1}Compare Register	00h	R/W
0064h		MDREG	D capture/Compare Register	00h	R/W
0065h		MWGHT	Weight Register	00h	R/W
0066h		MPRSR	Prescaler and Ratio Register	00h	R/W
0067h		MIMR	Interrupt Mask Register	00h	R/W
0068h		MISR	Interrupt Status Register	00h	R/W
0069h		MCRA	Control Register A	00h	R/W
006Ah		MCRB	Control Register B	00h	R/W
006Bh		MPHST	Phase State Register	00h	R/W
006Ch		MPAR	Output Parity Register	00h	R/W
006Dh		MPOL	Output Polarity Register	00h	R/W
006Eh to 006Fh	Reserved Area (2 bytes)				
0070h	ADC	ADCDR	Data Register	00h	Read Only
0071h		ADCCSR	Control/ Status Register	00h	R/W
0072h to 007Fh	Reserved Area (14 bytes)				

2 Motor Control peripheral overview

The Motor Control (MTC) peripheral can be seen as a Pulse Width Modulator which can be multiplexed on six output channels, and a Back Electromotive Force (BEMF) zero-crossing detector which enables a sensorless control of self commutated Permanent Magnet Direct Current (PMDC) brushless motor.

This peripheral is particularly suited to driving synchronous motors and enables the implementation of operating modes like

- Commutation step control with motor voltage regulation.
- Commutation step control with motor current regulation, i.e. direct torque control.
- Sensor or sensorless motor phase commutation control.
- BEMF zero-crossing detection with high sensitivity. The integrated phase voltage comparator is directly referred to the full BEMF voltage without any attenuation. So a BEMF voltage down to 200mV can be detected, providing high noise immunity and a self-commutated operation in a large speed range.
- Real time motor winding demagnetisation detection enabling to fine-tune the phase voltage masking time to be applied before BEMF monitoring.
- Automatic and programmable delaying between BEMF zero-crossing detection and motor phase commutation.

2.1 MTC peripheral main features

- Two on-chip analog comparators, one for BEMF zero-crossing detection with an 100mV hysteresis, the other for current regulation or limitation.
- One of four selectable internal voltage reference values for the hysteresis comparator (0.2V, 0.6V, 1.2V, 2.5V).
- One central 8-bit timer with two compare registers and two capture features.
- A “measurement window generator” allowing BEMF zero-crossing detection.
- An auto-calibrated prescaler with 16 division steps.
- One 8-bit by 8-bit multiplier.
- Phase input multiplexer.
- Sophisticated output management:
  - The six output channels can be split in two groups (high side & low side).
  - The PWM signal can be multiplexed on high, low or both groups, alternatively or simultaneously.
  - The output polarity is programmable channel by channel.
  - An output enable bit forces the outputs in HiZ (active low).
  - An emergency stop pin input (MCES) immediately forces the outputs in HiZ when reset.
- The MTC peripheral always operates at a 4MHz frequency, equal to f_{CPU} or $f_{CPU}/2$ depending on the external clock frequency, and not affected by slow mode selection.

2.2 General principle

The following example (Figure 6) relates to a six step command sequence for a PMDC brushless motor.

The commutation event [Cn] is automatically generated by the MTC peripheral after detecting the zero-crossing of the BEMF induced in the non-exited coil by the rotor. The delay between this event [Zn] and the commutation is computed by the MTC peripheral. The BEMF zero-crossing detection is enabled only after the end of demagnetization event [Dn], also detected (or simulated) by the MTC peripheral.

The speed regulation is managed by the microcontroller, by means of an adjustable reference current level (current control), or by the PWM duty-cycle adjustment (voltage control).

All the detection of [Zn] events is done during a short measurement window while the high side switch is turned off. The high side node (refer to Table 4) is tied to 0V by the free-wheeling diode, and the “zero-crossing” detection is then possible.

Figure 6. Example of command sequence for 6-step mode

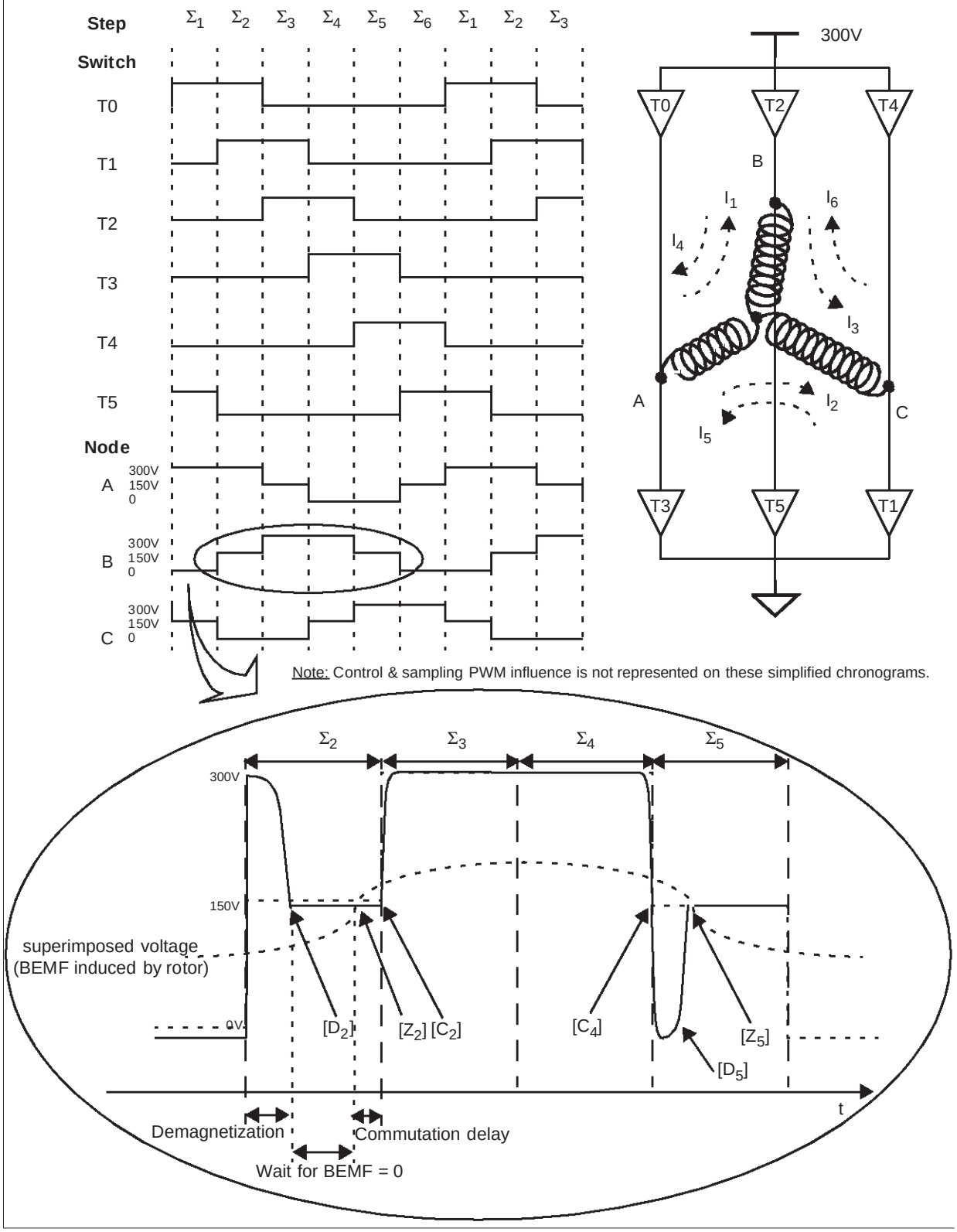
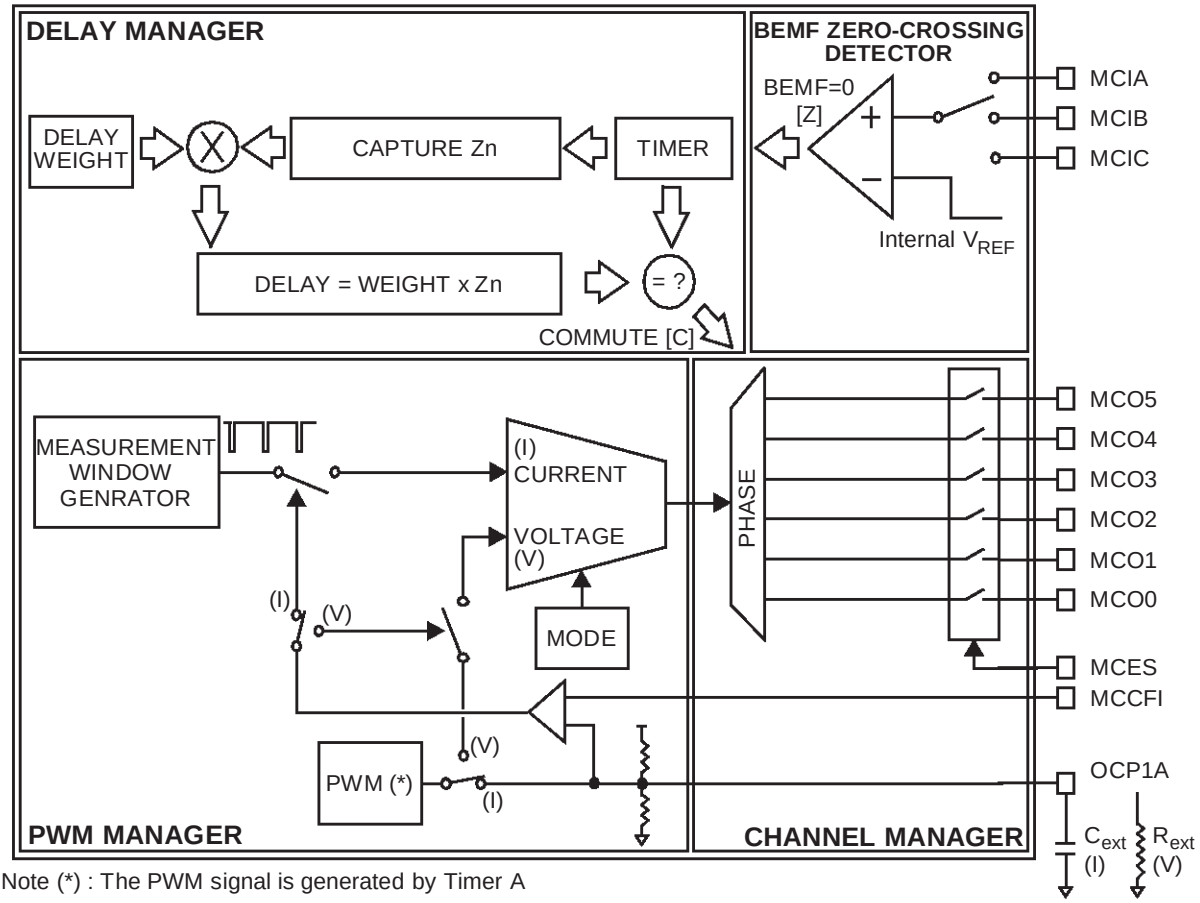


Table 4. Step configuration summary

Step	Σ_1	Σ_2	Σ_3	Σ_4	Σ_5	Σ_6
Current direction	A(+)/B(-)	A(+)/C(-)	B(+)/C(-)	B(+)/A(-)	C(+)/A(-)	C(+)/B(-)
High side active switch	T0	T0	T2	T2	T4	T4
Low side active switch	T5	T1	T1	T3	T3	T5
Measure done on	MCIC	MCIB	MCIA	MCIC	MCIB	MCIA

Figure 7. Simplified MTC peripheral block diagram (without microcontroller interface)



Note (*) : The PWM signal is generated by Timer A

[Z] : Back EMF Zero-crossing event
Z_n : Time elapsed between two consecutive Z events
[C] : Commutation event
C_n : Time delayed after Z event to generate C event
(I): Current mode
(V): Voltage mode

3 MTC Peripheral general description

The MTC peripheral can be split into four main parts as described in the simplified block diagram (Figure 7).

– The PWM MANAGER, including a “measurement window generator”, a mode selector and current control.
– The BEMF ZERO-CROSSING DETECTOR with a comparator and an input multiplexer.
– The DELAY MANAGER with an 8 bit timer and an 8x8 bit multiplier.
– The CHANNEL MANAGER with the PWM multiplexer, polarity programming capability and emergency HiZ configuration input.

3.1 PWM Manager

The PWM manager enables a voltage control or a current control of the motor to be performed via the six output channels.

3.1.1 Voltage Mode

In voltage mode, the PWM provided by TimerA is directed to the channel manager.

Its duty cycle is adjusted by software according to the needs of the application (speed regulation for example).

The current comparator is used for safety purpose as a current limitation, with a limit fixed by means of an internal resistor bridge, adjustable with an external resistor (R_{ext} on OCP1A).

3.1.2 Current Mode

In current mode, the PWM output signal is generated by a combination of the “measurement window generator” and the current comparator outputs, and is directed to the channel manager.

The “on state” of the resulting PWM starts at the end of the “measurement window” (rising edge), and ends either at the beginning of the next “measurement window” (falling edge), or when the current level in the exited coils reaches the current reference.

This current reference is provided to the comparator by the PWM output of TimerA (0.25% resolution), filtered through a RC (integrated resistor and external capacitor C_{ext} on OCP1A).

3.2 Channel manager

The channel manager includes a channel state register, a multiplexer with upper and lower channel differentiation, a polarity register and a tri-state output buffer.

A pre-load register enables the CPU to asynchronously update the channel configuration for the next step.

The multiplexer directs the PWM to the upper channel, the lower channel or both of them alternatively or simultaneously, enabling to choose the most appropriate reference potential when free-wheeling the motor in order to improve system efficiency and speed up the demagnetisation phase.

The polarity register is used to fit the polarity of the power drivers keeping the same control logic and software.

3.3 BEMF zero-crossing detector

This detector is made of:

– a phase multiplexer for addressing the non-excited motor winding
– an analog comparator referred to a selectable voltage level for zero-crossing detection. This voltage reference can be chosen between four values, depending on the noise level and the voltage supply of the application
– a latch to sample the BEMF zero-crossing detection.

This block is used for detecting BEMF zero-crossing and end of demagnetization events.

The BEMF detections are performed during the “measurement window”, when free-wheeling through the low side switches. The zero-crossing sampling frequency is then defined by the “measurement window generator” frequency.

3.4 Delay manager

The delay manager computes in real time the delay between the BEMF zero-crossing detection and the next step commutation.

It includes an 8 bit timer with two capture, two compare registers and an 8x8 bit multiplier.

An auto-updated prescaler always configures the timer in the best accuracy area.

Two BEMF zero-crossing consecutive events are memorized by the capture registers. Starting from those values, and using parameters preset by the CPU, the delay manager calculates the value to be loaded in a compare register, which automatically triggers the next commutation.

The second compare register is used for end of demagnetization simulation when the event is not detectable ([D_2] on the example of Figure 6).

Notes: