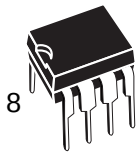
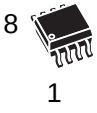
ST24/25C08, ST24C08R
ST24/25W08

SERIAL 8K (1K x 8) EEPROM

- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x08 versions
  - 2.5V to 5.5V for ST25x08 versions
  - 1.8V to 5.5V for ST24C08R version only
- HARDWARE WRITE CONTROL VERSIONS: ST24W08 and ST25W08
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

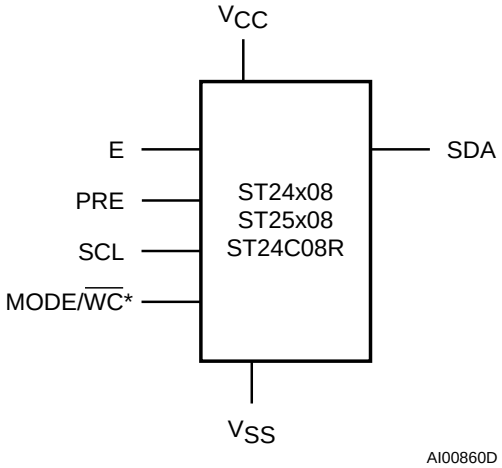


PSDIP8 (B)
0.25mm Frame



SO8 (M)
150mil Width

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W08 products.

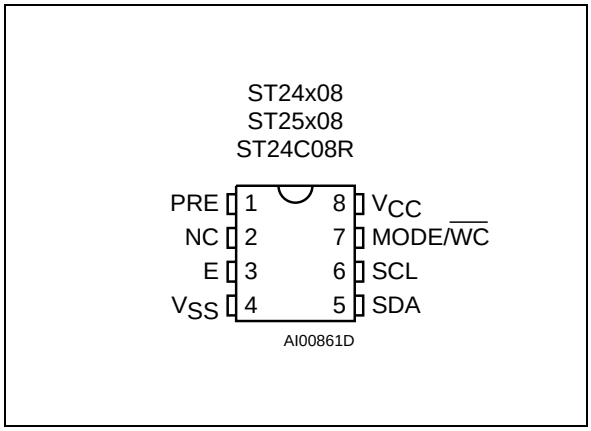
DESCRIPTION

This specification covers a range of 8K bits I^2C bus EEPROM products, the ST24/25C08, the ST24C08R and the ST24/25W08. In the text, products are referred to as ST24/25x08, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

Table 1. Signal Names

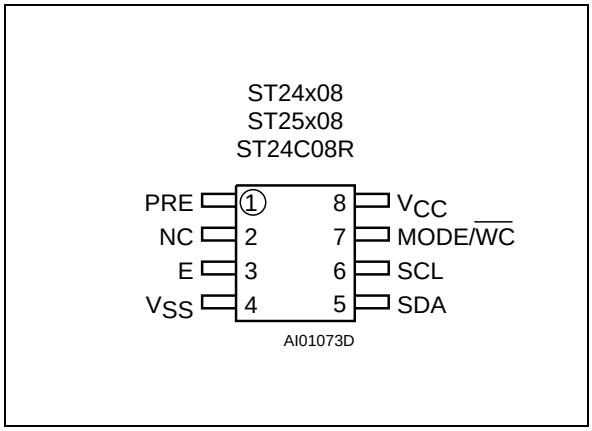
PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected.

Figure 2B. SO Pin Connections



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x08 are 8K bit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The memories operate with a power supply value as low as 1.8V for the ST24C08R only.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 1 chip enable input (E) so that up to 2 x 8K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable	Block Select		RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 1024	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	8	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W08 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E). This chip enable input is used to set one least significant bit (b3) of the device select byte code. This input may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 3FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also WC feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control (WC). An hardware Write Control (WC) feature is offered only for ST24W08 and ST25W08 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC = V_{IH}) or disable (WC = V_{IL}) the internal write protection. When unconnected, the WC input is internally read as V_{IL} and the memory area is not write protected.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x08 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x08 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x08 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x08 and the bus master. A STOP condition at the end of a Read command, after and only after a No Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x08 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x08, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

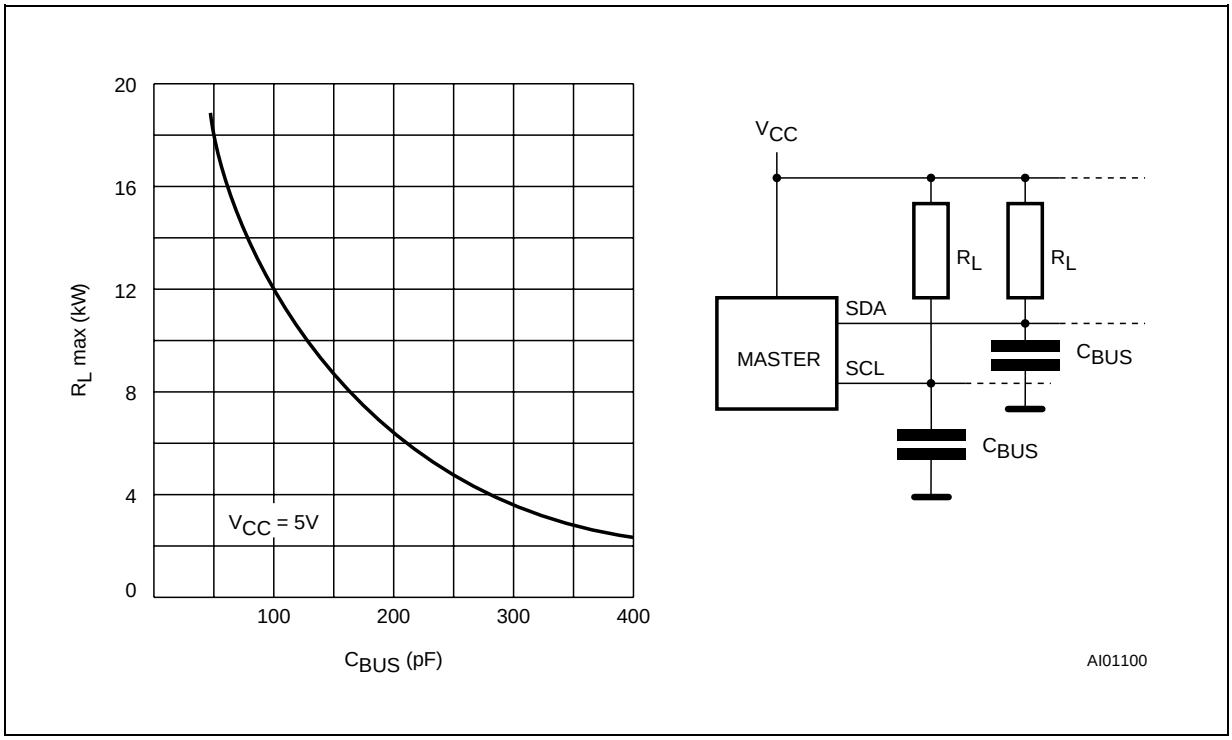


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W08)	V_{IN} £ 0.3 V_{CC}	5	20	kW
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W08)	V_{IN} ³ 0.7 V_{CC}	500		kW
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V £ V_{IN} £ V_{CC}		±2	mA
I_{LO}	Output Leakage Current	0V £ V_{OUT} £ V_{CC} SDA in Hi-Z		±2	mA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		100	mA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	mA
I_{CC2}	Supply Current (Standby) (ST25 series)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		5	mA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	mA
I_{CC3}	Supply Current (Standby) (ST24C08R)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V		20	mA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V, f_C = 100kHz		60	mA
I_{CC4}	Supply Current (Standby) (ST24C08R)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		10	mA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V, f_C = 100kHz		20	mA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (ST24C08R)	I_{OL} = 1mA, V_{CC} = 1.8V		0.3	V

Table 7. AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°

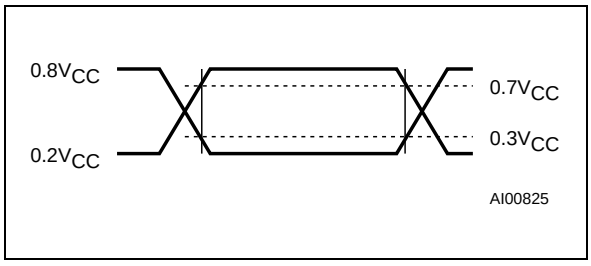
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	ms
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	ms
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		ms
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		ms
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		ms
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		ms
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		ms
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		ms
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		ms
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	ms
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	£ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following bit identifies the specific memory on the bus. It is matched to the chip enable signal E. Thus up to 2 x 8K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following bit to its chip enable input E.

The 6th and 7th bits sent, select the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.