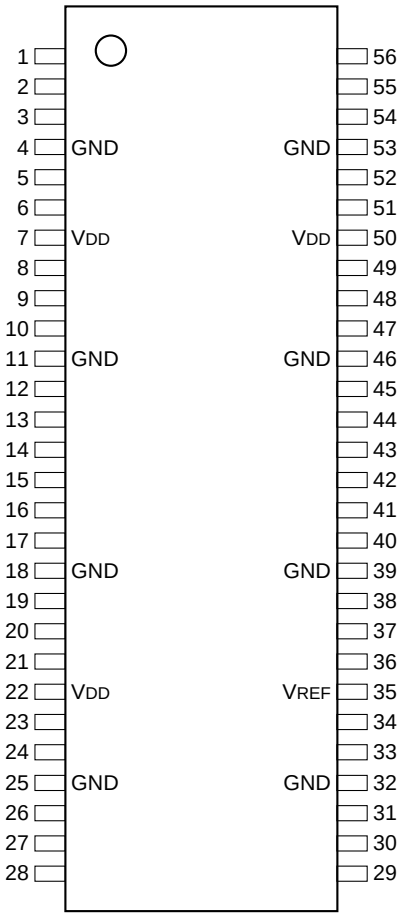
C-MOS 17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS WITH BUFFERED CLOCK OUTPUTS

—TOP VIEW—



INPUT

$\overline{CEAB}$: CLOCK ENABLE (A-TO-B DATA FLOW)
$\overline{CEBA}$: CLOCK ENABLE (B-TO-A DATA FLOW)
CLKAB : CLOCK (A-TO-B DATA FLOW)
CLKBA : CLOCK (B-TO-A DATA FLOW)
CLKIN : CLOCK IN
LEAB : LATCH ENABLE (A-TO-B DATA FLOW)
LEBA : LATCH ENABLE (B-TO-A DATA FLOW)
$\overline{OEAB}$: OUTPUT ENABLE (A-TO-B DATA FLOW)
$\overline{OEBA}$: OUTPUT ENABLE (B-TO-A DATA FLOW)

OUTPUT

CLKOUT : CLOCK OUT

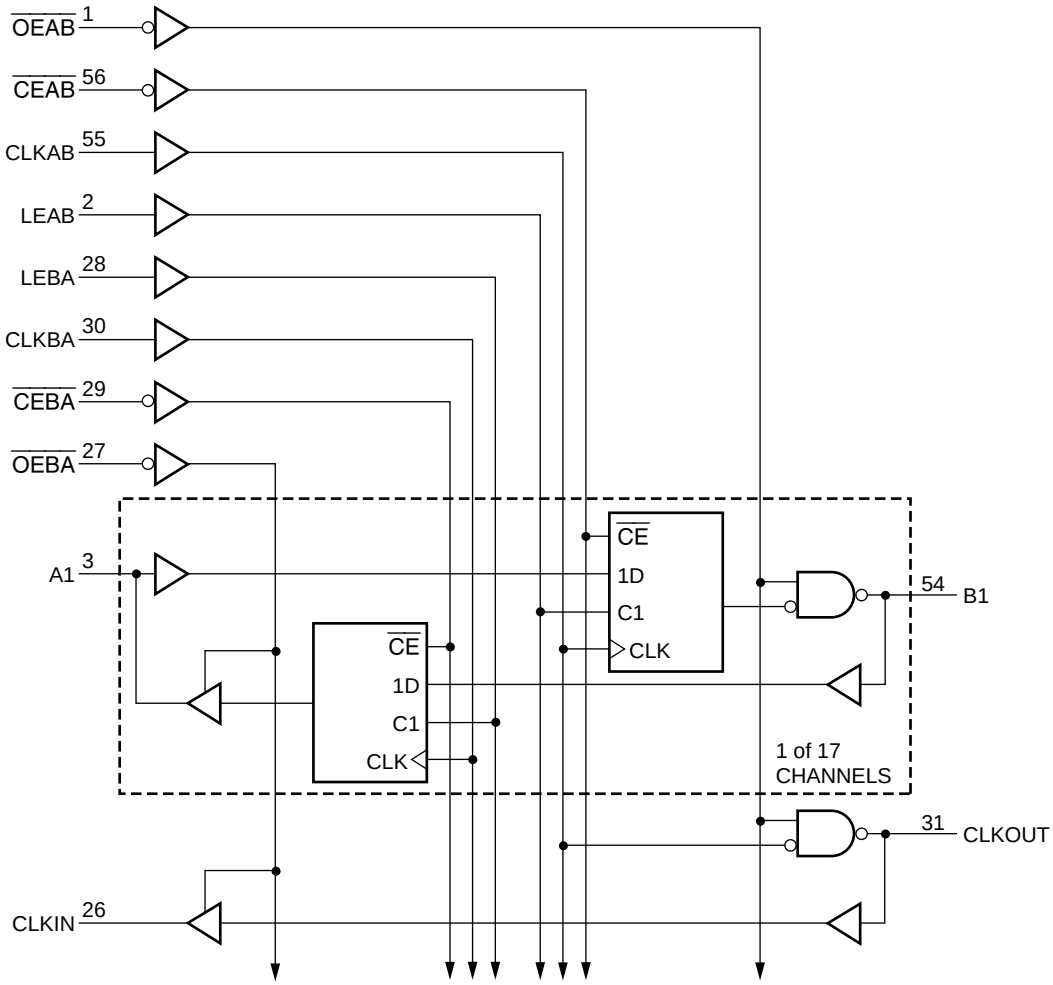
INPUT/OUTPUT

A1 - A18 : A-BUS DATA
B1 - B18 : B-BUS DATA

INPUTS					OUTPUT
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B
×	1	×	×	×	HI-Z
0	0	0	1 or 0	×	Bo
0	0	0	1 or 0	×	Bo
×	0	1	×	0	0
×	0	1	×	1	1
0	0	0	↑	0	0
0	0	0	↑	1	1
1	0	0	×	×	Bo

0 : LOW LEVEL × : DON'T CARE
1 : HIGH LEVEL HI-Z : HIGH IMPEDANCE

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{OEAB}$	15	I/O	A10	29	I	$\overline{CEBA}$	43	I/O	B9
2	I	LEAB	16	I/O	A11	30	I	CLKBA	44	I/O	B8
3	I/O	A1	17	I/O	A12	31	O	CLKOUT	45	I/O	B7
4	—	GND	18	—	GND	32	—	GND	46	—	GND
5	I/O	A2	19	I/O	A13	33	I/O	B17	47	I/O	B6
6	I/O	A3	20	I/O	A14	34	I/O	B16	48	I/O	B5
7	—	VDD	21	I/O	A15	35	—	VREF	49	I/O	B4
8	I/O	A4	22	—	VDD	36	I/O	B15	50	—	VDD
9	I/O	A5	23	I/O	A16	37	I/O	B14	51	I/O	B3
10	I/O	A6	24	I/O	A17	38	I/O	B13	52	I/O	B2
11	—	GND	25	—	GND	39	—	GND	53	—	GND
12	I/O	A7	26	I	CLKIN	40	I/O	B12	54	I/O	B1
13	I/O	A8	27	I	$\overline{OEBA}$	41	I/O	B11	55	I	CLKAB
14	I/O	A9	28	I	LEBA	42	I/O	B10	56	I	$\overline{CEAB}$


OEAB
1
CEAB
56
CLKAB
55
LEAB
2
LEBA
28
CLKBA
30
CEBA
29
OEBA
27
A1
3
CE
1D
C1
CLK
54
B1
1 of 17
CHANNELS
31
CLKOUT
CLKIN
26