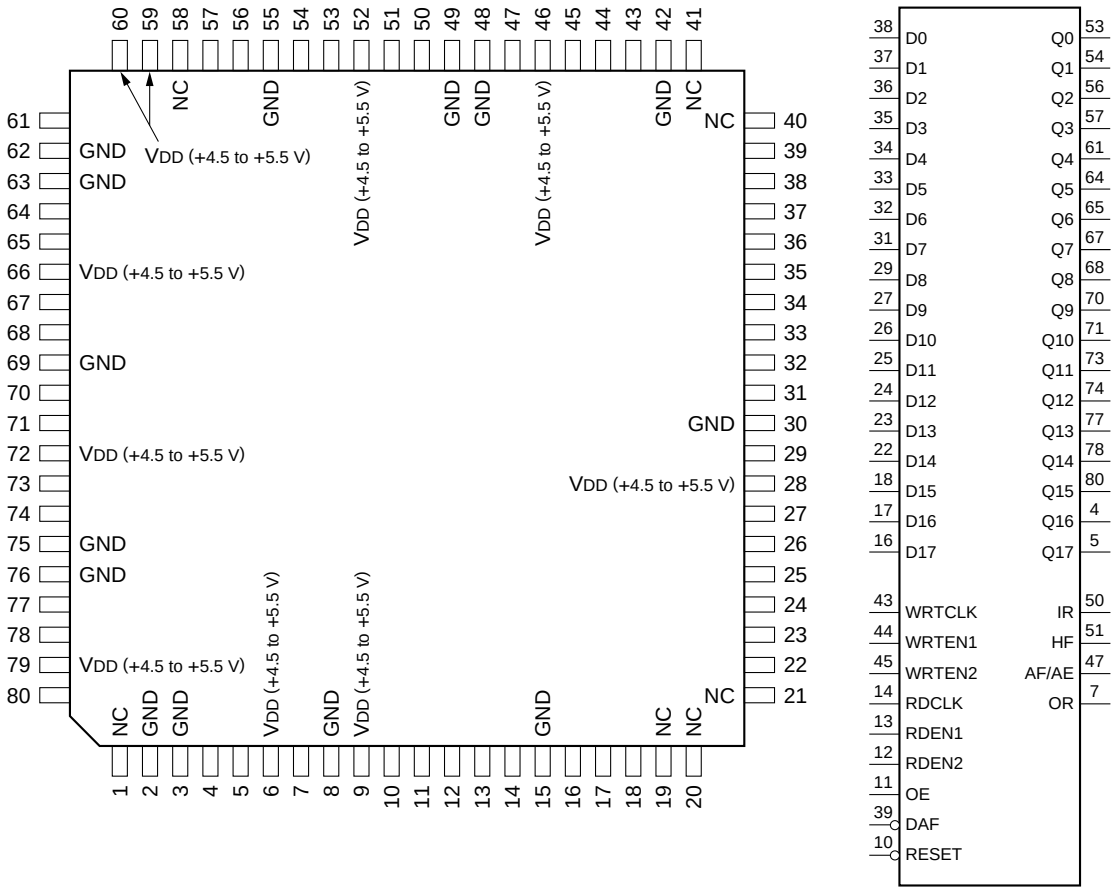
C-MOS 1024 × 18 CLOCKED FIRST-IN/FIRST-OUT MEMORY

—TOP VIEW—



(VDD = +4.5 to +5.5 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	21	—	NC	41	—	NC	61	O	Q4
2	—	GND	22	I	D14	42	—	GND	62	—	GND
3	—	GND	23	I	D13	43	I	WRTCLK	63	—	GND
4	O	Q16	24	I	D12	44	I	WRTEN1	64	O	Q5
5	O	Q17	25	I	D11	45	I	WRTEN2	65	O	Q6
6	—	VDD	26	I	D10	46	—	VDD	66	—	VDD
7	O	OR	27	I	D9	47	O	AF/AE	67	O	Q7
8	—	GND	28	—	VDD	48	—	GND	68	O	Q8
9	—	VDD	29	I	D8	49	—	GND	69	—	GND
10	I	$\overline{\text{RESET}}$	30	—	GND	50	O	IR	70	O	Q9
11	I	OE	31	I	D7	51	O	HF	71	O	Q10
12	I	RDEN2	32	I	D6	52	—	VDD	72	—	VDD
13	I	RDEN1	33	I	D5	53	O	Q0	73	O	Q11
14	I	RDCLK	34	I	D4	54	O	Q1	74	O	Q12
15	—	GND	35	I	D3	55	—	GND	75	—	GND
16	I	D17	36	I	D2	56	O	Q2	76	—	GND
17	I	D16	37	I	D1	57	O	Q3	77	O	Q13
18	I	D15	38	I	D0	58	—	NC	78	O	Q14
19	—	NC	39	I	$\overline{\text{DAF}}$	59	—	VDD	79	—	VDD
20	—	NC	40	—	NC	60	—	VDD	80	O	Q15

INPUT

$\overline{DAF}$	:	DEFINE-ALMOST FULL
$\overline{RESET}$	:	RESET
D0 - D17	:	18-BIT WIDE DATA
OE	:	OUTPUT ENABLE
RDCLK	:	READ CLOCK
RDEN1, RDEN2	:	READ ENABLE
WRTCLK	:	WRITE CLOCK
WRTEN1, WRTEN2	:	WRITE ENABLE

OUTPUT

AF/AE	:	ALMOST-FULL/ALMOST-EMPTY FLAG
HF	:	HALF-FULL FLAG
IR	:	INPUT-READY FLAG
OR	:	OUTPUT-READY FLAG
Q0 - Q17	:	DATA