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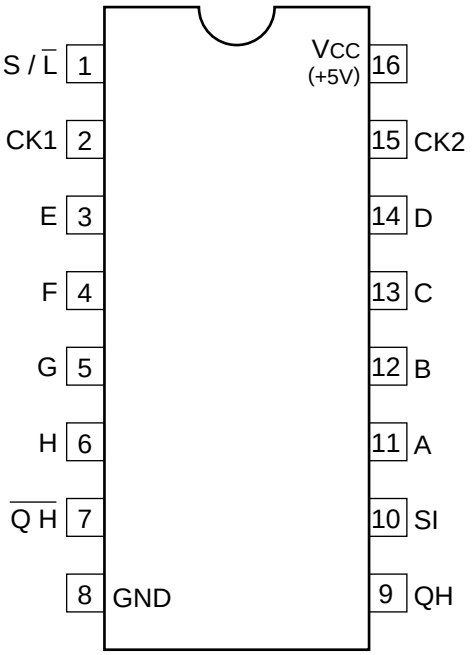
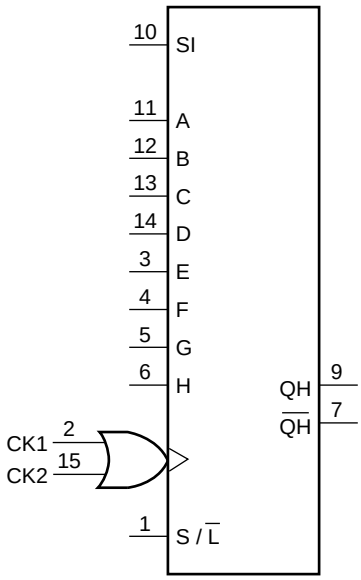
TTL PARALLEL-LOAD OR SERIAL-IN 8-BIT SHIFT REGISTER

-TOP VIEW-





SI ; SERIAL DATA IN
A – H ; PARALLEL DATA IN
CK1, CK2 ; CLOCK IN (↑)
S / L̄ ; SHIFT / LOAD IN
QH, Q H̄ ; 8th BIT OUT (COMPLEMENTALY)

INPUTS				CONTENTS		OUTPUT	OPERATION
S / L̄	CK1 + CK2	SI	A·····H	QA	QB·····	QH	
0	×	×	a·····h	a	b·····	h	PARALLEL LOAD
1	↑	0	×	0	QAo....	QGo	RIGHT SHIFT
1	↑	1	×	1	QAo....	QGo	
1	↓	×	×	QAo	QBo....	QHo	NO COUNT
1	0	×	×	QAo	QBo....	QHo	
1	1	×	×	QAo	QBo....	QHo	

0 ; LOW LEVEL 1 ; HIGH LEVEL × ; DON'T CARE

a – h ; LEVEL OF INPUTS A – H

QAo – QHo ; LEVEL OF QA – QH BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED