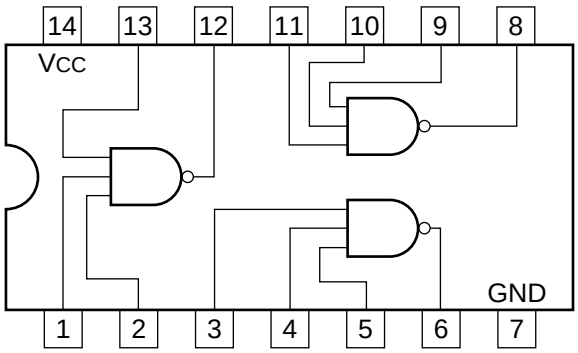
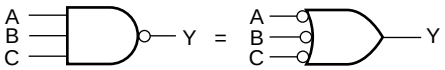
TTL 3-INPUT POSITIVE NAND GATE

—TOP VIEW—





$Y = \overline{A} \bullet \overline{B} \bullet \overline{C} = \overline{A + B + C}$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL