SM5L1/5L2/5L3

4-Bit Single-Chip Microcomputer (LCD Driver)

DESCRIPTION

The SM5L1/5L2/5L3 is CMOS 4-bit single-chip microcomputers operated in single 1.5 V power supply. This microcomputer integrates 4-bit parallel processing function, ROM, RAM, display RAM, 15-stage divider, 2-kind of interrupt and 4-level of subroutine stack. With a built-in LCD drive circuit for maximum of 84/136/168/ (SM5L1/5L2/5L3) elements, a 2-mode standby function, and a melody generator circuit in a single chip, the SM5L1/5L2/5L3 permits the design of system configuration with a minimum of peripheral components. It can be used in a variety of products from handheld equipment to electrical appliances, such as audio timers, and also achieves low power consumption.

FEATURES

- ROM capacity : 2 048 x 8 bits (SM5L1)
  3 072 x 8 bits (SM5L2)
  4 096 x 8 bits (SM5L3)
- RAM capacity :
  69 x 4 bits (including 21 x 4 bits display RAM) (SM5L1)
  130 x 4 bits (including 34 x 4 bits display RAM) (SM5L2)
  170 x 4 bits (including 42 x 4 bits display RAM) (SM5L3)
- Instruction sets : 51
- Subroutine nesting : 4 levels
- I/O port :

Input	1
Output	5
Input/output	8

- Interrupts :

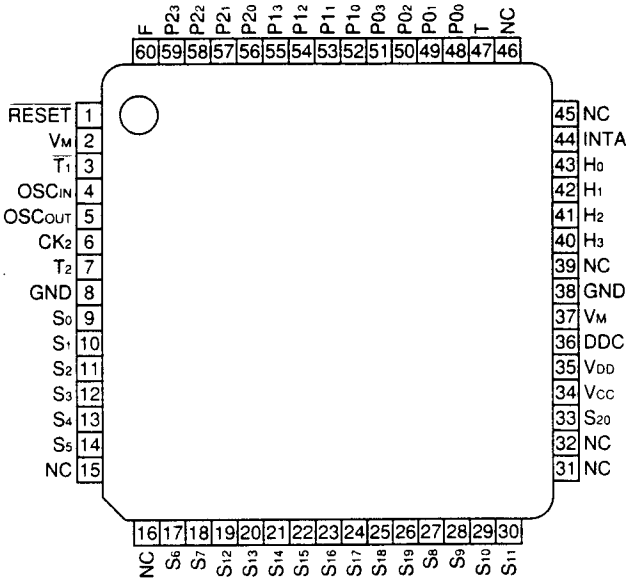
Internal interrupt	x 1 (INTA)
External interrupt	x 1 (divider overflow)

- Built-in main clock oscillator for system clock
- Signal generation for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver :
  84 segments (SM5L1) / 136 segments (SM5L2) / 168 segments (SM5L3), 1/2 bias, 1/4 duty cycle
- Built-in melody generator circuit :
  Melody ROM
  160 steps (SM5L1), 256 steps (SM5L2/5L3)
  Generating time (at 32.768 kHz)
  20 s (MAX.) (SM5L1)
  32 s (MAX.) (SM5L2/5L3)
- Instruction cycle time : 61 µs (TYP., at 32.768 kHz)
- Standby function
- Supply voltage :
  1.5 V ± 10% (SM5L1)
  1.5 V ± 20% (SM5L2/5L3)
- Packages :
  60-pin QFP (QFP060-P-1414) (SM5L1)
  72-pin QFP (QFP072-P-1010) (SM5L2)
  80-pin QFP (QFP080-P-1420) (SM5L2/5L3)

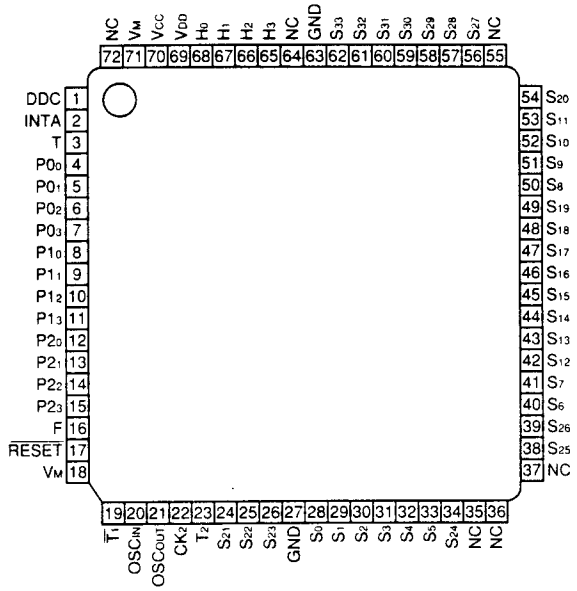
PIN CONNECTIONS

TOP VIEW

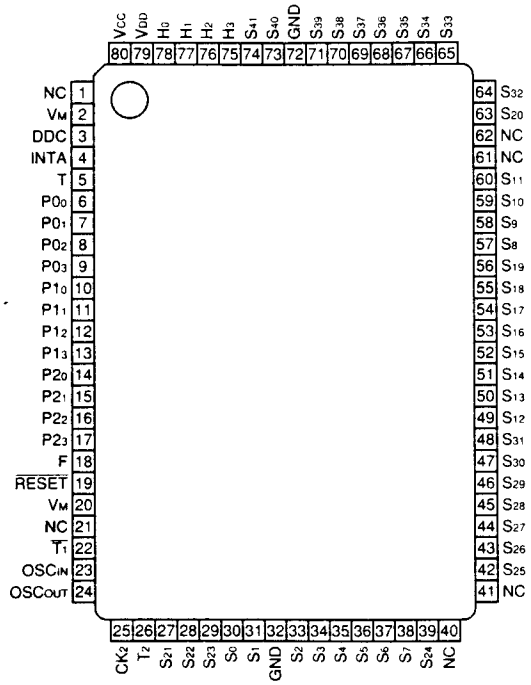
60-PIN QFP (SM5L1)



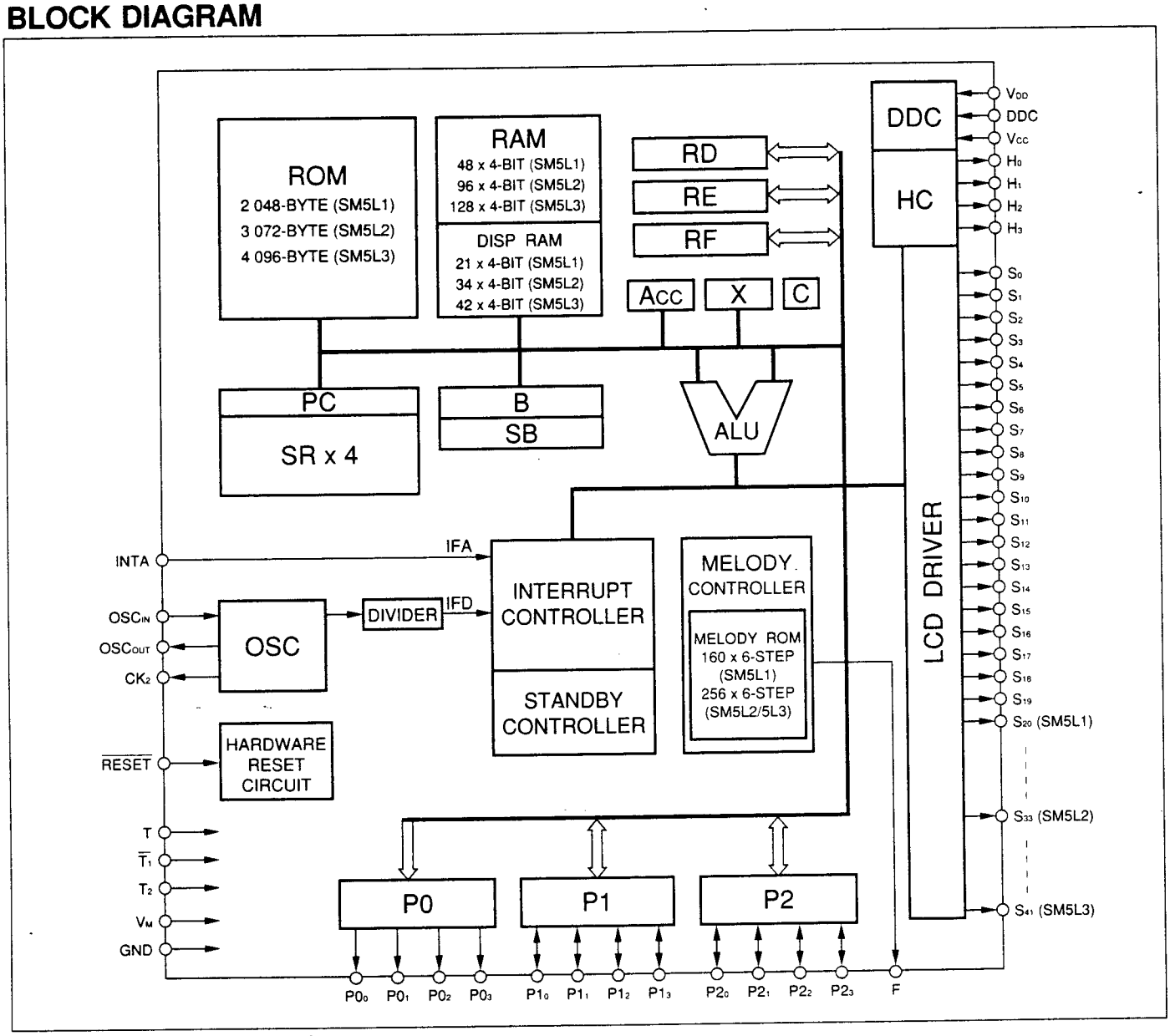
72-PIN QFP (SM5L2)



80-PIN QFP (SM5L2/SM5L3)



BLOCK DIAGRAM



Nomenclature

ACC	: Accumulator
ALU	: Arithmetic logic unit
B	: RAM address register
C	: Carry flag
DDC	: Display boost circuit
HC	: Backplate signal generator circuit
IFA	: External interrupt flag
IFD	: Divider overflow flag
OSC	: System clock oscillator
P0-P2	: Port registers
PC	: Program counter
RAM	: Data memory
RD, RE, RF	: Mode registers
ROM	: Program memory
SB	: Stack B register
SR	: PC stack register
X	: X register

PIN DESCRIPTIONS

PIN NAME	I/O	FUNCTION
GND, V_M	I	Power supply pins. The V_M pin applies a positive supply with respect to the GND.
T, $\overline{T_1}$, T_2	I	LSI chip test pins. Cannot be used by the user. Connect T and T_2 pin to GND. Connect $\overline{T_1}$ pin to V_M.
$\overline{RESET}$	I	Input pin with built-in pull-up register. Hardware-reset the LSI chip when a Low level signal is input. Normally, a capacitor is connected between it and GND to form a power-on reset circuit.
OSC_{IN}, OSC_{OUT}, CK_2	I/O	CR or crystal oscillator pins. Connect a CR or crystal oscillating element across [OSC_{IN} - OSC_{OUT} (crystal)] or [OSC_{IN} - CK_2 (CR)] to form a clock generator circuit. (Use of a CR or crystal oscillating element is determined by the mask option)
F	O	Melody output pin. Outputs the contents of a melody ROM with 12-musical scale (555 to 2114 Hz) in two octaves.
H_0-H_3	O	Backplate output pins. Pins for the LCD's backplate signals.
S_0-S_{20} (SM5L1) S_0-S_{33} (SM5L2) S_0-S_{41} (SM5L3)	O	Pins for the LCD's segment signals.
INTA	I	Input pin for external interrupt. The IFA flag is set at the leading edge of INTA.
$P0_0$-$P0_3$	O	Output pins. The accumulator A_{CC} can be transferred to this port by instruction.
$P1_0$-$P1_3$, $P2_0$-$P2_3$	I/O	I/O pins which can switch to input or output pins in 4-bit units by instruction. They can be used as output pins when configured for a key matrix. The SM5Lx is forced to hardware-reset when all of $P1_0$ to $P1_3$ pins are High level. (By mask option)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power suppiy voltage	V_M	−0.3 to 2.0	V	
	V_{DD}	−0.3 to 4.0		
Input voltage	V_I	−0.3 to V_M + 0.3	V	
Output voltage	V_O	−0.3 to V_M + 0.3	V	
Source output current for each pin	I_{O1}	2	mA	1
	I_{O2}	2	mA	2
	I_{O3}	2	mA	3
	I_{O4}	2	mA	4
Sink output current for each pin	I_{O5}	2	mA	1
	I_{O6}	100	μA	2
	I_{O7}	2	mA	3
	I_{O8}	2	mA	4
Total source output current	I_{OH}	10	mA	
Total sink output current	I_{OL}	10	mA	
Operating temperature	T_{OPR}	0 to 50	°C	
Storage temperature	T_{STG}	−55 to 150	°C	

NOTES :

1. Applicable pins : $P0_0$-$P0_3$
2. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
3. Applicable pins : F
4. Applicable pins : H_0-H_3, S_0-S_{20} (SM5L1), S_0-S_{33} (SM5L2), S_0-S_{41} (SM5L3)

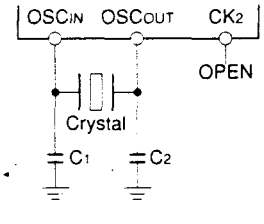
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Power supply voltage	V_M	1.35 to 1.65 (SM5L1) 1.2 to 1.8 (SM5L2/5L3)	V	
	V_{DD}	2.4 to 3.6		
Instruction cycle	T_{SYS}	122 to 50	μs	
Oscillation starting voltage	V_{OSC}	1.4	V	1

NOTE :

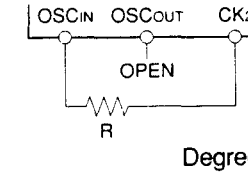
1. Use the crystal oscillation circuit

Oscillation Circuit



Crystal : 32.768 kHz
C_1 = 8 pF
C_2 = 8 pF

Crystal oscillation (frequency = 32.768 kHz)



Degree of fluctuation frequency : ± 30%
(V_M = 1.5 V, T_{OPR} = 25°C)

CR oscillation (frequency = 40 kHz)

NOTE :

Mount the R, C and crystal as close to the LSI chip as possible to minimize the effects of stray capacitance.

DC CHARACTERISTICS

(V_M = 1.5 ± 0.1 V, Ta = 0 to +50°C)

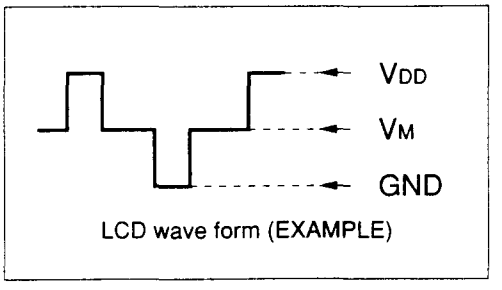
PARAMETER	SYMBOL	CONDITIONS	MIN.*1	TYP.*2	MAX.*1	UNIT	NOTE
Input voltage	V_{IH1}		0.8 x V_M		V_M	V	1
	V_{IL1}		0		0.2 x V_M		
	V_{IH2}		V_M–0.25		V_M	V	2
	V_{IL2}		0		0.25		
Input current	I_{IH1}	V_{IH} = V_M			1.0	μA	3
	I_{IH2}	V_{IH} = V_M		1.5/3/3			4
	I_{IL1}	V_{IL} = 0 V		1.5/3/3			5
Boost output voltage	V_{DD1}	V_M = 1.4 V RL = 5 MΩ	2.5			V	6
	V_{DD2}	V_M = 1.6 V RL = 5 MΩ	2.9				
Output current	$-I_{OH1}$	V_{OH} = V_M–0.5 V	100			μA	7
	I_{OL1}	V_{OL} = 0.5 V	100				
	$-I_{OH2}$	V_{OH} = V_M–0.5 V	100				8
	I_{OL2}	V_{OL} = 0.5 V	3.0				
Output impedance	D_{COM}	V_M = 1.5 V		15		kΩ	9
	D_S	V_M = 1.5 V		30			10
Supply current	I_{DA}	V_M = 1.5 V T_{SYS} = 122 μs		8/10/12	15	μA	11
	I_{DH1} (Halt mode)			5/7/8	8		12
	I_{DH2} (Halt mode)			3/4/5	5		13
	I_{DS} (Stop mode)			1/1.5/2	3		14

*1 : SM5L1's spec.

*2 : */*/* → SM5L1/5L2/5L3

NOTES :

1. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, T, INTA
3. Applicable pins : $P2_0$-$P2_3$
4. Applicable pins : T, INTA, $P1_0$-$P1_3$
5. Applicable pins : $\overline{RESET}$
6. Applicable pins : V_{DD}
7. Applicable pins : $P0_0$-$P0_3$, F
8. Applicable pins : $P1_0$-$P1_3$, $P2_0$-$P2_3$
9. Applicable pins : H_0-H_3
10. Applicable pins : S_0-S_{20} (SM5L1), S_0-S_{33} (SM5L2), S_0-S_{41} (SM5L3)
11. No-load condition. Supply current under the operation when driving a CR oscillator.
12. No-load condition. Supply current when driving a CR oscillator and turning LCD ON placed the device in halt mode.
13. No-load condition. Supply current when driving a CR oscillator and turning LCD OFF placed the device in halt mode.
14. No-load condition. Supply current when the entire system is inactivated.



LCD wave form (EXAMPLE)

Singlechip LH7xxxx ‘790 ‘789 ‘791 SMxxxx ‘K series MCU Microcontroller MPU Microprocessor ARM Advanced RISC Machines Databank LCD Controller LCD Driver Controllers Processors Portable Low Power Low Voltage High Performance Power curve MIPS MIPS/Watt Execution Cycle Multiplier High Speed Compact Handheld System on Chip System Integration Chip Integration Integration Superchip Standard Cell Core Core based IC VHDL Verilog Synthesis Chip on Board COB Chip on Flex COF Device on Board DOB Power Supply Controller Handy Products Development Tools Board Support Software Tools Tools 2.10 Software Support Emulators Evaluation Boards ICE In-Circuit Emulators ROM ICE SME Series Programmable User Configurable RTOS Real Time Operating Systems Third Party Support Software Hardware Yokogawa Digital Cosmic Compiler C Language C Like Assembler Linker Debugger Debug A/D D/A DAC Analog Digital 10-bit 4-bit 8-bit 16-bit 32-bit Address bus Data Bus