SM5K3/SM5K4 SM5K5

4-Bit Single-Chip Microcomputers (Controllers With 10-Bit A/D Converter)

DESCRIPTION

The SM5K3/5K4/5K5 are CMOS 4-bit single-chip microcomputers incorporating 4-bit parallel processing function, ROM, RAM, 10-bit A/D converter and timer/counters.

It provides three kinds of interrupts and 4 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and available in a small package : best suitable for Low power controlling, compact equipment like a precision charger.

FEATURES

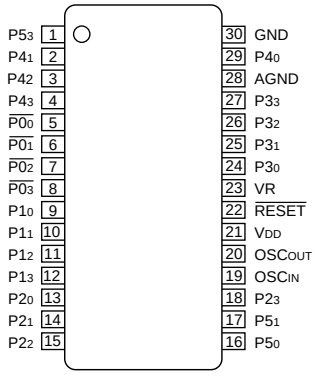
- ROM capacity : 2 048 x 8 bits
- RAM capacity : 128 x 4 bits
- Instruction sets : 50
- Subroutine nesting : 4 levels
- I/O port :
  - Input 8
  - Output 4
  - Input/output 12 (36QFP/32SOP)
    11 (30SDIP)
    8 (28SOP)
- Interrupts :
  - Internal interrupt x 1 (timer)
  - External interrupt x 2 (2 external interrupt inputs)
- A/D converter :
  - Resolution 10 bits
  - Channels 4
- Timer/counter : 8-bit x 1
- Built-in main clock oscillator for system clock
  - Ceramic/crystal oscillator (SM5K3/5K5)
  - CR oscillator (SM5K4)
- Signal generation for real time clock* (SM5K3/5K5)
- Built-in 15 stages divider
  (for real time clock* : SM5K3/5K5)
- Instruction cycle time :
  - 1 µs (MIN.) (2 MHz, at 5 V ± 10%) (SM5K3/5K5)
  - 2 µs (MIN.) (1 MHz, at 2.2 to 5.5 V) (SM5K3/5K5)
  - 1 µs (MIN.) (1.67 MHz ± 20%, at 5 V ± 10%) (SM5K4)
- Large current output pins (LED direct drive) :
  - 15mA (TYP.) x 4 (sink current)
- Supply voltages :
  - 2.2 to 5.5 V (SM5K3/5K5)
  - 2.7 to 5.5 V (SM5K4)
- Packages :
  - 30-pin SDIP (SDIP030-P-0400)
  - 32-pin SOP (SOP032-P-0525)
  - 36-pin QFP (QFP036-P-1010)
  - 28-pin SOP (SOP028-P-0450) (SM5K3/5K5)
  - 24-pin SSOP (SSOP024-P-0275) (SM5K4)

* In case of using crystal oscillator

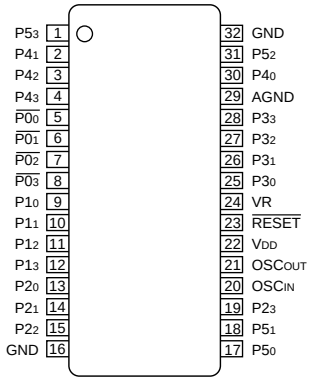
PIN CONNECTIONS

TOP VIEW

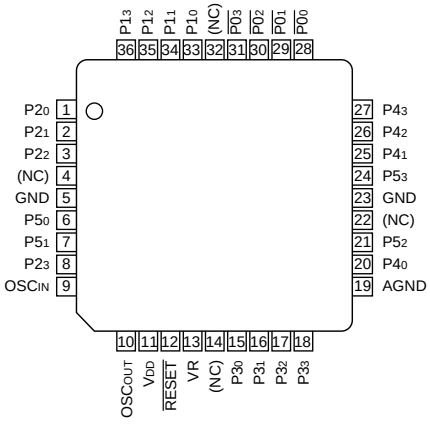
30-PIN SDIP



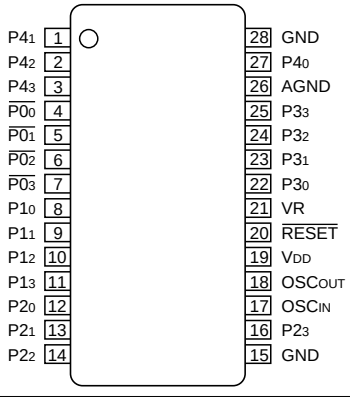
32-PIN SOP



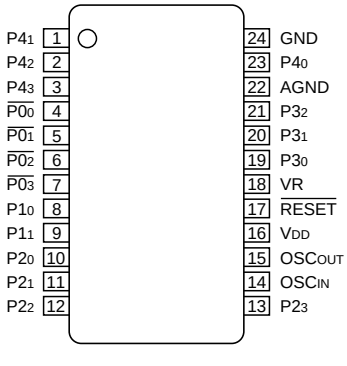
36-PIN QFP



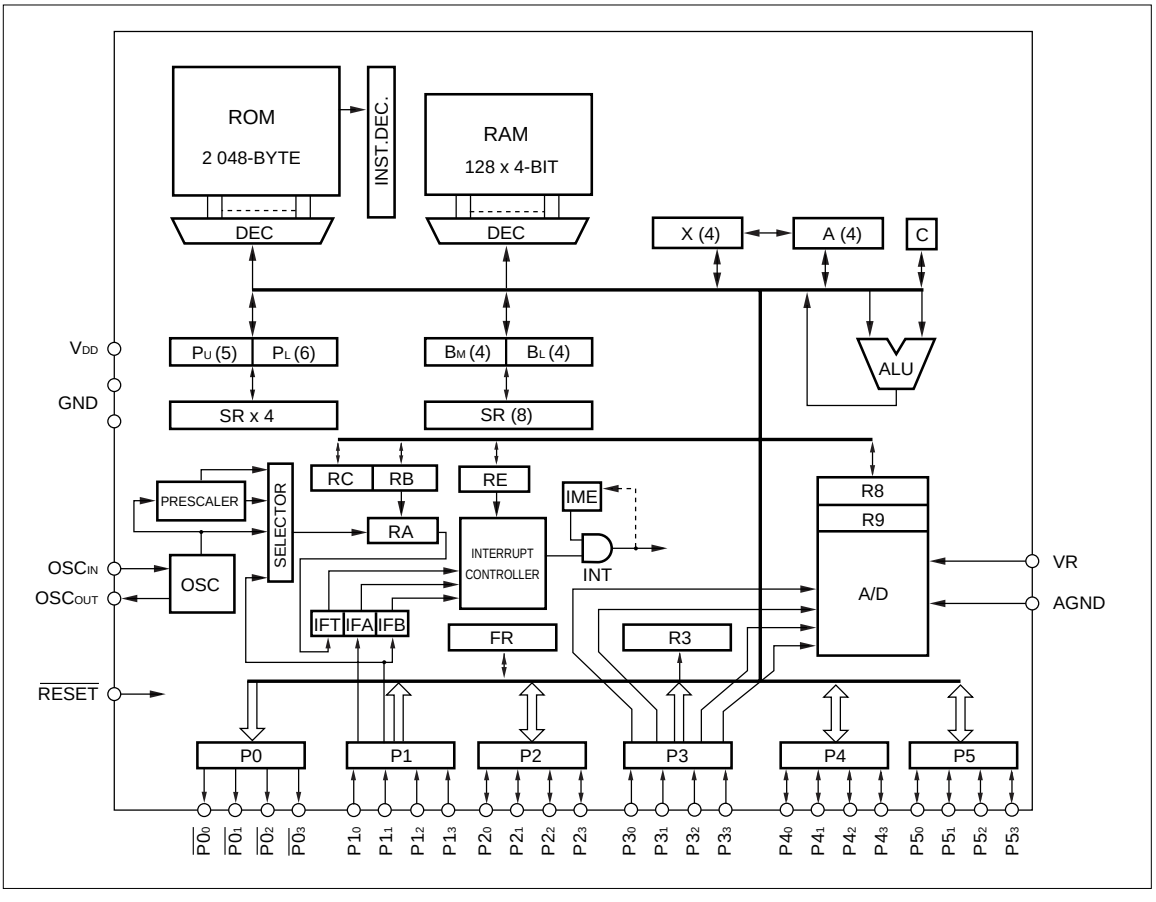
28-PIN SOP (SM5K3/5K5)



24-PIN SSOP (SM5K4)



BLOCK DIAGRAM



Nomenclature

A	: A register
A/D	: A/D converter unit
ALU	: Arithmetic logic unit
B_M, B_L	: RAM address register
C	: Carry flag
IFA, IFB, IFT	: Interrupt request flag
IME	: Interrupt master enable flag
INST. DEC.	: Instruction decoder
INT	: Interrupt control unit
P0-P5	: Port register
P_U, P_L	: Program counter
R8, R9, RC, RE, RF	: Mode register
RA	: Count register
RB	: Modulo register
SB	: SB register
SR	: Stack register

PIN DESCRIPTION

SYMBOL	I/O	FUNCTION
$\overline{P0_0}$-$\overline{P0_3}$	O	High current output (sink current 15 mA)
$P1_0$-$P1_1$	I	Input (standby release) (counter input : $P1_1$) with pull-up resistor
$P1_2$-$P1_3$	I	Input (standby release) with pull-up resistor
$P2_0$-$P2_3$	I/O	Input (with pull-up resistor) or output (independent)
$P3_0$-$P3_3$	I	Input (also used as analog input) with pull-up resistor
$P4_0$-$P4_3$, $P5_0$-$P5_3$	I/O	Input (with pull-up resistor) and output
OSC_{IN}, OSC_{OUT}	I/O	Ceramic/crystal oscillation pin (SM5K3/5K5)/CR oscillation pin (SM5K4)
$\overline{RESET}$	I	Reset signal input with pull-up resistor
VR, AGND	I	A/D converter reference supply input port
V_{DD}, GND	I	Power supply, Ground

NOTE :

Symbols apply to 32-pin SOP and 36-pin QFP. (In case of 30-pin SDIP, $P5_2$ does not exist. In case of 28-pin SOP, $P5_0$-$P5_3$ do not exist. In case of 24-pin SSOP, $P1_2$, $P1_3$, $P3_3$, $P5_0$-$P5_3$ pins do not exist.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{DD}+0.3	V
Output voltage	V_O		–0.3 to V_{DD}+0.3	V
Maximum output current	I_{OH}	High-level output current (all outputs)	4	mA
	I_{OL0}	Low-level output current ($\overline{P0_0}$-$\overline{P0_3}$)	30	mA
	I_{OL1}	Low-level output current (all but $\overline{P0_0}$-$\overline{P0_3}$)	4	mA
Total output current	$\sum I_{OH}$	High-level output current (all outputs)	20	mA
	$\sum I_{OL}$	Low-level output current (all outputs)	80	mA
Operating temperature	T_{OPR}		–20 to +70 (SM5K3/5K5) –20 to +85 (SM5K4)	°C
Storage temperature	T_{STG}		–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(SM5K3/5K5)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		2.2 to 5.5	V
Instruction cycle	T_{SYS}	V_{DD} = 2.2 to 5.5 V	2 to 61	µs
		V_{DD} = 5.0 V ± 10%	1 to 61	
Main clock frequency (OSC_{IN}-OSC_{OUT})	f_{OSC}	V_{DD} = 2.2 to 5.5 V	1 M to 32.768 k	Hz
		V_{DD} = 5.0 V ± 10%	2 M to 32.768 k	

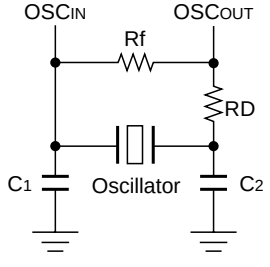
(SM5K4)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		2.7 to 5.5	V
Instruction cycle	T_{SYS}	V_{DD} = 2.7 to 5.5 V	2 to 5	µs
		V_{DD} = 5.0 V ± 10%	1 to 5	
Main clock frequency * (OSC_{IN}-OSC_{OUT})	f_{OSC}	V_{DD} = 2.7 to 5.5 V	1 M to 400 k	Hz
		V_{DD} = 5.0 V ± 10%	2 M to 400 k	

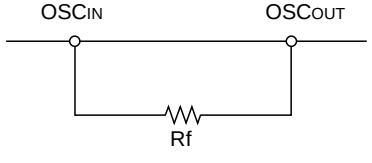
* Degree of fluctuation frequency : ± 20%

OSCILLATION CIRCUIT

• SM5K3/5K5



• SM5K4



Rf = 33 kΩ
(fosc = 1.67 MHz, TYP.)

* Reference only : Circuit configuration varies according to oscillator used.

NOTES :

- The typical oscillation frequency shall be determined in consideration of operating condition and fluctuation frequency.
- Mount Rf, RD, C_1, C_2, Oscillator (SM5K3/5K5)/Rf (SM5K4) as close as possible to the oscillator pins of the LSI, in order to reduce an influence from floating capacitance.
- Since the value of resistor Rf, RD, C_1, C_2, Oscillator (SM5K3/5K5)/Rf (SM5K4) varies depending on circuit pattern and others, the final Rf, RD, C_1, C_2, Oscillator (SM5K3/5K5)/Rf (SM5K4) value shall be determined on the actual unit.
- Don't connect any line to OSC_{IN} and OSC_{OUT} except oscillator circuit.
- Don't put any signal line across the oscillator circuit line.
- On the multilayer circuit, do not let the oscillator circuit wiring cross other circuit.
- Minimize the wiring capacitance of GND and V_{DD} .

DC CHARACTERISTICS

• **SM5K3** (T_{OPR} = –20 to +70°C, TYP. value : V_{DD} = 5.0 or 3.0 V, Unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.2 to 3.3 V	2	25	90	µA	3
			V_{DD} = 4.5 to 5.5 V	25	70	250		
	I_{IH1}	V_{IN} = V_{DD}				2		
	I_{IL2}	V_{IN} = 0 V			1.0	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}			1.0	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.2 to 3.3 V	5	15		mA	5
			V_{DD} = 4.5 to 5.5 V	15	25			
	I_{OH1}	V_O = V_{DD} – 0.5 V	V_{DD} = 2.2 to 3.3 V	0.3	1.5			
			V_{DD} = 4.5 to 5.5 V	1.0	2.2			
	I_{OL2}	V_O = 1.5 V	V_{DD} = 2.2 to 3.3 V	1.2	5.0		mA	6
			V_{DD} = 4.5 to 5.5 V	5	9.0			
	I_{OH2}	V_O = V_{DD} – 0.5 V	V_{DD} = 2.2 to 3.3 V	0.3	2.0			
			V_{DD} = 4.5 to 5.5 V	1.0	2.4			
	I_{OH3}	V_{OH} = V_{DD} – 1.0 V	V_{DD} = 2.2 to 3.3 V	0.15			mA	7
			V_{DD} = 4.5 to 5.5 V	0.5				
Supply cerrent	I_{DD}	f_{OSC} = 2 MHZ	V_{DD} = 4.5 to 5.5 V		1 200	2 500	µA	8
		f_{OSC} = 1 MHz	V_{DD} = 2.2 to 3.3 V		300	800		
			V_{DD} = 4.5 to 5.5 V		600	1 200		
		f_{OSC} = 32.768 kHz (Crystal OSC mode)	V_{DD} = 2.2 to 3.3 V		20	120		
	I_{HLT}	f_{OSC} = 2 MHz	V_{DD} = 4.5 to 5.5 V		760	1 500		
		f_{OSC} = 1 MHz	V_{DD} = 2.2 to 3.3 V		200	600		
			V_{DD} = 4.5 to 5.5 V		400	900		
		f_{OSC} = 32.768 kHz (Crystal OSC mode)	V_{DD} = 2.2 to 3.3 V		20	75		
	I_{STOP}	Ceramic OSC mode	V_{DD} = 2.2 to 3.3 V			2		
		f_{OSC} = 32.768 MHz (Crystal OSC mode)	V_{DD} = 2.2 to 3.3 V		15	40		
	I_{VR}	A/D in operation	V_{DD} = 4.5 to 5.5 V		220	450	µA	9
		A/D in stop	V_{DD} = 4.5 to 5.5 V			2	µA	10
A/D conversion	Resolution				10		bit	
	Differential linearity error	f_{OSC} = 1 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Sequential linearity error	f_{OSC} = 1 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	f_{OSC} = 1 MHz TOPR = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		

NOTES :

1. Applicable pins : $P1_2$, $P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_0$-$P4_3$ $P5_0$-$P5_3$
2. Applicable pins : $\overline{OSC_{IN}}$, $\overline{RESET}$, $P1_0$, $P1_1$
3. Applicable pins : $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (digital input mode)
4. Applicable pins : $P3_0$-$P3_3$ (analog input mode)
5. Applicable pins : $\overline{P0_0}$-$\overline{P0_3}$ (high current mode)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (output mode)*1
7. Applicable pins : $P3_0$-$P3_3$*2
8. No load (A/D conversion is stop.)
9. A/D conversion in operation (operation enable)
10. A/D conversion in stop (operation disable)

*1 In case of 32-pin SOP and 36-pin QFP. (In case of 30-pin SDIP, $P5_2$ dose not exist. In case of 28-pin SOP, $P5_0$-$P5_3$ do not exist.)

*2 P3 ports are normally used for input ports with pull-up resistor. These ports can be also used.

• **SM5K4** (T_{OPR} = –20 to +85°C, TYP. value : V_{DD} = 5.0 or 3.0 V, Unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.7 to 3.3 V	1.0	25	90	µA	3
			V_{DD} = 4.5 to 5.5 V	15	70	250		
	I_{IH1}	V_{IN} = V_{DD}				3.0		
	I_{IL2}	V_{IN} = 0 V			1.0	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}			1.0	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.7 to 3.3 V	3	15		mA	5
			V_{DD} = 4.5 to 5.5 V	12	25			
	I_{OH1}	V_O = V_{DD} – 0.5 V	V_{DD} = 2.7 to 3.3 V	0.2	1.5			
			V_{DD} = 4.5 to 5.5 V	0.8	2.2			
	I_{OL2}	V_O = 1.5 V	V_{DD} = 4.5 to 5.5 V	4.0	9.0		mA	6
	I_{OH2}	V_O = V_{DD} – 0.5 V	V_{DD} = 2.7 to 3.3 V	0.2	2.0			
			V_{DD} = 4.5 to 5.5 V	0.8	2.4			
	I_{OH3}	V_{OH} = V_{DD} – 1.0 V	V_{DD} = 4.5 to 5.5 V	0.5			mA	7
Supply current	I_{DD}	f_{OSC} = 2.0 MHz	V_{DD} = 4.5 to 5.5 V		1 200	2 800	µA	8
		f_{OSC} = 1.0 MHz	V_{DD} = 2.7 to 3.3 V		300	900		
			V_{DD} = 4.5 to 5.5 V		600	1 400		
	I_{HLT}	f_{OSC} = 2.0 MHz	V_{DD} = 4.5 to 5.5 V		760	1 700		
		f_{OSC} = 1.0 MHz	V_{DD} = 4.5 to 5.5 V		400	1 000		
	I_{STOP}	V_{DD} = 2.7 to 5.5 V				5		
	I_{VR}	A/D conversion in operation	V_{DD} = 2.7 to 3.3 V		130	350	µA	9
			V_{DD} = 4.5 to 5.5 V		220	500		
		A/D conversion in stop	V_{DD} = 2.7 to 5.5 V			3	µA	10
A/D conversion	Resolution					10	bit	
	Differential linearity error	f_{OSC} = 1.0 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Sequential linearity error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	f_{OSC} = 1 MHz, T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		
Reference clock oscillator frequency	f_{OSC}	V_{DD} = 4.5 to 5.5 V, Rf = 33 kΩ		1.34	1.67	2.0	MHz	

NOTES :

1. Applicable pins : $P1_2$, $P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_0$-$P4_3$, $P5_0$-$P5_3$ *1
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, $P1_0$, $P1_1$
3. Applicable pins : $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (digital input mode) *1
4. Applicable pins : $P3_0$-$P3_3$ (analog input mode)
5. Applicable pins : $\overline{P0_0}$-$\overline{P0_3}$ (high current output)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (output mode) *1
7. Applicable pins : $P3_0$-$P3_3$ *2
8. No load (A/D conversion in stop)
9. A/D conversion in operation (A/D conversion enable)
10. A/D conversion in stop (A/D conversion disable)

*1 In case of 32-pin SOP and 36-pin QFP.
(In case of 30-pin SDIP, $P5_2$ pin dose not exist. In case of 24-pin SSOP, $P1_2$, $P1_3$, $P3_3$, $P5_0$-$P5_3$ pins do not exist.)

*2 P3 ports are normally used for input port with pull-up resistor. These ports can be also used as a suspected case of output port.

• **SM5K5** (T_{OPR} = –20 to +70°C, TYP. value : V_{DD} = 5.0 or 3.0 V, Unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}			0.8 x V_{DD}		V_{DD}	V	1
	V_{IL1}			0		0.2 x V_{DD}		
	V_{IH2}			0.9 x V_{DD}		V_{DD}	V	2
	V_{IL2}			0		0.1 x V_{DD}		
Input current	I_{IL1}	V_{IN} = 0 V	V_{DD} = 2.2 to 3.3 V	2	25	90	µA	3
			V_{DD} = 4.5 to 5.5 V	25	70	250		
	I_{IH1}	V_{IN} = V_{DD}				2		
	I_{IL2}	V_{IN} = 0 V			1	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}			1	10		
Output current	I_{OL1}	V_O = 1.0 V	V_{DD} = 2.2 to 3.3 V	5	15		mA	5
			V_{DD} = 4.5 to 5.5 V	15	25			
	I_{OH1}	V_O = V_{DD}–0.5 V	V_{DD} = 2.2 to 3.3 V	0.3	1.5			
			V_{DD} = 4.5 to 5.5 V	1.0	2.2			
	I_{OL2}	V_O = 0.5 V	V_{DD} = 2.2 to 3.3 V	7	35		µA	6
			V_{DD} = 4.5 to 5.5 V	20	60			
	I_{OH2}	V_O = V_{DD}–0.5 V	V_{DD} = 2.2 to 3.3 V	300	2 000			
			V_{DD} = 4.5 to 5.5 V	1 000	2 400			
Supply current	I_{DD}	f_{OSC} = 2 MHz	V_{DD} = 4.5 to 5.5 V		1 200	2 500	µA	7
		f_{OSC} = 1 MHz	V_{DD} = 2.2 to 3.3 V		300	800		
			V_{DD} = 4.5 to 5.5 V		600	1 200		
		f_{OSC} = 32.768 kHz (Crystal OSC mode)	V_{DD} = 2.2 to 3.3 V		20	120		
			V_{DD} = 4.5 to 5.5 V		40	160		
	I_{HLT}	f_{OSC} = 2 MHz	V_{DD} = 4.5 to 5.5 V		760	1 500	µA	7
		f_{OSC} = 1 MHz	V_{DD} = 4.5 to 5.5 V		400	900		
		f_{OSC} = 32.768 kHz (Crystal OSC mode)	V_{DD} = 2.2 to 3.3 V		15	60		
			V_{DD} = 4.5 to 5.5 V		20	90		
	I_{STOP}	Ceramic OSC mode	V_{DD} = 2.2 to 3.3 V			2		
		f_{OSC} = 32.768 kHz (Crystal OSC mode)	V_{DD} = 2.2 to 3.3 V		2	10		
			V_{DD} = 4.5 to 5.5 V		10	25		
	I_{VR}	A/D in operation	V_{DD} = 2.2 to 3.3 V		130	300	µA	8
			V_{DD} = 4.5 to 5.5 V		220	450		
		A/D in stop	V_{DD} = 2.2 to 5.5 V			2	µA	9
A/D conversion	Resolution				10		bit	
	Differential linearity error	f_{OSC} = 1 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 2.5	± 4.0	LSB	
	Sequential linearity error	f_{OSC} = 1 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 3.2	± 5.0		
	Total error	f_{OSC} = 1 MHz T_{OPR} = 25°C	V_{DD} = VR = 5.0 V		± 4.0	± 6.0		

NOTES :

1. Applicable pins : $P1_2$, $P1_3$, $P2_0$-$P2_3$, $P3_0$-$P3_3$ (digital input mode), $P4_0$-$P4_3$, $P5_0$-$P5_3$[*1]
2. Applicable pins : OSC_{IN}, $\overline{RESET}$, $P1_0$, $P1_1$
3. Applicable pins : $\overline{RESET}$, $P1_0$-$P1_3$, $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (digital input mode)[*1]
4. Applicable pins : $P3_0$-$P3_3$ (analog input mode)
5. Applicable pins : $\overline{P0_0}$-$\overline{P0_3}$ (high current port)
6. Applicable pins : $P2_0$-$P2_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$ (output mode)[*1]
7. No load (A/D conversion in stop)
8. A/D conversion in operation (operation enable)
9. A/D conversion in stop (operation disable)

*1 In case of 32-pin SOP and 36-pin QFP.
(In case of 30-pin SDIP, $P5_2$ dose not exist. In case of 28-pin SOP, $P5_0$-$P5_3$ do not exist.)

SYSTEM CONFIGURATION

A Register and X Register

The A register (or accumulator : A_{CC}) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register. When the table reference instruction PAT is used, the X and A registers load ROM data. A pair of A and X registers can accommodate 8-bit data.

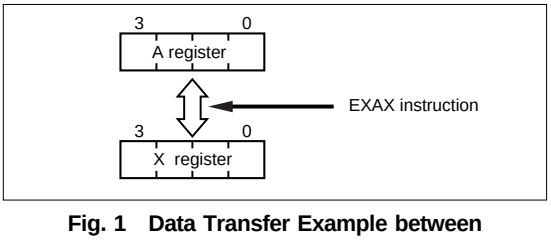


Fig. 1 Data Transfer Example between A Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation

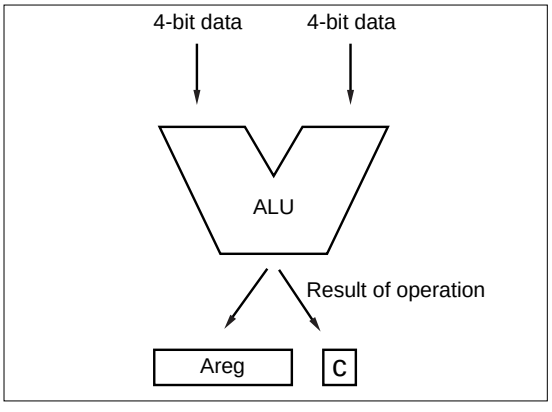


Fig. 2 ALU

The ALU operates binary addition in conjunction with RAM, C flag and A register. The carry signal Cy is generated if a carry occurs during ALU operation. Some instructions use Cy : ADC instruction sets/clears the content of the C flag; ADX instruction causes the program to skip the next instruction. Note that Cy is the symbol for carry signal and not for C flag.

B Register and SB Register

• B register (B_M, B_L)

The B register is an 8-bit register that is used to specify the RAM address. The upper 4-bit section is called B_M register and lower 4-bit B_L.

• SB register

The SB register is an 8-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

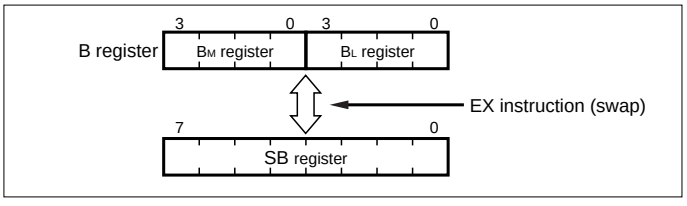


Fig. 3 B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used to store data up to 4 x 16 x 8 = 512 bits.

Word (0-F_H)

B_M \ B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																※

File (0-7)

※ 1 word = 4-bit

Fig. 4 RAM File and Word

Program Counter PC and Stack Register SR

The program counter PC specifies the ROM address. The PC consists of 12-bit as shown in Fig. 5 : The upper 6-bit (P_U) represents a page while the lower 6-bit (P_L) denotes a step. The P_U section is a register and the P_L section, a binary counter.

Execution of interrupt handling and the table reference instruction PAT also automatically uses 1 stage of the stack register SR.

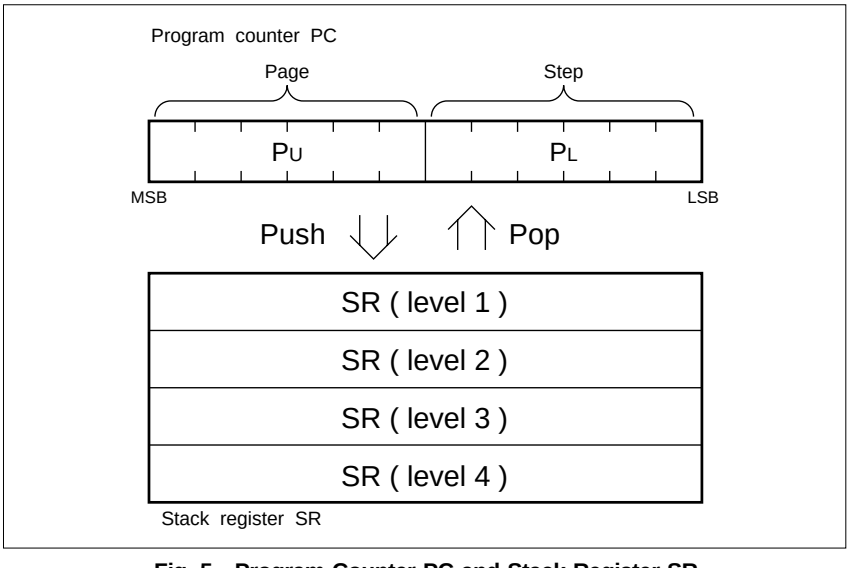


Fig. 5 Program Counter PC and Stack Register SR

Program Memory (ROM)

The ROM is used to store the program. The capacity of the ROM is 2 048-step (32-page by 64-step. See Fig. 6). The configuration of the ROM and program jumps are illustrated in Fig. 7.

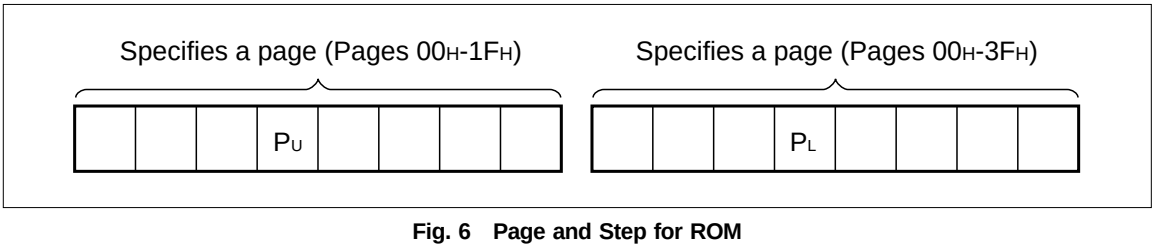
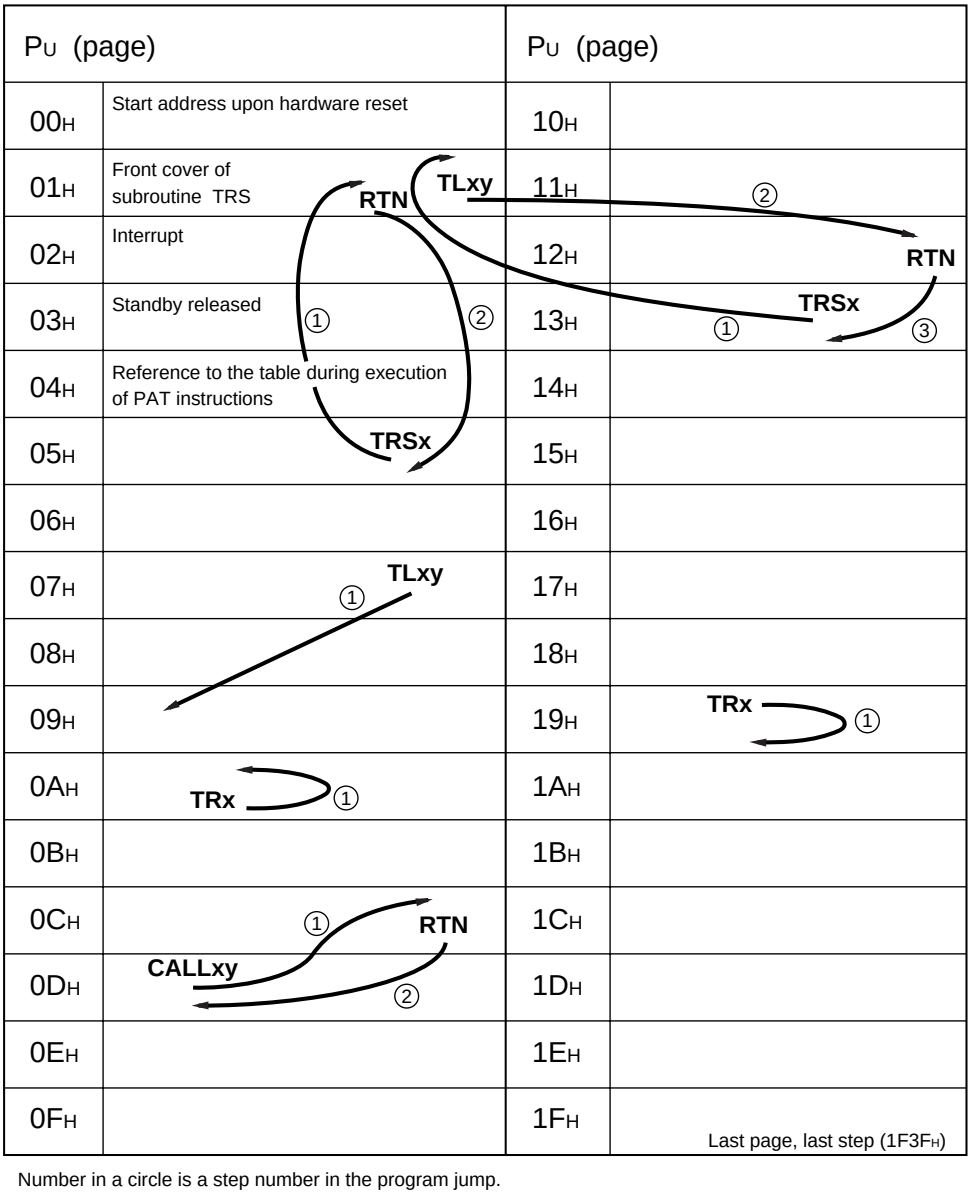


Fig. 6 Page and Step for ROM



Number in a circle is a step number in the program jump.

Fig. 7 ROM Configuration and Program Jump Example

Output Latch Register and Mode Register

The SM5K3/5K4/5K5 contain 6 output-latch registers and 8 mode-registers which either latch contents of output ports or control some functions of the SM5K3/5K4/5K5.

These registers, their functions and available transfer instructions are shown in Table 1 below.

An output latch register sets the output level of the pin to which it is connected.

Refer to the section of "MODE REGISTERS" concerning about the details mode registers.

Table 1 Output Latch Registers and Mode Registers

SYMBOL	FUNCTION	OUT	INL	OUT	IN/TPB	ANP/ORP	CONTENT OF B_L
P0	Output register	O	–	O	–	O	0
P1	Input register	–	O	–	O	–	1
P2	I/O register (independent)	–	–	O	O	O	2
P3	Input register (and analog input)	–	–	–	O	–	3
R3	Control register	–	–	O	–	–	3
P4	I/O register	–	–	O	O	O	4
P5	I/O register	–	–	O	O	O	5
R8*	A/D data/control register	–	–	O	O	–	8
R9*	A/D data register	–	–	O	O	–	9
RA*	Timer/counter register	–	–	O	O	–	A
RB*	Timer/modulo register	–	–	O	O	–	B
RC	Timer control register	–	–	O	O	–	C
RE	Interrupt mask register	–	–	O	O	–	E
RF	P2 directional register	–	–	O	O	–	F

* 8-bit register

NOTE :

Bit 4 (R84) in the R8 register is read only.

(Read or write operation of this bit does not affect any other operation.)

FUNCTIONAL DESCRIPTION

Hardware Reset Function

Reset function initializes the SM5K3/5K4/5K5 systems. When the input on the $\overline{\text{RESET}}$ pin goes Low, the system enters reset condition after 2 command cycles. After the $\overline{\text{RESET}}$ pin goes High level, the reset condition is removed as the input pulse from OSC_{IN} pin repeats 2^{15} times, forcing the program counter to start at 0 page and 0 address. Initialized status of the system immediately after resetting is shown below.

Table 2 Status of Flags and Registers Immediately after Reset

FLAG REGISTER	STATUS	FLAG REGISTER	STATUS
PC	0	IFA flag	0
SP	Level 1	IFB flag	0
RAM	Undefined	IFT flag	0
Register A	Undefined	IME flag	0
Register X	Undefined	C flag	Undefined
P0, P2, P4, P5 output latch register	0	B_M, B_L registers, SB register	Undefined
Timers (RA, RB), divider	0	R3, R8*, R9, RC, RE, RF	0

* The content of the bit R84 is undefined because it is read only.

Reset causes the following changes.

1) I/O pins are set input.
2) All mode registers are reset.
3) Output latch register P0 is reset, causing $\overline{P0_0}$ to $\overline{P0_3}$ pins go High level.
4) Interrupt request flags (IFA, IFB, and IFT), interrupt master enable flag (IME) are reset, disabling all interrupts.

Standby Feature

The standby function saves power by stopping the program whenever it is not necessary to run. The mode in which the microcomputer is executing the program is called the run mode and the mode in which it stops the program is called the standby mode. Standby mode is further divided into two modes : stop mode and halt mode, one of which is selected by halt instruction or stop instruction. Upon removal of standby condition, the SM5K3/5K4/5K5 return from the standby mode to the normal run mode. To enter the standby mode, select either stop mode or halt mode whichever is appropriate (Fig. 8).

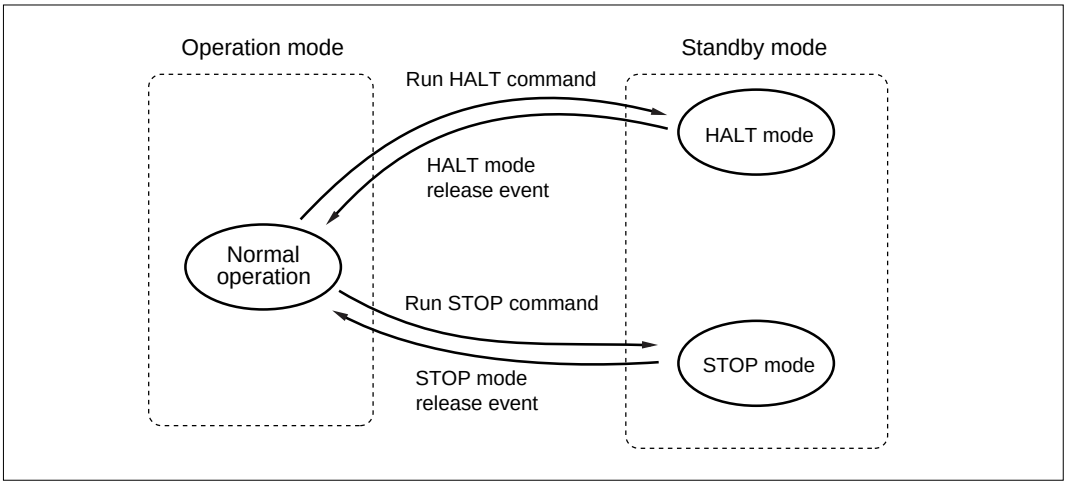


Fig. 8 Operation Shift of Program

• Blocks stopped during standby mode

In the halt mode

The system clock generating circuit stops during the halt mode, deactivating all the blocks driven by the system clock. The main clock and dividers remain active. This means that timers can be used while in the halt mode. Both internal and external clocks can be used as the count clock.

In the stop mode

The main clock and system clock stop upon entering the stop mode. Therefore, only timers using the external clock remain active.

• Counters that the system retains during standby mode

The contents that will be retained in the halt mode will also be retained in the stop mode. These items are shown in Table 3.

Table 3 System Contents Secured During Standby Mode

FLAG	REGISTER	OUTPUT LATCH REGISTER/MODE REGISTER	OTHER
IFA flag	A register	P0, P2, R3, P5	RAM
IFB flag	X register	R8, R9, RA, RB	
IFT flag	B_M, B_L register	RC, RE, RF	
IME flag	SP		
C flag	SR		

• Releasing events of standby mode (6-type)

RELEASING EVENT	FLAG	INT/EXT	MASKABLE / NONMASKABLE	PRIORITY
Reset input	–	External	Nonmaskable	–
Low level input on $P1_0$ pin	IFA	External	Maskable	1
Low level input on $P1_1$ pin	IFB	External	Maskable	2
Low level input on $P1_2$ pin	–	External	Nonmaskable	–
Low level input on $P1_3$ pin	–	External	Nonmaskable	–
Timer overflow	IFT	Internal	Maskable	3

• Usage of halt mode and stop mode

The system returns back to the normal operation mode upon occurring of a standby mode releasing condition. The halt mode should be used when the system must enter and exit normal operation frequently as in the case of key operation.

The halt mode should also be used to keep timers that are operating from the internal clock, while in the standby mode.

The stop mode further saves power than the halt mode but requires slightly longer time to return to the normal mode. Therefore, the stop mode should be used when the system will not be required to return to the normal mode in a short time.

Interrupt Feature

The interrupt block consists of mask flags (bits RE0, RE1 and RE2), IME flag and interrupt request handling circuit. Fig. 9 shows the configuration of the interrupt block.

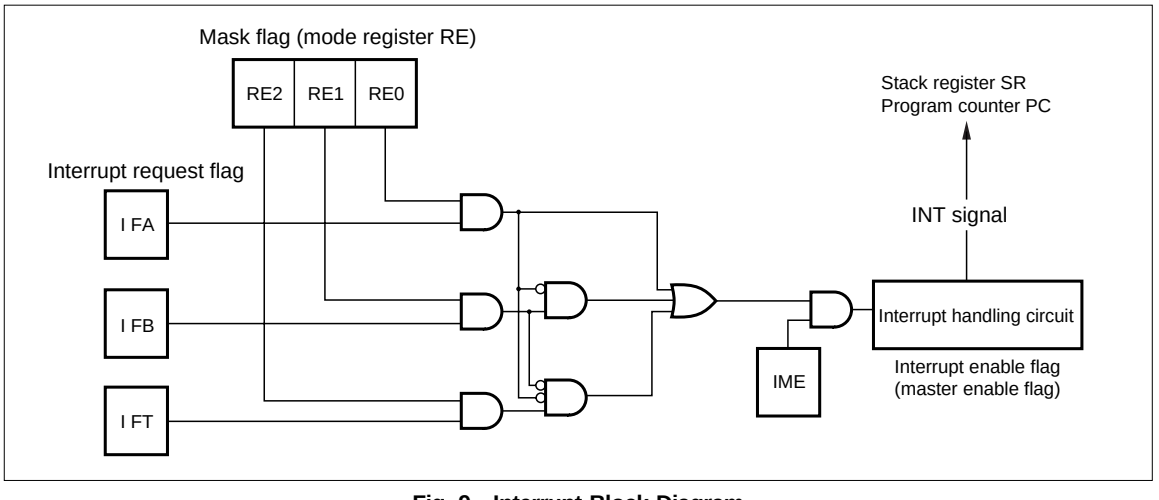


Fig. 9 Interrupt Block Diagram

• Interrupt used with SM5K3/5K4/5K5

Interrupt event occurs on the falling edge of $P1_0$ or $P1_1$ pin input, or the overflow at the timer. These events set flags IFA, IFB and IFT respectively, that then serve as interrupt request flag.

Table 4 shows interrupt handling priority level and jump address.

Table 4 Interrupt Event Summary

INTERRUPT EVENT (REQUEST FLAG)	JUMP ADDRESS		PRIORITY ORDER	INTERRUPT MASK FLAG
	PAGE	STEP		
Falling edge of input on $P1_0$ (IFA)	2	0	1	RE0
Falling edge of input on $P1_1$ (IFB)	2	2	2	RE1
Timer overflow (IFT)	2	4	3	RE2

• IME flag (master enable flag)

The IME enables or disables all interrupts at the same time. The IE command, when executed, sets the IME flag and enables the interrupt specified by the mask flag setting. The ID command resets the IME flag, disabling process of any interrupt request. Setting the IME flag to reset after releasing hardware reset, all interrupts are inhibited.

• Mode register RE (interrupt mask flag)

The mode register RE (RE0, RE1 and RE2; interrupt mask flag) individually enables or disables three type of interrupts.

Timer/Counter

The SM5K3/5K4/5K5 have a pair of built-in timer/counter. The timer/counter are used to handle periodic interrupts and to count. The overflowing timer can be used to disable the halt mode. The timer/counter serve as interval timer.

The timer/counter consists of an 8-bit count register RA, modulo register RB (for counter initial value setting), 15-bit divider and 4-bit mode register RC (for count clock selection). The configuration of the timer/counter is shown in Fig. 10.

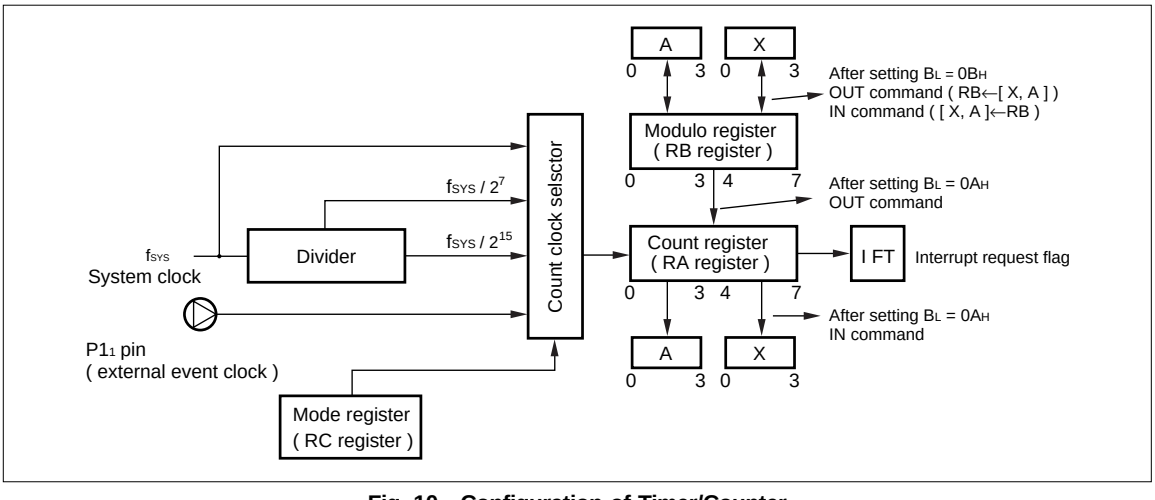


Fig. 10 Configuration of Timer/Counter

• Selecting count clock

A count clock is selected by the bit settings in the mode register RC.

Table 5 Count Clock Selection

LOWER 2-BIT OF RC BITS		SELECTED COUNT CLOCK
1	**0**	
0	0	f_{SYS} (system clock)
0	1	$f_{SYS}/2^7$
1	0	$f_{SYS}/2^{15}$
1	1	External event clock ($P1_1$)

A/D Conversion

The SM5K3/5K4/5K5 are provided with a built-in 10-bit A/D converter having 4-channel multiplexer analog inputs. The A/D converter operates in A/D conversion mode and comparison mode. In the A/D conversion mode, the converter converts the analog input from the P3 pin to the digital value; and in the comparison mode, it compares the input analog amplitude with that of a reference voltage set inside the SM5K3/5K4/5K5. The $P3_0$ to $P3_3$ pins can be used as analog voltage inputs. One or more of these 4 inputs can be set to assume A/D pin by the bit operation of the mode register R3. One of these A/D pins is further set as analog input by the bit operation of the mode register R8. The A/D converter is controlled by the bits set in the mode register R8. For details of the mode register R8, refer to " MODE REGISTERS R8 ".

Configuration of the A/D converter is illustrated in Fig. 11.

CAUTIONS

- Keep the A/D converter reference voltage on the VR pin equal to or below V_{DD}.
- Do not apply the voltage to the VR pin before V_{DD} is applied.
- Connect AGND to GND.

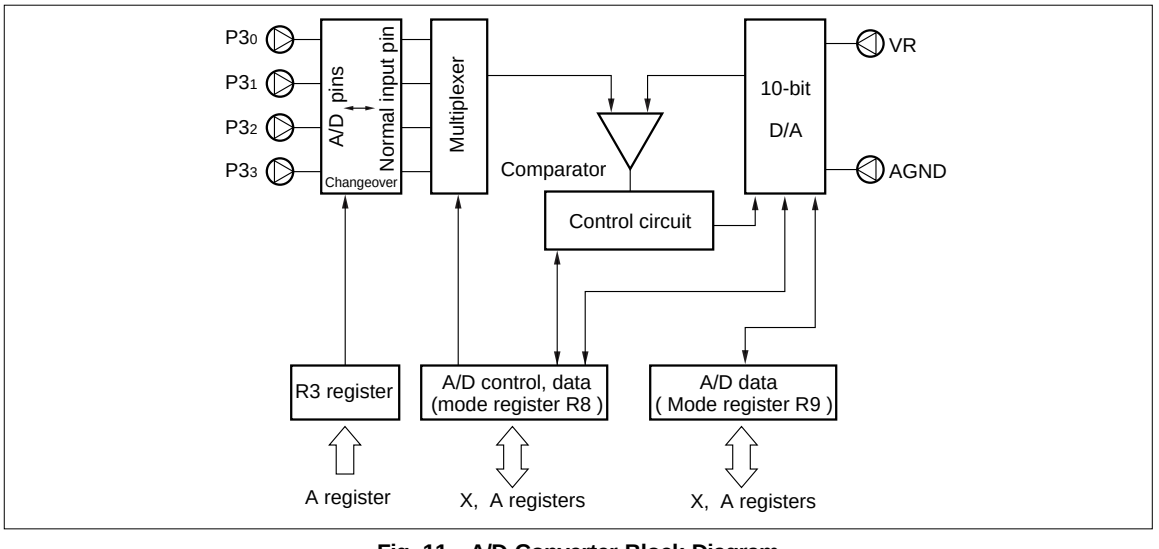


Fig. 11 A/D Converter Block Diagram

A/D CONVERSION MODE

In the A/D conversion mode, the converter converts the analog input voltage to the digital value. The analog input voltage is successively compared with the internal voltage charged on the weighted capacitor array until its digital equivalent is determined. The resultant digital data is stored into the mode registers R8 and R9.

The conversion requires 152.5 µs (main clock at 400 kHz/system clock at 5 µs) or 1.86 ms (main clock at 32.768 kHz/system clock at 61 µs).

COMPARISON MODE

In the comparison mode, the analog voltage from one of $P3_0$ to $P3_3$ pins is compared, in amplitude, with internally generated voltage whose value is set by the mode registers R8 and R9. The result data of the comparison is saved into the bit 4 (bit R84) position of the mode register R8. The comparison cycle lasts 62.5 µs (main clock at 400 kHz, system clock at 5 µs) or 763 µs (main clock at 32.768 kHz/system clock at 61 µs).

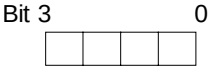
MODE REGISTERS

The registers which control functions of the SM5K3/5K4/5K5 and which serve as counter/timer are commonly referred to as “mode registers”. In the SM5K3/5K4/5K5, R8 to RB are 8-bit mode registers; and R3, RC, RE and RF are 4-bit mode registers.

To set data into the mode registers, the OUT command is used; and to check the contents of the mode registers IN command is used.

R3 (A/D pin selection register)

Any pin on 4-pin port P3 can be set accommodate analog voltage (hereafter called A/D pin).



Bit i (i = 3 to 0)

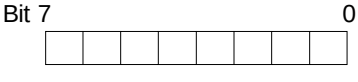
Sets P3i pin to either general purpose input or A/D pin

0	(General purpose) input
1	A/D input

* Select one pin which is to be selected by mode register R8.

R8 (A/D conversion control & A/D data register)

An 8-bit register used to control A/D conversion and storing part of A/D conversion result. It also stores the results of comparison.



Bits 7 to 6

Storage of A/D conversion result (A/D conversion mode) and setting of internal voltage (comparison mode)

- Use as part of a 10-bit data ragister in combination with mode register R9.
- Bit R86 is the LSB.
- Store lower 2-bit of converted data in A/D conversion mode.
- Use as lower 2-bit of internal voltage setting data in comparison mode.

Bit 5

* A/D operation enable/disable flag

0	Disable (A/D power source off)
1	Enable (A/D power source on)

Bit 4

Storages of comparison result (read only)

0	P3i pin voltage < internal setting voltage
1	P3i pin voltage > internal setting voltage

(i = 3 to 0)

Bit 3

* S/R flag (start/clear)

0	End of operation (or stop)
1	Start of operation (or in operation)

Bit 2

Operation mode selection

0	A/D conversion
1	Comparison

Bits 1 to 0

Select one of A/D pins as A/D conversion

00	$P3_0$
01	$P3_1$
10	$P3_2$
11	$P3_3$

* When operation is end, these bits are cleared.

R9 (A/D data register)

The register to store the upper 8-bit of 10-bit data resulting from A/D conversion.

Bit i (i = 7 to 0)

Storages of A/D conversion result (A/D conversion mode) and setting of internal voltage (comparison mode)

- Uses as part of a 10-bit data register in combination with mode register R8.
- Bit R97 is the MSB.
- Stores upper 8-bit of A/D conversion result.
- Uses as upper 8-bit of internal voltage setting data in comparison mode.

RA (Count register)

Bit 7 0

Bit i (i = 7 to 0)

Count clock input register

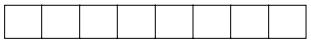
- Uses as counter part of timer/counter (count clock input).
- Loads the content of RB to RA when the RA overflows or when OUT command ($B_L = 0A_H$) is executed.

  RA←RB
- Loads the content of RA to X and A registers upon execution of IN command ($B_L = 0A_H$).

  (X, A)←RA
- Bit 7 = MSB, bit 0 = LSB

RB (Modulo register)

Bit 7 0



Bit i (i = 7 to 0)

Count initial value storage register

- Uses as modulo register of timer/counter
- Loads the content of RB to X and A registers upon execution of

  IN command ($B_L = 0B_H$) : X = upper bits, A = lower bits.

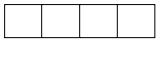
  (X, A)←RB
- Loads the contents of X and A registers to RB upon execution of

  OUT command ($B_L = 0B_H$) : X = upper bits, A = lower bits.

  RB←(X, A)
- Bit 7 : MSB, Bit 0 : LSB

RC (Timer control)

Bit 3 0



Bit 3

Starts up count of the timer.

0	Stop
1	Start

Bit 2 (Unused)

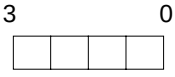
Bits 1 to 0

Select the source clock to the timer.

00	f_{SYS} (system clock)
01	$f_{SYS}/2^7$
10	$f_{SYS}/2^{15}$
11	Falling edge input on $P1_1$ pin

RE (Interrupt mask flag)

Bit 3 0



Bit 3 (Unused)

Bit 2

Removes overflow interrupt from timer or standby condition.

0	Disable
1	Enable

Bit 1

Interrupts on the falling edge of input from $P1_1$ pin, or releases of standby mode by the Low input from $P1_1$ pin.

0	Disable
1	Enable

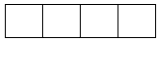
Bit 0

Interrupts on the falling edge of input on $P1_0$ pin, or releases of standby mode by the Low input from $P1_0$ pin.

0	Disable
1	Enable

RF (P2 port direction register)

Bit 3 0



Bit i (i = 3 to 0)

Selection of input pin/output pin

0	Set P2i pin to input.
1	Set P2i pin to output.

I/O Ports

The SM5K3/5K4/5K5 have 24 ports : 8-input, 4-output and 12-I/O port. To verify the input, use suitable instruction to transfer the input on the pin directly to the A register. To select the output latch register to which the content of the A register is to be transferred, and to select the input port from which the signal or data is to be transferred to the A register, use the B_L register. For details of B_L settings and associated ports, refer to Table 1.

• Port $P0_0$ to $P0_3$ (CMOS inverting output port)
The data transfers in 4-bit string (use OUT or OUTL instruction) or in unit of 1-bit (use ANP or ORP instruction).

• Port $P1_0$ to $P1_3$ (input port with pull-up resistor)
The data transfers in unit of 4-bit. This port can be used as standby/external interrupt input or count pulse input. The P1 port can also be used as a standby release port without requiring specific setting on $P1_2$ and $P1_3$ pins. Pins $P1_0$ and $P1_1$ require settings through the mode resister RE. When using the P1 port as an external interrupt input, use pins $P1_0$ and $P1_1$ with suitable settings in the mode register RE. When using the P1 port as the count pulse input, use $P1_1$ pin.

• Port $P2_0$ to $P2_3$ (I/O port with pull-up resistor)
Each bit can be independently be set its direction and can be transferred independently or in combination of other 3-bit. The direction of the bits is determined by the RF register. After reset, the P2 port is set input.

• Port $P3_0$ to $P3_3$ (input port with pull-up resistor)
The data transfers in unit of 4-bit. The port can also be used as A/D analog voltage input. To use the P3 port as the A/D port, set the mode register R3.

• Port $P4_0$ to $P4_3$ (I/O port with pull-up resistor)
The data transfers in unit of 4-bit.
When set output, content of each bit can be set.
Executing the input instruction (IN) sets the P4 ports ($P4_0$ to $P4_3$) to input; and executing output instruction (OUT, ANP or ORP) sets the port to output. After reset, the P4 port is set input.

• Port $P5_0$ to $P5_3$ (I/O port with pull-up resistor)
The data transfers in unit of 4-bit.
When set output, content of each bit can be set.
Executing the input instruction (IN) sets the P5 ports ($P5_0$ to $P5_3$) to input; and executing output instruction (OUT, ANP or ORP) sets the port to output. After reset, the P5 port is set input.

Flags

The SM5K3/5K4/5K5 have 4 flags (C flag and interrupt request flags [IFA, IFB, IFT]), which are used to perform setting and judgments.

System Clock Generator and Dividers

• System clock generator

The system clock is the divided-by-two main clock applied through OSC_{IN} and OSC_{OUT} (See Fig. 12). The system clock generator is shown in Fig. 13.

One system clock cycle period is equal to one instruction execution time when the instruction consists of 1 word. When the ceramic oscillator runs at 400 kHz, the system clock fsys is 200 kHz. This means that the instruction execution time is 5 µs/word. Using a 32.768 kHz crystal oscillator generates 16.384 kHz fsys and the instruction execution time is 61 µs/word. The system clock can be used as count input pulse to the timer.

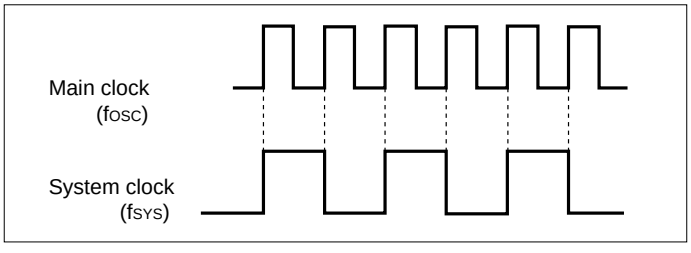


Fig. 12 Main Clock and System Clock

• Divider

The divider consists of 15 divided-by-two dividers, providing 2 ($f_{SYS}/2^7$, $f_{SYS}/2^{15}$) of 4 count clocks that are fed to the counter RA from the system clock. Its configuration is shown below. The divider can be cleared by using the DR instruction.

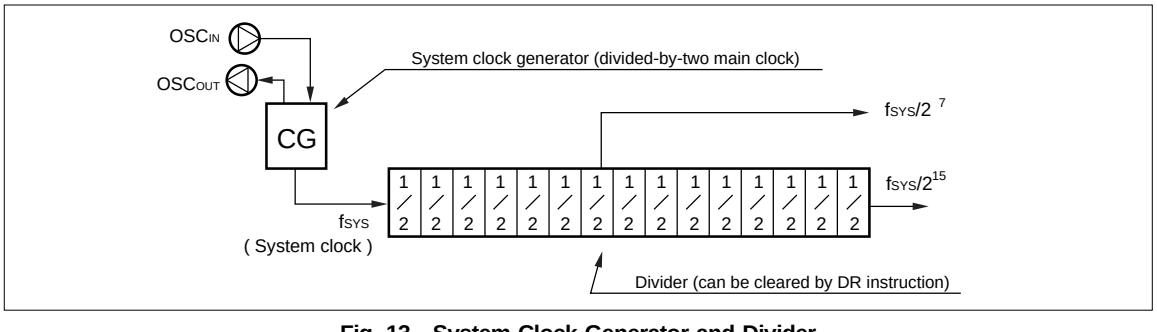


Fig. 13 System Clock Generator and Divider

• Oscillator mask option

Selection of type of oscillator, ceramic or crystal, is made by mask option.

INSTRUCTION SET

Definition of Symbols

M : Content of RAM at the address defined by the B register.

← : Transfer direction

∪ : Logical OR

∩ : Logical AND

⊕ : Exclusive OR

Ai : An i bit of A register (i = 3 to 0)

Push : Saves the contents of PC to stack register SR.

Pop : Returns the contents saved in the stack register back to PC.

Pj : Indicates output latch register or input register. Pj (j = 0, 1, 2, 3, 4, 5)

Rj : Mode register. Rj register (j = 3, A, B, C, E, F)

ROM ( ) : Content stored in ROM location defined by the value in ( ).

CY : Carry in ALU (independent of C flag) The CY(carry) is a signal which is generated when the ALU has been carried by the execution of a command. It is different from the C flag.

X : Used to represent a group of bits in the content of a register or memory. For example, the X in the LDAX instruction denotes the lower 2 digits (I_1 and I_0) of A register.

- A bit in a register is affixed to the register symbol, e.g. a bit (i = 0, 1, 2, 3....) of X register is expressed as Xi and P (R) register as P (R) i.
- Increment means binary addition of 1_H and decrement addition of F_H.
- Skipping an instruction means to ignore that instruction and to do nothing until starting the next instruction. In this sense, an instruction to be skipped is treated as an NOP instruction. Skipping 1-byte instruction requires 1-cycle, and 2-byte instruction 2-cycle. Skipping 1-byte 2-cycle instruction requires 1-cycle.

Instruction Summary

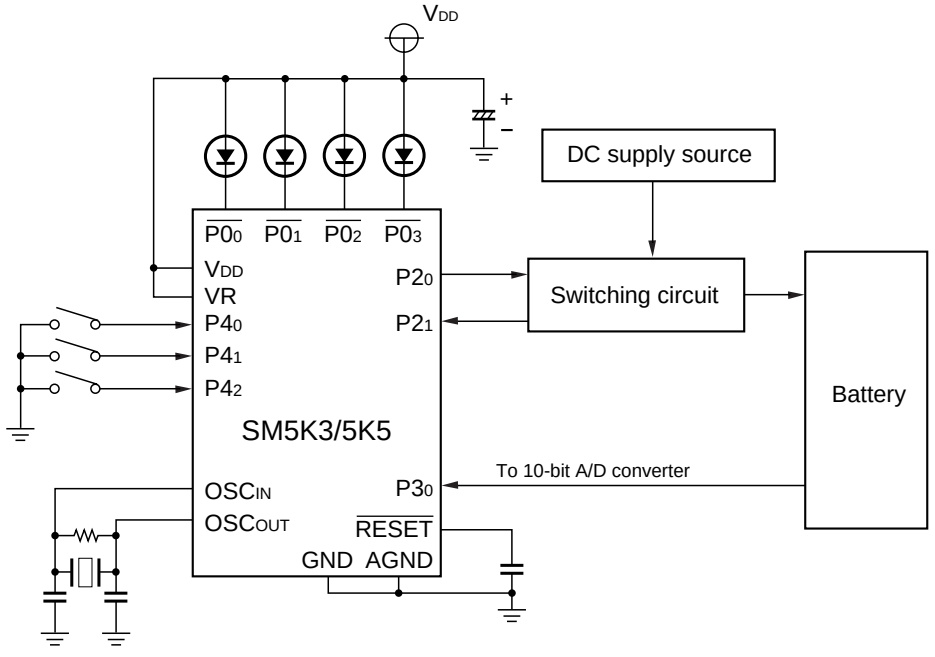
MNEMONIC	MACHINE CODE	OPERATION
ROM Addressing Instructions		
TR x	80 to BF	$P_L \leftarrow x$ (I_5-I_0)
TL xy	E0 to E7, 00 to FF	$P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
TRS x	C0 to DF	Push, $P_U \leftarrow 01_H$, $P_L \leftarrow x$ (I_4, I_3, I_2, I_1, I_0)
CALL xy	F0 to F7 00 to FF	Push, $P_U \leftarrow x$ (I_{11}-I_6) $P_L \leftarrow y$ (I_5-I_0)
RTN	7D	Pop
RTNS	7E	Pop, Skip the next step
RTNI	7F	Pop, IME←1
Data Load Instructions		
LAX x	10 to 1F	A←x (I_3-I_0)
LBMX x	30 to 3F	$B_M \leftarrow x$ (I_3-I_0)
LBLX x	20 to 2F	$B_L \leftarrow x$ (I_3-I_0)
LDA x	50 to 53	A←M, $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0)
EXC x	54 to 57	M↔A, $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0)
EXCI x	58 to 5B	M↔A, $B_L \leftarrow B_L$+1 $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0) Skip the next step, if result of B_L = 0
EXCD x	5C to 5F	M↔A, $B_L \leftarrow B_L$–1 $B_{Mi} \leftarrow B_{Mi} \oplus x$ (I_1, I_0), (i = 1, 0) Skip the next step, if result of B_L is F_H
EXAX	64	A↔X-reg
ATX	65	X-reg←A
EXBM	66	$B_M \leftrightarrow A$
EXBL	67	$B_L \leftrightarrow A$
EX	68	B↔SB

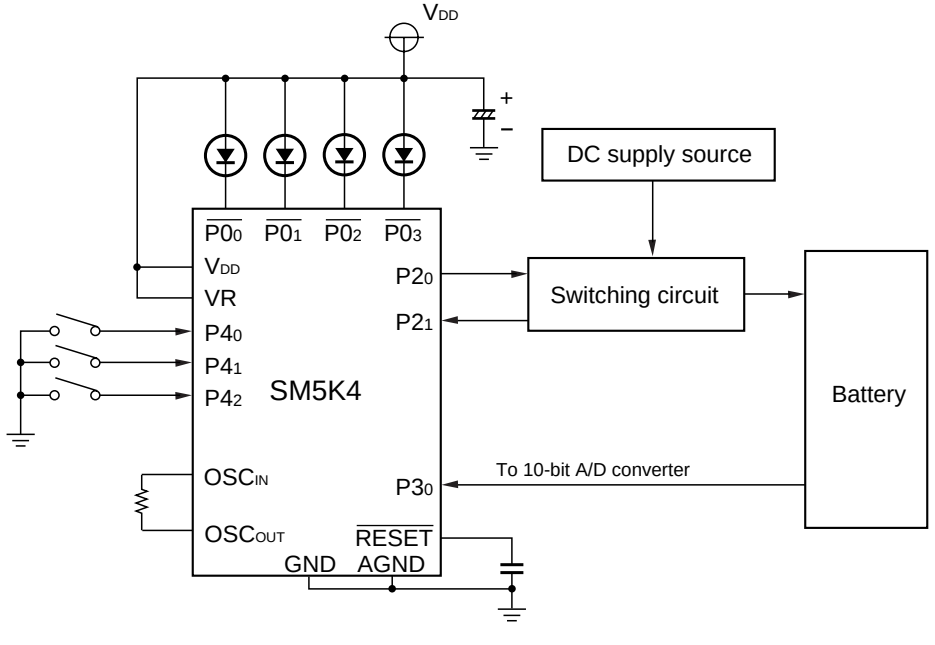
MNEMONIC	MACHINE CODE	OPERATION
Arithmetic Instructions		
ADX x	00 to 0F	A←A+x (I_3-I_0) Skip the next step, if CY = 1
ADD	7A	A←A+M
ADC	7B	A←A+M+C, C←CY Skip the next step, if CY = 1
COMA	79	A←$\overline{A}$
INCB	78	B_L←B_L+1, Skip the next step, if result of B_L = 0
DECB	7C	B_L←B_L–1, Skip the next step, if result of B_L = F_H
Test Instructions		
TAM	6F	Skip the next step, if A = M
TC	6E	Skip the next step, if C = 1
TM x	48 to 4B	Skip the next step, if Mi = 1, (i = 3 to 0)
TABL	6B	Skip the next step, if A = B_L
TPB x	4C to 4F	Skip the next step, if P (R) i = 1, (i = I_1, I_0)
TA	6C	Skip the next step, if IFA = 1 IFA←0
TB	6D	Skip the next step, if IFB = 1 IFB←0
TT	69 02	Skip the next step, if IFT = 1 IFT←0
Bit Operation Instructions		
SM x	44 to 47	Mi←1 (i = 3 to 0)
RM x	40 to 43	Mi←0 (i = 3 to 0)
SC	61	C←1
RC	60	C←0
IE	63	IME←1 (Interrupt enable)
ID	62	IME←0 (Interrupt disable)

MNEMONIC	MACHINE CODE	OPERATION
I/O Instructions		
INL	70	A←P1
OUTL	71	P0←A
ANP	72	Pj←Pj ∩ A (j = 0, 2, 4, 5)
ORP	73	Pj←Pj ∪ A (j = 0, 2, 4, 5)
IN	74	A←Pj (j = 1, 2, 3, 4, 5) X-reg, A←Rj (j = 8, 9, A, B) A←Rj (j = C, E, F)
OUT	75	Pj←A (j = 0, 2, 4, 5) Rj←X-reg, A (j = 8, 9, B) RA←RB Rj←A (j = 3, C, E, F)
Table Search Instruction		
PAT	6A	Push P_U←04_H, P_L←(X_1, X_0, A) X-reg←ROM_H, A←ROM_L Pop
Divider Operation Instruction		
DR	69 03	Divider (f_0-f_{15}) clear
Special Instructions		
STOP	76	Standby mode (STOP)
HALT	77	Standby mode (HALT)
NOP	00	No operation

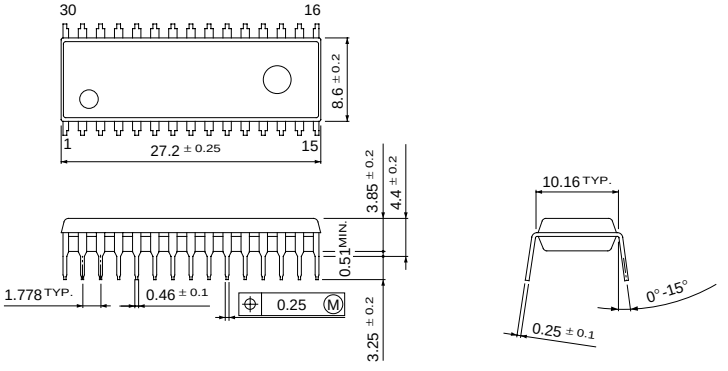
SYSTEM CONFIGURATION EXAMPLE

• Charger controller

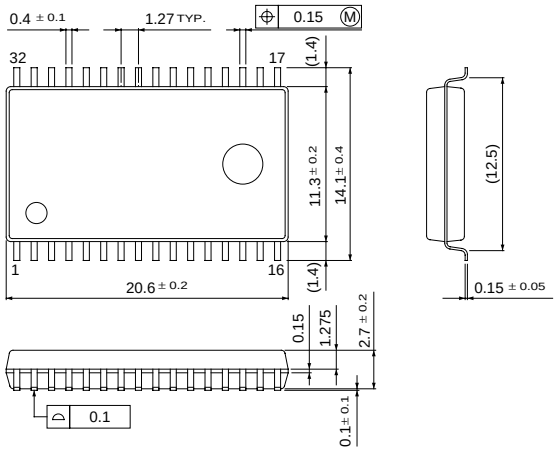




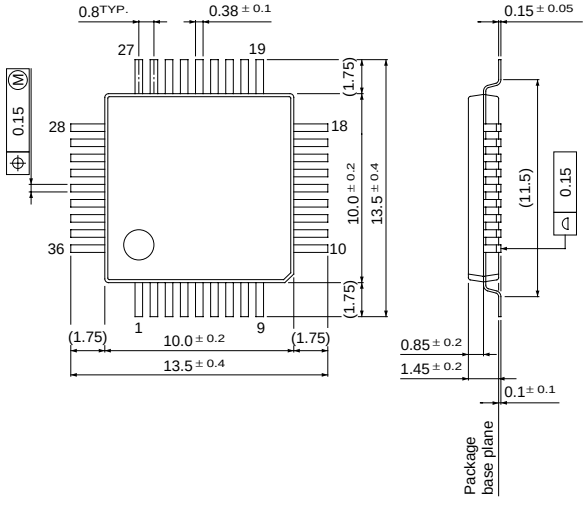
30 SDIP (SDIP030-P-0400)



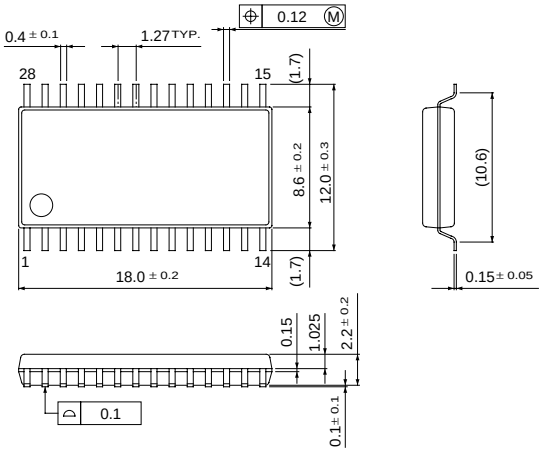
32 SOP (SOP032-P-0525)



36 QFP (QFP036-P-1010)



28 SOP (SOP028-P-0450)



24 SSOP (SSOP024-P-0275)