SN100KT5540 OCTAL ECL-TO-TTL TRANSLATOR WITH 3-STATE OUTPUTS SDZS005 – DECEMBER 1989

- 100K Compatible
- Inverting Outputs
- ECL and TTL Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

description

This octal ECL-to-TTL translator is designed to provide a efficient translation between a 100K ECL signal environment and a TTL signal environment. This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Two output pins, $\overline{OE1}$ and $\overline{OE2}$, are provided. These control inputs are ANDed together with $\overline{OE1}$ being ECL compatible and $\overline{OE2}$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN100KT5540 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE

OUTPUT		DATA	OUTPUT		
ENABLE		INPUT	TTL		
OE1	OE2	Α	Y		
Х	Н	Х	Z		
н	Х	Х	Z		
L	L	L	н		
L	L	Н	L		

(TOP VIEW)							
Y1 [Y2] Y3 [Vcc] G ND [G ND] Y5 [Y6] Y7 [(TOP V) 1 2 3 4 5 6 7 8 9 10 11	24 A1 23 A2 22 A3 21 A4 20 OE2 (TTL) 19 V _{EE} 18 GND 17 OE1 (ECL) 16 A5 15 A6					
Y8	12	14 A7 13 A8					

logic symbol[†]

R NT PACKAGE



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	–0.5 V to 7 V
Supply voltage range, V _{EE}	8 V to 0 V
Input voltage range: TTL (see Note 1)	–1.2 V to 7 V
ECL	V _{EE} to 0 V
Voltage applied to any output in the high state	
Voltage applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Input current range (TTL)	
Current into any output in the low state	
Operating free-air temperature range	0°C to 85°C
Storage temperature range	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.



recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	TTL supply voltage	4.5	5	5.5	V
VEE	ECL supply voltage	-4.2	-4.5	-4.8	V
VIH	TTL high-level input voltage	2			V
VIL	TTL low-level input voltage			0.8	V
VIH	ECL high-level input voltage [†]	-1150		-840	mV
VIL	ECL low-level input voltage [†]	-1810		-1490	mV
IК	TTL input clamp current			-18	mA
ЮН	High-level output current			-15	mA
IOL	Low-level output current			48	mA
TA	Operating free-air temperature	0		85	°C

[†] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
VIK	OE2 only	V _{CC} = 4.5 V,	$V_{EE} = -4.2 V_{,}$	l _l = –18 mA			-1.2	V
		V _{CC} = 4.5 V,	V_{EE} = -4.5 V \pm 0.3 V,	I _{OH} = -3 mA	2.4	3.3		
∨он		V _{CC} = 4.5 V,	$V_{\mbox{\scriptsize EE}}$ = -4.5 V \pm 0.3 V,	I _{OH} = -15 mA	2	3.1		V
VOL		V _{CC} = 4.5 V,	$V_{\mbox{\scriptsize EE}}$ = -4.5 V \pm 0.3 V,	l _{OL} = 48 mA		0.38	0.55	V
Ц	OE2 only	V _{CC} = 5.5 V,	$V_{EE} = -4.8 V_{,}$	VI = 7 V			0.1	mA
ЧΗ	OE2 only	V _{CC} = 5.5 V,	$V_{EE} = -4.8 V_{,}$	VI = 2.7 V			20	μA
١ _{IL}	OE2 only	V _{CC} = 5.5 V,	$V_{EE} = -4.8 V,$	VI = 0.5 V			-0.5	mA
Iн	Data inputs and OE1	V _{CC} = 5.5 V,	$V_{EE} = -4.8 V,$	VIH = -840 mV			350	μA
۱	Data inputs and OE1	V _{CC} = 5.5 V,	$V_{EE} = -4.8 V_{,}$	$V_{IL} = -1810 \text{ mV}$	0.50			μA
IOZH		V _{CC} = 5.5 V,	$V_{EE} = -4.8 V_{,}$	V _O = 2.7 V			50	μΑ
IOZL		V _{CC} = 5.5 V,	V _{EE} = -4.8 V,	V _O = 0.5 V			-50	μA
los§		V _{CC} = 5.5 V,	$V_{EE} = -4.8 V,$	VO = 0 V	-100		-225	mA
ІССН		V _{CC} = 5.5 V,	V _{EE} = -4.8 V			67	97	mA
ICCL		V _{CC} = 5.5 V,	V _{EE} = -4.8 V			84	120	mA
Iccz		V _{CC} = 5.5 V,	V _{EE} = -4.8 V			81	116	mA
IEE		V _{CC} = 5.5 V,	V _{EE} = -4.8 V			-22	-33	mA
Ci		V _{CC} = 5 V,	V _{EE} = 4.5 V			5		pF
Co		V _{CC} = 5 V,	V _{EE} = 4.5 V			7		pF

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -4.5 \text{ V}$, $T_A = 25^{\circ}\text{C}$. § Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω			UNIT
			MIN	TYP†	MAX	
^t PLH			1.6	3.9	6.4	
^t PHL	А	Y	1.6	4.2	6.4	ns
^t PZH			2.4	4.5	6.9	
^t PZL	OE1	Y	3.5	5.9	8.7	ns
^t PHZ		X	2.8	5.2	8.1	
^t PLZ	OE1	Y	2.2	4.6	8	ns
^t PZH	OE2		1.4	3.3	6.1	
^t PZL		Y	2.5	4.7	7.9	ns
^t PHZ	OE2		1.6	4.1	6.5	
^t PLZ		Y	0.7	3.3	6.4	ns

 $\overline{\text{†}}$ All typical values are at V_{CC} = 5 V, V_{EE} = -4.5 V, T_A = 25°C.





- NOTES: A.C_L includes probe and jig capacitance.
 - B. For TTL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
 - C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 0.7 ns, t_f \leq 0.7 ns.
 - D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. The outputs are measured one at a time with one transition per measurement.



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FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS



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