What a Designer Should Know

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Contents

List of Illustrations

List of Illustrations (continued)

List of Tables

Abstract

Information in data sheets, which usually give information on device behavior only under recommended operating conditions, may only partially answer engineering questions that arise during the development of systems using integrated circuits (ICs). However, information is frequently needed regarding the behavior of the device outside the conditions in the data sheet. Such questions might be: “How does a bus driver behave with reduced (or even switched-off) supply voltage?” or “How does the delay time of a gate with a large capacitive load change?” or “What must be considered when using so-called *backdriving*?”.

This report gives information on a number of questions that frequently arise. In addition, it provides examples that explain phenomena that the designer should be aware of when using ICs outside their recommended operating conditions.

1 Introduction

The function and behavior of digital ICs are described fully in data sheets. Most questions regarding the behavior of the device that arise when developing a system can be answered with the information given. However, the devices might be operated under conditions not covered by the data sheet. This report addresses this issue and provides information on the behavior of ICs under such conditions.

Many parameter values in data sheets are not measured when the circuits are tested. The information is based on typical values that have been established experimentally and that are applicable to the majority of devices of the same type or family. In individual cases it might be necessary to interpret data and make measurements to accurately forecast the behavior of the complete system.

2 Behavior With the Supply Voltage Reduced

Although not specifically mentioned in data sheets, additional components, some of them parasitic, influence operational characteristics of ICs. These components can affect the function of a system if the devices are not operated within the recommended operating conditions. For example, large systems often require that parts of the system be shut down while other parts continue to operate. Frequent problems occur at the interfaces between subsystems, which are operated with different supply voltages, or whose supply voltages are switched off. This section describes the behavior of digital circuits operated with low supply voltages.

2.1 Behavior With the Supply Voltage Switched Off

Because many circuits can be used with the various logic families, no general rule applies to the behavior of systems with supply voltages switched off. For this reason, only the most important circuits and their behavior are discussed.

2.1.1 Bipolar Circuits

Figure 1 shows the simplified circuit of a TTL device with diode inputs, such as used with devices in the SN74LS (Low-Power Schottky TTL) logic family. However, the following comments apply to all other bipolar logic families.

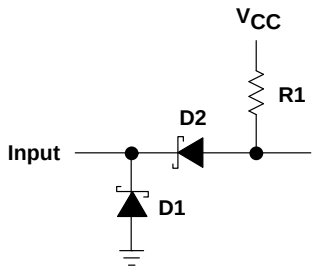

Figure 1. Input Circuit of a Bipolar IC

When the supply voltage in a system is switched off (V_{CC} = 0 V), the V_{CC} pin of an IC is short circuited to ground via the other components in the system. If a voltage is then applied to the input of an IC, as shown in Figure 1, and if this voltage lies within the logic level range (V_I = 0 to 5.5 V), diode D2 is blocking and the clamping diode D1 is biased into a blocking state. Therefore, a very small current flows into the IC, corresponding to the leakage current of these diodes. The value for this current given in the data sheets for the corresponding input voltage can be used. This statement applies, without exception, to all TTL devices.

Figure 2 shows the output stage of circuits from the SN74 (Standard TTL) series. Parasitic collector-substrate diode D2 and diode D3 are in a blocking position between the V_{CC} and GND connections of all ICs. If the V_{CC} pin is at GND potential and a positive voltage is applied to the output, diode D1 is blocking and the output is in the high-impedance state.

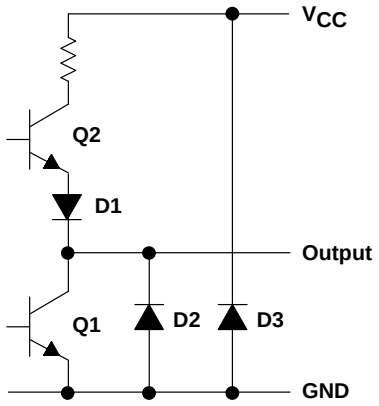

Figure 2. IC Output From SN74 Family (Standard TTL)

Other bias relationships result when supply voltages are switched off to Schottky TTL devices (SN74LS, SN74S, SN74ALS, SN74AS, and SN74F series). Figure 3 shows the important parts of the output stage. If a voltage is applied to the output of the device whose supply voltage is switched off, parasitic diode D1, which is in parallel with resistor R, becomes conducting. The output is then at a low impedance.

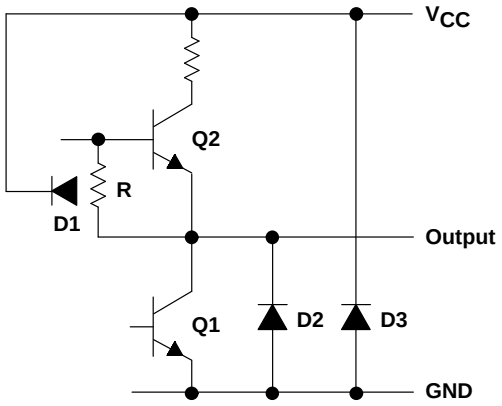

Figure 3. Output of Schottky TTL ICs

If the circuit in Figure 3 is modified for bipolar devices using 3-state outputs, parasitic diode D1 at the output is no longer significant. One possibility is to tie resistor R to GND potential instead of to the output of the circuit (see Figure 4). In this case, the output remains at a high impedance when the supply voltage is switched off.

The outputs of TTL circuits with an open collector are always at a high impedance when the supply voltage is switched off.

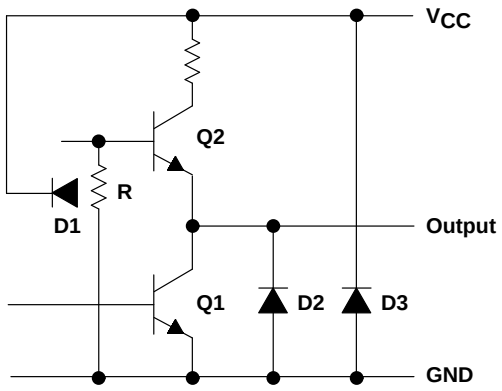

Figure 4. 3-State Output of Schottky TTL Devices

2.1.2 CMOS Circuits

The behavior of CMOS devices when the supply voltage is switched off is essentially determined by the protective circuits at the inputs and outputs. These circuits are intended to protect the device from damage from electrostatic discharge. Figure 5 shows, in simplified form, the construction of a CMOS circuit with additional diode paths at the input and output. Both the input, via diode D1, and the output, via diode D3, are at a low impedance when the supply voltage is switched off. Diode D3 also exists in circuits having an open drain at the output.

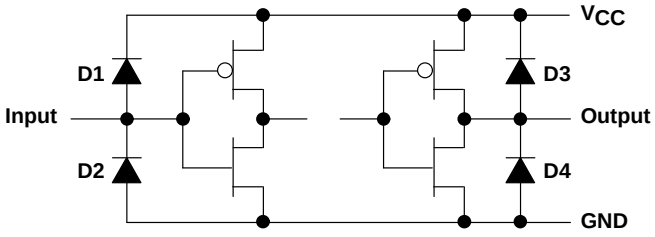

Figure 5. Diode Paths in CMOS Devices

2.2 Behavior With Low Supply Voltages

The behavior of ICs at low supply voltages is difficult to predict because a detailed knowledge of the internal circuit, including its dimensions, is necessary. An example is the behavior of a noninverting buffer with open-collector outputs (SN7407) when the supply voltage is switched on and off. Figure 6 shows the internal circuit of the SN7407. At supply voltages lower than the forward voltage of the diode path (base-emitter path), all transistors are blocking. Therefore, the output voltage (V_O) first follows the supply voltage (V_{CC}). When the latter reaches about 0.7 V, current flows via resistor R3 into the base of transistor Q4 and the output switches to a low level. If the supply voltage reaches a value of $3 \times V_{be}$, and if a logic high is applied to the input, current flows into the base of transistor Q3 (via transistors Q1 and Q2), which switches. Output transistor Q4 is again switched off, causing the output voltage to rise to the value of V_{CC}. In the previous analysis, the voltage drop necessary for a sufficient base current to switch on the transistor is neglected. TTL devices attain stability with a supply voltage of about 3.5 V, and are fully functional at a typical voltage of 4 V. However, with supply voltages below the minimum specified in data sheets, not all parameters can be attained. This applies to both dc parameters, such as output currents and voltages, and to ac parameters, such as propagation delay time and maximum clock frequency.

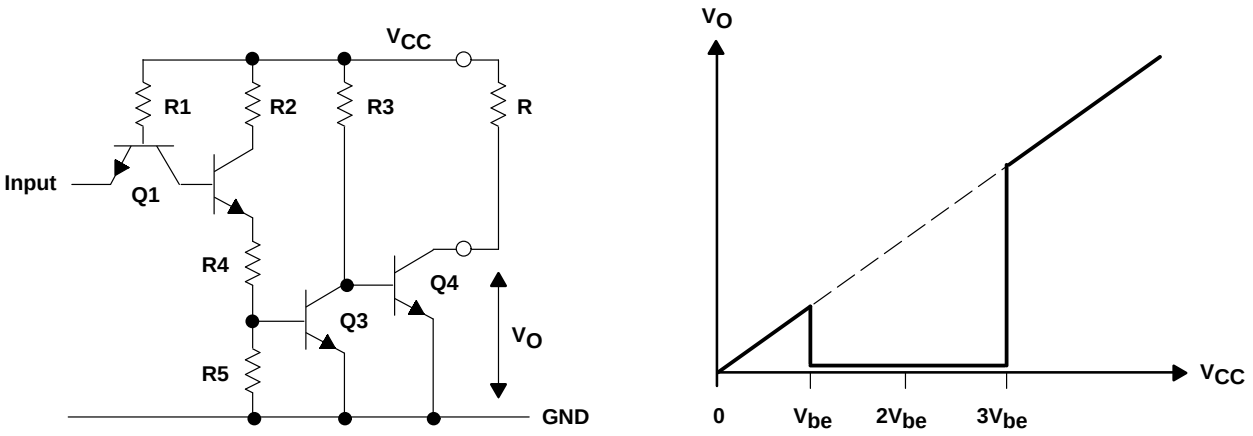

Figure 6. Behavior of a TTL Device at Low Supply Voltages

In a way similar to TTL devices, CMOS devices also fail to operate at supply voltages below the threshold voltages of the MOS transistors. If the supply voltage is further increased, parts of the circuit are activated (see Figure 6). As previously mentioned, the precise circuit configuration of the device determines the circuit behavior. Full functionality of CMOS devices from the SN74HC family is ensured from V_{CC} = 2 V, whereas the 74AC family can only be ensured from 3 V, although the latter is also stable with a supply voltage of only 2 V. Since the maximum clock frequency of CMOS devices is dependent on the supply voltage, at a high clock frequency, circuits might not operate reliably during the switch-on or switch-off phases, even though the supply voltage is more than 2 V.

Special design measures have been taken to achieve a defined behavior, even when circuits are operated at supply voltages far below the conditions recommended in data sheets. For example, on bus drivers of the BiCMOS series (SN74ABT/BCT), a voltage-monitoring circuit ensures that the 3-state outputs remain in the high-impedance state at supply voltages below about 3.5 V, regardless of the inputs to these devices. At supply voltages above this threshold voltage, the control inputs (enable and disable) are effective. If a voltage level is applied to these inputs that results in a high impedance at the output, the same state is implemented at the output.

2.3 Supply Voltages Partially Switched Off

In large systems, often part of the voltage supply is switched off, while other parts of the system continue to operate. Then, the critical part of the system is the interface between the device that is supplied and the device that is not supplied with voltage. In such a case, two requirements must be met. First, the part of the system that continues to operate must not be disturbed by the part that is switched off. Second, the switched-off part must not be disturbed by fed-back voltages from the operating part.

These requirements can be met with bipolar circuits. As mentioned previously, the inputs of switched-off bipolar circuits are at a high impedance and do not influence parts of the device that are still active. With outputs of switched-off parts of devices that are connected to active parts, only the outputs of bus drivers (e.g., SN74xx240 or SN74xx245) are at a high impedance. Therefore, only such devices should be used for bus lines connecting systems. For unidirectional lines that connect switched-off and active devices, it must be determined in each case whether the operation of the system could be influenced by the outputs being at a low impedance when switched off. If this is not the case, then at this position in the system, any kind of device, including CMOS, can be used.

As mentioned previously, when switching the supply on and off, the logic state of the devices concerned cannot be ensured. Therefore, undefined states can arise during this time at the interfaces and cause malfunction of the system (see Figure 6). The use of SN74ABT/BCT-series bus drivers provides a solution, since the outputs of these parts go into the high-impedance inactive state at supply voltages below about 3.5 V. A difficult situation arises when using CMOS devices. As shown in Figure 5, these parts have protection diodes, which are connected to the supply rails, at both inputs and outputs. If the supply voltage V_{CC2} of this circuit is switched off (see Figure 7) while the supply voltage V_{CC1} remains switched on, a current (I) flows out of gate G1, via diode D1, into the next circuit. This current can rapidly overload protective diode D1 (the maximum current of the input clamp diodes of CMOS devices is only 20 mA) and destroy the device. Remember that, in general, the next device represents a short circuit and, apart from the output resistance of gate G1, there is no current-limiting circuit element.

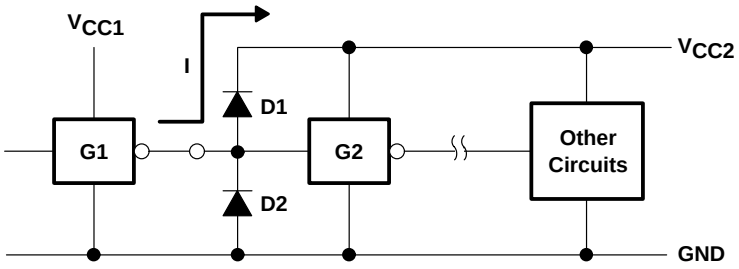

Figure 7. Feeding Back With CMOS Devices

Figure 8 shows recommended design ideas, with reservations, to provide some current limiting. In Figure 8a, the input current of the switched-off device is limited by resistor R. Using this, the input current of the circuit to be protected can be limited to a permissible value. The input current of CMOS devices is extremely low and series resistors of several ohms usually have no negative effect on the function of the part. However, feeding of the next device, via input clamping diode D1, is not prevented entirely.

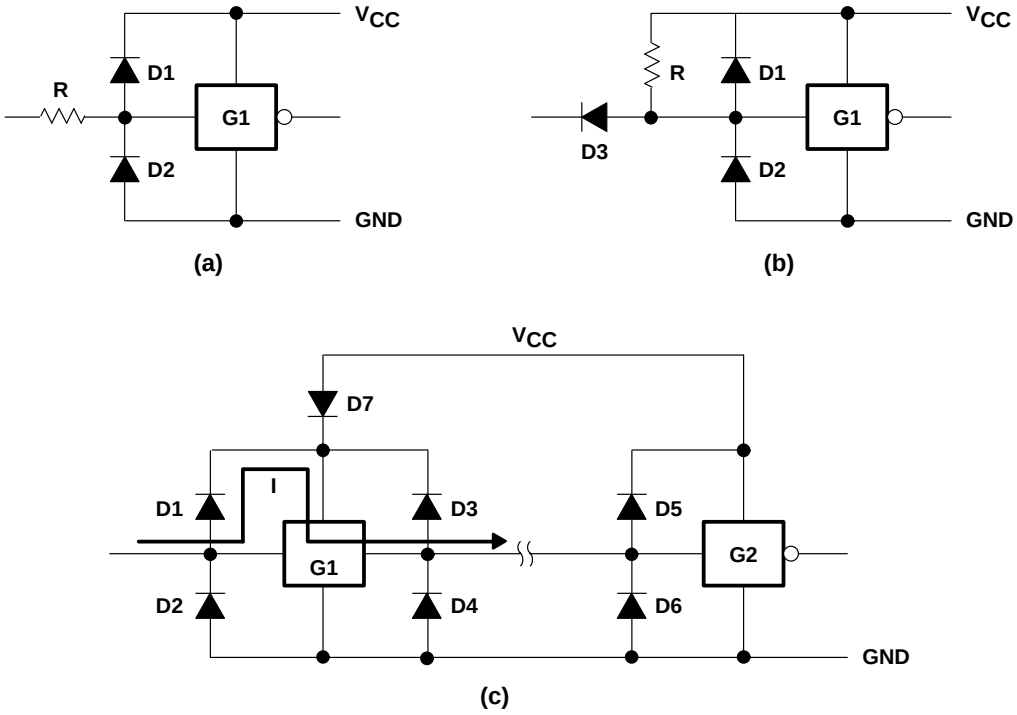

Figure 8. Ideas for Protecting CMOS Devices

In the circuit of Figure 8b, the flow of current into the device to be protected when the supply voltage V_{CC} is switched off, is prevented by diode D3. However, to ensure a high level at the input of gate G1 with normal operation, a pull-up resistor is needed, and this significantly increases the power consumption of the CMOS circuit. D3 also shifts the logic level at the input of the gate, and as a result, reduces the noise margin of the circuit. Apart from the noise-margin restriction, this circuit is effective, because it prevents feedback into the switched-off part of the device.

The diode in Figure 8c has no effect if gate G1 has a noninverting function. Even so, the flow of current via clamping diode D1 and the V_{CC} rail of gate G1 into the next circuit is prevented. Instead, the current flows via the output of gate G1, which, in this case, is at a high logic level, and into the following circuit.

2.4 Changing Powered-Up Subsystems

In many applications, to carry out service or repair work without interrupting operation, it must be possible to change individual subsystems. Because of the partial switch off of supply voltage described previously, this is permissible only when circuit design modifications are made that prevent the destruction of semiconductor components and ensure that the operation of the rest of the system is not disturbed.

In the input and output circuits of ICs, some desired and some parasitic diodes are present. As explained, these components represent additional current paths, and undefined currents may flow into the device, either through the clamping diodes to the inputs and outputs, or through additional parasitic diodes in the ICs. To avoid uncontrolled operational states, changing subsystems while powered up is permissible only if the subsystems have a leading GND pin as a reference potential.

If the connection of the GND reference potential is made first when inserting subsystems and broken only after removing them, the operational state that results when changing subsystems can be limited to the cases previously mentioned. This assumes that parts of the system that have the same reference potential are not supplied with voltage.

The inputs of bipolar logic circuits, including devices in the SN74ABT/BCT series that are in subsystems to be changed, are at a high impedance under all conditions and so no problems need be expected. The totem-pole outputs of most TTL devices are at a low resistance when the supply voltage is switched off, so when reinserting a subsystem, the line concerned is switched to low, which may be incorrect. Three-state outputs of bipolar devices are at a high impedance when the supply voltage is switched off. However, they can go to a low impedance for a short time during switch on or switch off. This could generate an incorrect logic level because at low supply voltages the internal circuit does not operate properly. The result is that during the change of subsystems, short-duration undefined signals that disturb other systems may appear at the corresponding outputs. This problem can be avoided if devices from the SN74ABT/BCT series are used. With these components, the outputs are switched into the inactive high-impedance state if the supply voltage falls below about 3 V.

The problem of changing subsystems with power supplied can be easily solved, particularly when using devices that include a supply-voltage monitor, but CMOS circuits can be used only under these circumstances with certain restrictions. In this case too, the use of a leading GND pin on the connector is essential. The CMOS inputs of devices on the subsystem to be changed should, in every case, be protected at least with series resistors (see Figure 8a), to prevent excessive currents in the clamping diodes of the input protection circuitry. In extreme cases, depending on the layout of pins on the connector, the current for the complete subsystem could, for a short time, flow through one of these diodes. For the outputs of CMOS devices, no practicable protection circuit can be recommended. Also, the use of protection resistors must be considered, to limit the current in the clamping diodes at the output. However, this is not possible in most cases because an unacceptable reduction in the output drive capability would result.

3 Unused Inputs

In many cases, functions or parts of functions of digital ICs are unused. For example, when only two inputs of a triple-input AND gate are used. Such parts should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. A rule that must be observed under all circumstances is:

> At all unused inputs of digital ICs, defined logic levels (low or high) must be applied in every case.

The logic level that should be applied to any particular unused input depends on the function of the device. As a result of the input circuits of bipolar ICs, a high level is established at open-circuited inputs. The voltage at such an input corresponds to the threshold voltage of the input circuit (about 1.4 V or 1.1 V with devices from the SN74LS family). In a test of the function of such a circuit, this order of voltage at the input, in general, indicates that this circuit is open. CMOS inputs are of such high impedance that the smallest change on the open input can generate any undesired logic level. A slight change of the capacitance at the unconnected input, for example, by bringing the hand close to the package, can so change the effective voltage at the input that a high level can change into a low level, or vice versa. Additionally, for the same reasons mentioned, unconnected inputs may react to all kinds of coupled-in interference voltages, and the behavior of the circuit can no longer be predicted.

With gates, the best solution is to connect unused inputs to inputs that are in use. The function of the device is unaffected. This circuit arrangement can be used equally well with AND (NAND) as with OR (NOR) gates (see Figure 9). Here, connecting the inputs together increases the capacitive load on the driver stage and, with bipolar circuits, also increases the dc current drain.

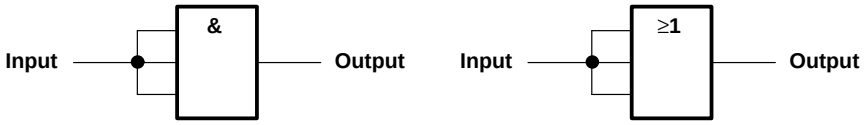

Figure 9. Interconnection of Unused Inputs With AND and OR Gates

In many cases, the simple method shown here cannot be used, especially if the unused inputs are not part of gate functions. In this case, a defined logic level must be applied to the inputs. If a low level is required, the input should be directly connected to GND; if a high level is required, it should be connected with a voltage source corresponding with a high level. In general, this is the positive supply voltage V_{CC}. Figure 10 shows how, in the previously mentioned cases, a fixed potential should be connected to unused inputs. Note that a high level should be applied to the unused inputs of an AND (NAND) function and a low level to unused inputs of an OR (NOR) function.

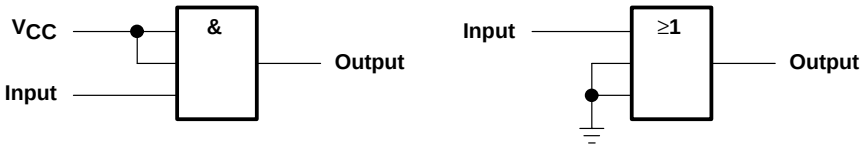

Figure 10. Fixed Potential Connected to Unused Inputs

Devices with multiple-emitter inputs (SN74 and SN74S series) are exceptions to the above. Since no voltage greater than 5.5 V should be applied to the inputs (because if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage V_{CC} via series resistor R_S (see Figure 11). This resistor should be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. But since the high-level input current of the circuits connected to the gate flows through this resistor, the resistor should be dimensioned so that the voltage drop across it still allows the required high level. Equations 1 and 2 are for dimensioning resistor R_S, and several inputs can be connected to a high level via a single resistor, provided the following conditions are met:

$$R_{S(min)} = \frac{V_{CCP} - 5.5\ V}{1\ mA} \quad (1)$$

$$R_{S(max)} = \frac{V_{CC(min)} - 2.4\ V}{n \times I_{IH}} \quad (2)$$

Where:

n	=	number of inputs connected
I_{IH}	=	high input current (typical 40 μA)
$V_{CC(min)}$	=	minimum supply voltage V_{CC}
V_{CCP}	=	maximum peak voltage of the supply voltage V_{CC} (about 7 V)

If whole parts of an IC are unused, the unused-input rules should be applied. If, for example, in an application only one flip-flop from a dual flip-flop type SN74ALS74 is used, all inputs of the unused flip-flop should be connected to a defined logic level, which, in this case, could be either low or high.

NOTE:
Unused outputs of a device should not be left unconnected.

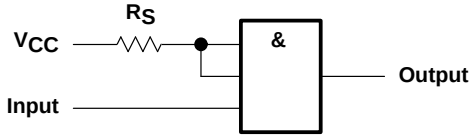

Figure 11. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors

4 Excessive Input Currents

All ICs have protection circuits at outside connections. These diodes, or similar components, are intended to protect the device against destruction by electrostatic discharge. In addition, clamping diodes at IC inputs limit overvoltage and undervoltage resulting from line reflections and divert the currents that flow, in consequence, to either the negative (GND) or positive (V_{CC}) supply rails. Currents that flow in these circuit parts can, under certain circumstances, activate so-called parasitic transistors, which results in incorrect operation of the circuit.

Examples of this are the clamping diodes at the inputs of HCMOS devices, which are intended to limit overvoltages resulting from reflections. These diodes are created with a P-doped region in an N-doped substrate which, in turn, is connected to the positive supply voltage (see Figure 12). Between two adjacent diodes and in conjunction with the substrate, a parasitic PNP transistor is effectively created. A part of the current in one of the two clamping diodes is, therefore, not diverted to the V_{CC} rail but, instead, flows to an adjacent input. The current gain of this transistor is small (about 0.01), so that under normal operating conditions no effect can be expected. If, however, a high positive voltage is applied to the input of a circuit, as in Figure 12, which adapts signal voltages with an amplitude of 24 V to HCMOS circuits, a current flows into the adjacent input, despite the low current gain of the parasitic transistors. The current in the adjacent input may then be sufficient to generate a false input signal. However, destruction or damage to the IC (as a result of latch-up) is not likely to occur.

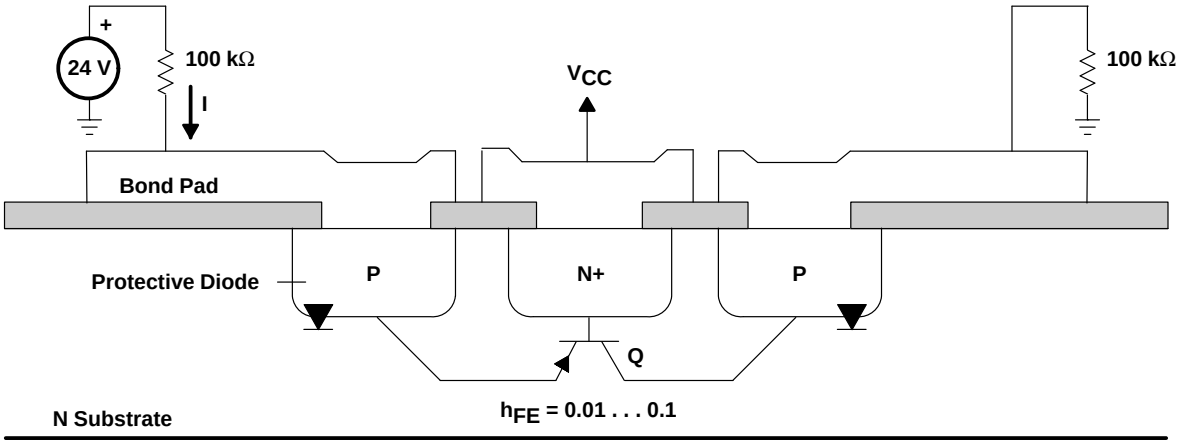

Figure 12. Parasitic Transistors in CMOS Input Stages

Similar effects caused by parasitic transistors can also be observed with bipolar transistors. Figure 13 shows a bipolar input that includes Schottky clamping diodes, realized with an N-doped region covered by a metallic contact. With a small negative input current, the forward voltage of the Schottky diode is about 400 mV, and the current in such an input is diverted, via the diode, to the GND pin of the device. If this current is increased, the forward voltage of the diode increases accordingly, and at a certain amplitude exceeds 700 mV. At this point, the silicon diode (which results from the N-doped region and the P-doped substrate under it, connected to the GND of the device) conducts. Here, also, a parasitic transistor is activated, whereby the whole adjacent N-doped region, comprising the collectors of active transistors, functions as a collector. This collects together a part of the current circulating in the substrate. If the amplitude of the negative current is sufficient, incorrect operation of the circuit can be expected.

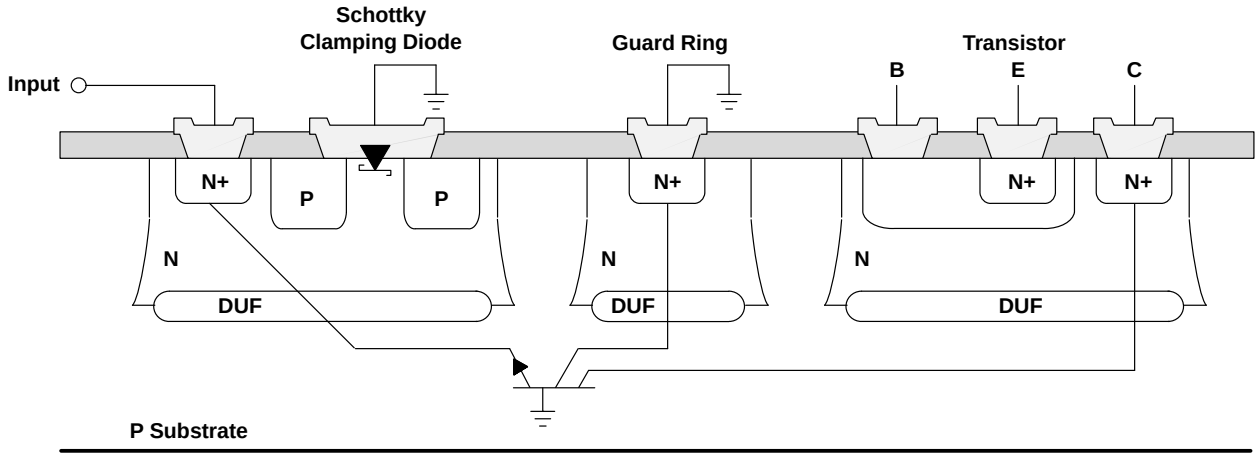

Figure 13. Parasitic Transistors in Bipolar Input Circuits

Negative voltage undershoot of considerable amplitude must be expected in practical operation of logic devices. Therefore, the semiconductor manufacturer must take the steps necessary to ensure reliable operation. Guard rings, which are placed in a ring around the circuit in question (see Figure 13), ensure reliable operation. In this example, these guard rings consist of an N-doped region connected to GND potential, which has the effect of an additional collector for the parasitic transistors, collecting the majority of the current circulating in the substrate and diverting it to GND potential. These guard rings are constructed so that a negative input current of I_{IN} = –60 mA with a duration t = 100 ns does not cause an incorrect function of the circuit. These values are again reflected in Figure 14. Here, a TTL device with a signal amplitude of 3 V drives a 10-meter-long coaxial cable with a characteristic impedance of Z = 50 Ω, at the end of which the input circuitry (with clamping diode) of the device in question is connected. High-amplitude current pulses, such as those generated by line reflection, are captured with this measuring setup.

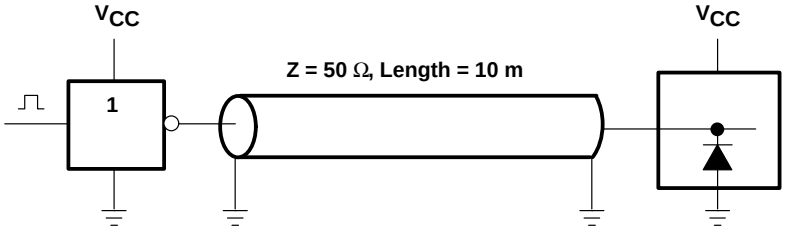

Figure 14. Setup for Generating an Undershoot Pulse (I = –60 mA, t = 100 ns)

Negative input currents with an amplitude of only a few milliamperes, but with a duration of several microseconds, can cause incorrect operation of the device. Since the transit frequency of the parasitic transistors is only about 1 MHz, the circuit and dimensioning of guard rings are simplified. A certain duration of the undershoot pulse is necessary to switch on the parasitic transistors, and possibly to cause abnormal operation of the circuit.

5 Transition Times

Correct operation of the circuit can be ensured only if the rise and fall times of the signal at the input do not exceed certain values. With CMOS devices (SN74HC and 74AC/SN74AC), these values are given in the data sheets. For devices from the SN74HC series, a rise and fall time (transition time) less than 500 ns is specified at V_{CC} = 4.5 V, while for ACL devices (74AC/SN74AC series), a value of 10 ns/V is given. Figure 15 shows this in more detail.

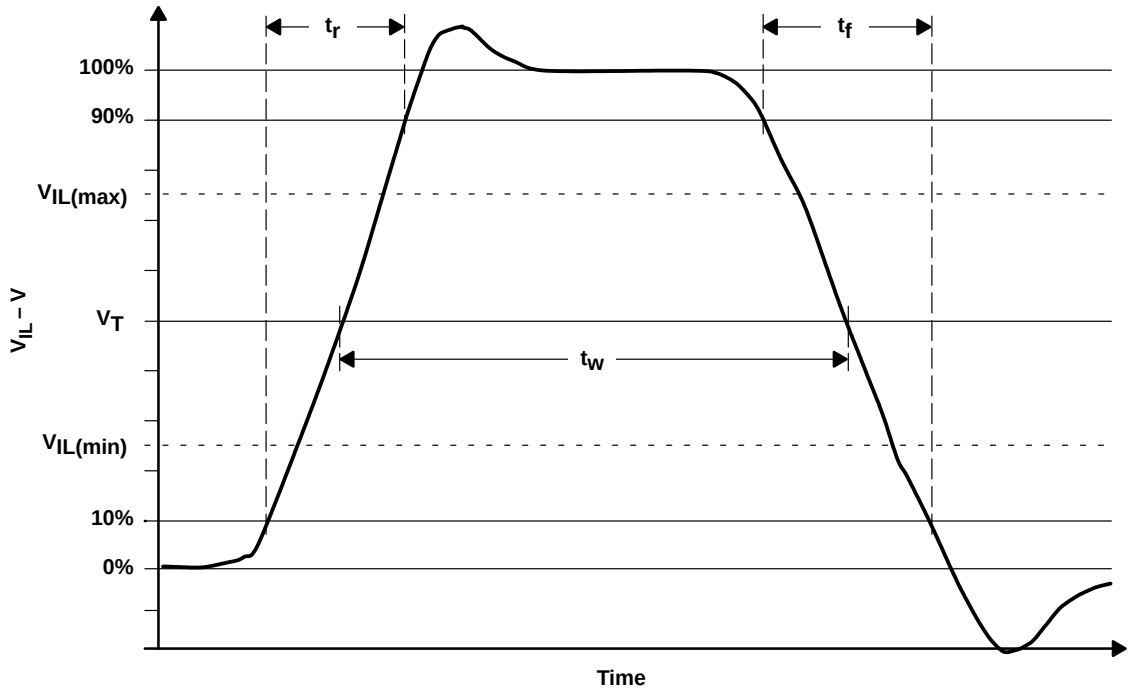

Figure 15. Definition of Signal Amplitude and Pulse Width

The signal amplitude is specified as the difference between the two stable signal levels for high (V_H) and low (V_L); overshoot and undershoot of the signal are not taken into account. The difference $V_H - V_L$ is taken as 100% of the amplitude. The rise time of the signal is defined as the time taken to rise from 10% to 90% of the full amplitude; similarly, the fall time is the time taken to fall from 90% to 10% of the amplitude. The pulse width (t_w) of a signal is measured at 50% of the amplitude. However, these definitions must be used for digital circuits with certain qualifications because, in most cases, the switching threshold (V_T) of the input is not 50% of the amplitude. So, the level needed by the circuit must be considered and, from this, the required signal waveform derived.

The values of voltage that are decisive for the correct operation of the part are the maximum permissible low voltage at the input $V_{IL(max)}$ and the minimum necessary high voltage at the input $V_{IH(min)}$. The following example applies for a device from the SN74HC series:

$V_{IL(max)} = 0.9$ V

$V_{IH(min)} = 3.15$ V at $V_{CC} = 4.5$ V

However, the rise and fall times are specified between 10% ($0.1 \times V_{CC} = 0.45$ V) and 90% ($0.9 \times V_{CC} = 4.05$ V) of the amplitude. The voltage waveform below 0.9 V (low level) and above 3.15 V (high level) has no influence on the function of the device, as long as the absolute maximum ratings are not exceeded. Therefore, it is better to define rise and fall times over the range between $V_{IL(max)}$ and $V_{IH(min)}$, which must be adhered to in order to ensure correct functioning of the device. From the amplitude (4.5 V) and the rise time specified in the data sheet (t_r = 400 ns), the transition time (dt/dv) rate can be derived as follows:

$$dv/dt = \frac{400\ ns}{(0.9 \times V_{CC}) - (0.1 \times V_{CC})} = \frac{400\ ns}{3.6\ V} = 110\ ns/V \quad (3)$$

The input signal must cross the region between $V_{IL(max)}$ and $V_{IH(min)}$ (and vice versa) at the transition rate or faster. This value is comparable to the transition rate given in 74AC-series data sheets of dt/dv = 10 ns/V. The pulse width (t_w) is measured at the actual threshold voltage (V_T) of the circuit and with CMOS devices at 50% of the amplitude. Bipolar and TTL-compatible CMOS devices have a switching threshold that is shifted considerably from the middle of the signal amplitude. This shift must then be taken into account when determining the pulse width. Table 1 shows the necessary minimum transition rise/fall rates for various logic families.

Table 1. Transition Rise/Fall Rates of Logic Circuits

SERIES	V_{CC} (V)	$V_{IL(max)}$ (V)	$V_{IH(min)}$ (V)	V_T (V)	dt/dv (ns/V)
SN74	4.75–5.25	0.8	2	1.4	100
SN74LS	4.75–5.25	0.8	2	1.4	50
SN74S	4.75–5.25	0.8	2	1.4	50
SN74ALS	4.5–5.5	0.8	2	1.4	15
SN74AS	4.5–5.5	0.8	2	1.4	8
SN74F	4.5–5.5	0.8	2	1.4	8
SN74HC	2	0.3	1.5	1.4	625
	4.6	0.9	3.15	2.25	110
	6	1.2	4.2	3	80
SN74HCT	4.5–5.5	0.8	2	1.4	125
74AC	3	0.9	2.1	1.5	10
	4.5	1.35	3.15	2.25	10
	5.5	1.65	3.85	2.75	10
74ACT	4.5–5.5	0.8	2	1.4	10
SN74BCT	4.5–5.5	0.8	2	1.4	10
SN74ABT	4.5–5.5	0.8	2	1.4	5/10
SN74LV	2.7–3.6	0.8	2	≈1.5	100
SN74LVC	2.7–3.6	0.8	2	≈1.5	5/10
SN74LVT	3.0–3.6	0.8	2	1.4	10

The values for the transition rise/fall rates (dt/dv) are understood to be a level that ensures the function of individual components if the circuit is controlled with these rates. This does not necessarily mean that the device operates correctly under all circumstances in a large system. Figure 16 shows this in more detail. It shows two D-type flip-flops connected as a two-stage shift register. The first flip-flop is the TTL-compatible device 74ACT11074 (input threshold voltage = 1.5 V), but the second flip-flop (74AC11074) has CMOS-compatible inputs with an input threshold voltage of $0.5 \times V_{CC}$.

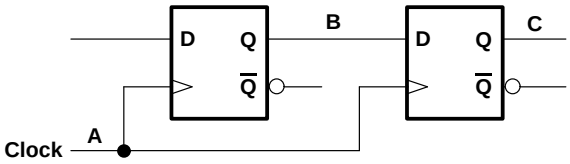

Figure 16. Two-Stage Shift Register

According to Table 1, devices from the 74ACT series must be controlled with a transition rate of at least 10 ns/V, if the function of individual parts is to be ensured. If, however, the behavior with time of the circuit is analyzed, it is found that the shift register does not behave as required (see Figure 17). When the clock signal reaches 1.5 V (having the required transition rate of 10 ns/V), the first flip-flop switches. The output typically reacts about 5 ns later. Only after another 5 ns does the voltage of the clock signal reach a value of 2.5 V, so that the second flip-flop switches. As a result of this late triggering, it accepts incorrect information: namely, the state that the first flip-flop has reached after the switching clock edge, and not the state that the flip-flop had before the clock edge.

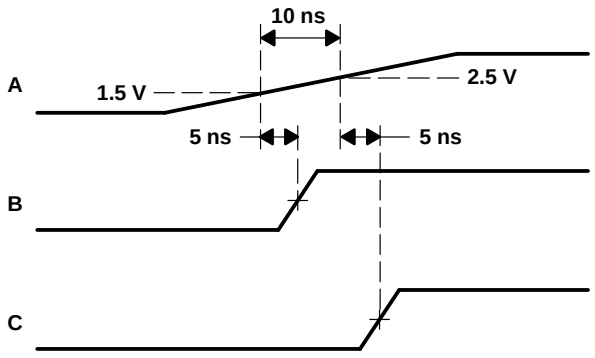

Figure 17. Incorrect Operation of a Shift Register

Under typical operating conditions, the circuitry would, however, operate correctly. The output signals of advanced CMOS devices have a rise time <5 ns (typical 2 ns). At the clock signal, a voltage change of 1.5 V to 2.5 V takes place in about 1.25 ns. A 74ACT11074 flip-flop has a minimum delay time of 1.5 ns, and under these circumstances correct functioning of the circuit is ensured.

Similarly, problems need not be expected when using devices from other families under similar conditions, as long as the signals have nominal rise and fall times. Under extreme conditions (for example, with unfavorable line routing), the switching times can be so lengthened that faults of the kind just described may occur.

6 Propagation Delay Times

6.1 Propagation Delay Times With Several Outputs Switching Simultaneously

The propagation delay times of circuits given in data sheets apply when only one output switches at a time. The reason for this is that the production equipment used to test circuits can test only one transmission channel at a time. If several outputs switch simultaneously, the propagation delay times given in data sheets can only be used with reservations. The reason for this is that the package inductances (L_P) of the supply-voltage lines, as well the output lines (see Figure 18), have a significant influence on the circuits and, thus, on the delay times. These inductances have the effect that the current in the power supply lines, and consequently in the output of the device, has a limited rate of rise. For this reason, when several outputs switch simultaneously, only a limited output current is available.

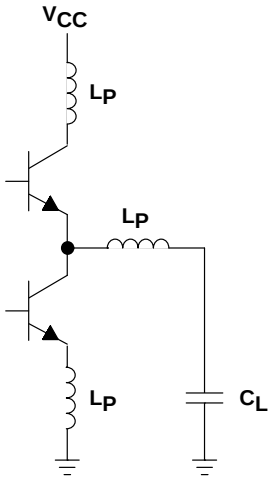

Figure 18. Inductances in the Lines Supplying a Package

Figure 19 shows the influence on the delay time of the number of outputs that are switched simultaneously. When packages having two supply-voltage pins (V_{CC} and GND) are used, as is the case with the majority of digital ICs, an increase of the delay time of 150 ps to 200 ps for each additional output that is simultaneously switched must be expected. With an octal bus driver, such as a SN74xx240, the delay time is increased by 1 ns to 1.4 ns when all eight outputs switch simultaneously. In those cases where there are several supply-voltage pins, such as the advanced CMOS devices in the 74ACT series from Texas Instruments (TI), the result influences speed of the circuit. As shown in Figure 19, the loss of speed of the components is halved when several outputs switch simultaneously.

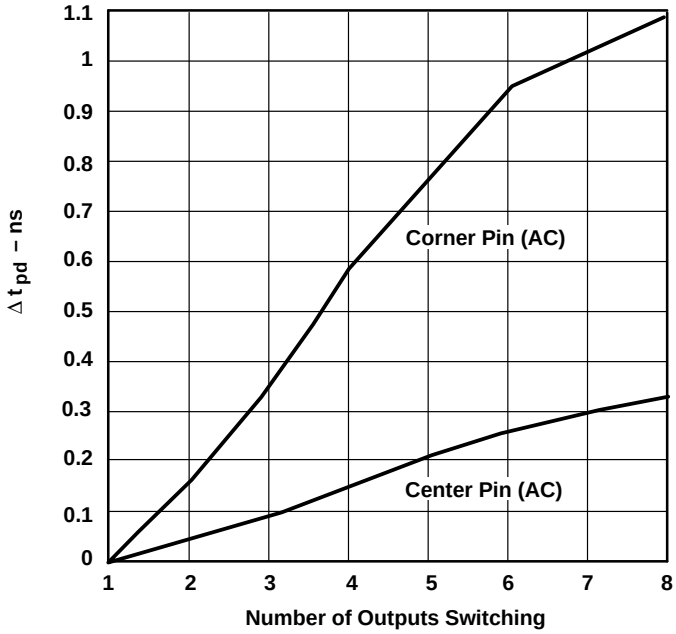

Figure 19. Increase of the Delay Time When Several Outputs Are Switched Simultaneously

With bus drivers and also VLSI circuits that have more than eight outputs that switch simultaneously, an appropriate number of additional supply-voltage pins are provided. A good example is given by the Widebus™ circuits from TI, which are bus drivers with 16, 18, or 20 outputs. To keep the loss of speed (because of so many outputs) within limits, about 25% of all pins of these devices are reserved for the provision of supply voltage. Figure 20 shows the increase of the delay time of a 74AC16240 as a function of the number of outputs that are switched simultaneously.

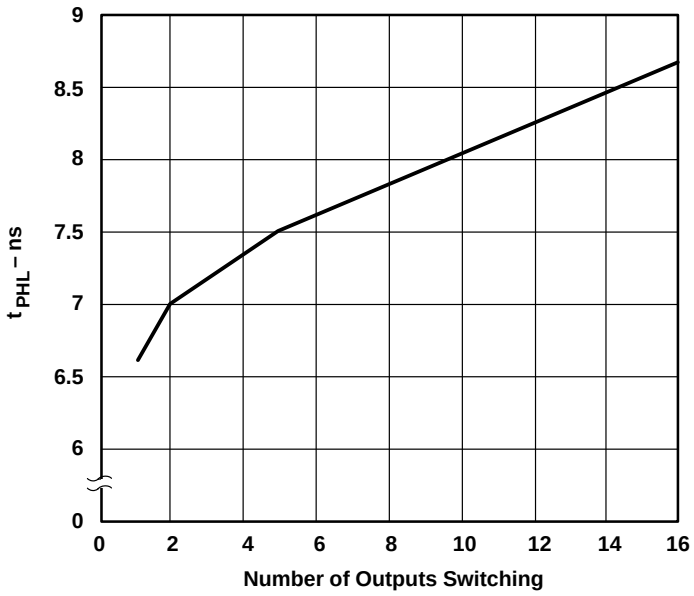

Figure 20. Increase of the Propagation Delay Time With a Widebus™ Circuit (74AC16240)

6.2 Propagation Delay Times With Negative Undershooting at the Outputs

With bipolar circuits, negative voltages caused by undershooting can influence the function of the device. Figure 21 shows this effect. This circuit represents the output stage of a bus driver, which should be in an inactive and high-impedance state. Active bus driver U1 switches the line between the two devices from a high to a low level. As a result of an inadequate termination of the line, there is a negative undershoot on the line, which causes a current (I_X) to flow in the internal circuit of the output stage. This current flows via the collector-base diode of transistor Q5 and Schottky diode D1, in parallel with it and via transistor Q1 to the base node of transistor Q2. Now this node is clamped to a low level. If this output stage should again be switched to the active state (output enable switches from low to high), the output does not follow until the capacitance of the bus line is charged through resistor R to the extent that the collector base diode of transistor Q5 is turned off again, which takes, typically, 5 ns to 10 ns. Apparently, the delay time to again switch on the output stage is increased by about this amount of time.

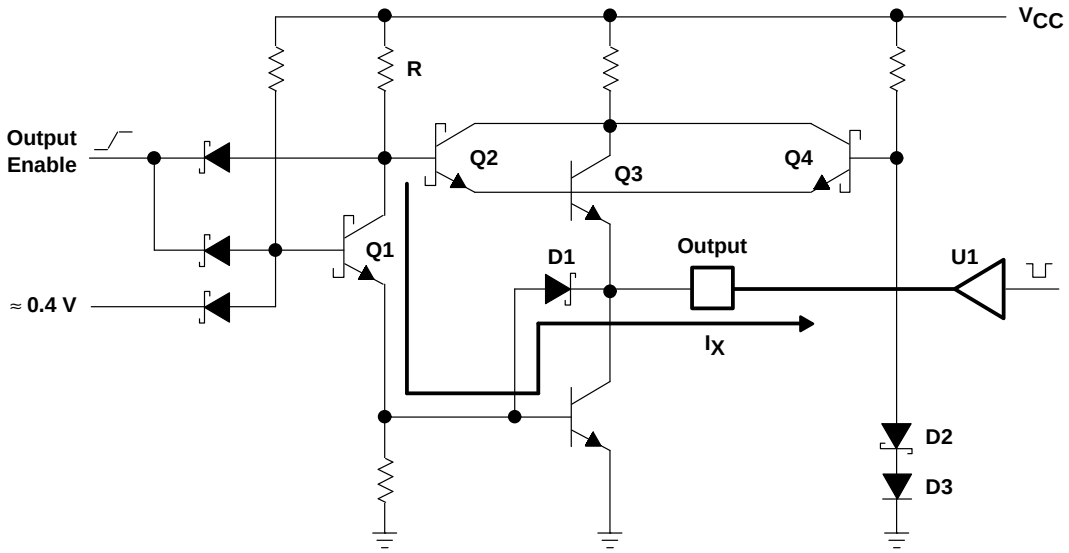

Figure 21. Currents in the Output Stage of a Bus Driver With Negative Undershoot

To prevent this delay, a clamping circuit (D2, D3, and Q4 in Figure 21) is integrated into modern bus drivers. This ensures that, should the output voltage go below –0.3 V, transistor Q3 switches on the output stage and the current I_X is diverted to the positive supply-voltage rail V_{CC}. With ABT devices, clamping is unnecessary and a different circuit that can be more effective is used.

6.3 Propagation Delay Times With Large Capacitive Loads

In digital IC data sheets, propagation delay times are specified with a capacitive load of 50 pF (15 pF on older logic families). This value represents the capacitive load of the test circuit on the output of the IC being tested. This value is also the capacitive load when the output drives five inputs of other circuits and this assumes that the length of the connecting lines is only a few centimeters, as is typically the case on printed circuit boards (PCBs). With such short lines, the first assumption is that the line itself behaves like a capacitor, which additionally loads the output and influences the propagation delay time accordingly. However, with long lines, this assumption leads to errors, because the signal delay is actually determined by the propagation speed of the electrical wavefront along the line. In fact, the propagation delay time of the IC is determined by the loading of the output, that is, by the characteristic impedance of the line to which it is connected, not by its length or capacitance. When driving a line terminated at its end with a resistance of 100 Ω, and lengths of 0 (resistor connected directly to the output), 1 m, and 11 m (see Figure 22), an SN74LS00 device has the output waveforms shown in Figure 23. The three resulting output signals are shown staggered, and are practically identical, i.e., the propagation delay time of the IC is not influenced. The length of the line and the resulting signal propagation time (5 ns/m) influence the delay time of the system. The propagation time of the wave along a 11-m transmission line is 55 ns. Add the propagation delay time of the SN74LS00 of about 10 ns for a total delay of 65 ns.

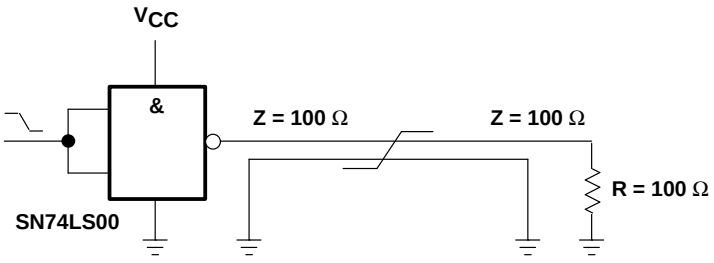

Figure 22. Measurement Setup

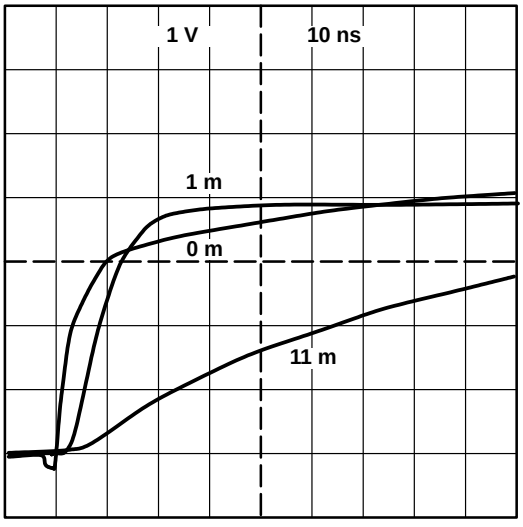

Figure 23. Waveforms for Various Line Lengths

If the capacitive load connected to the output of a device is represented as a single capacitor, the resulting propagation delay time can be calculated. A purely capacitive load can be assumed if the output of the IC controls a MOS power transistor with a relatively large input capacitance. To a first approximation, this assumption is correct if an output drives adjacent inputs over a line length of only a few centimeters. The propagation delay times given in data sheets consider the following:

- Propagation delay time through the internal circuitry of the IC
- Delay resulting from the switching time of the output stage
- Time needed to charge and discharge the capacitance of the load (typically 50 pF)

The first two considerations are independent of the load that is connected. The last consideration must account for the actual load, of which a load capacitance of C1 = 50 pF (15 pF) is already given in data sheets. The time taken to charge the additional capacitance is determined by the current that the device is able to deliver. For the high level, this value can be deduced indirectly from the data sheet. Figure 24 shows the relevant part of the circuit of a bipolar output stage and the resulting output characteristics.

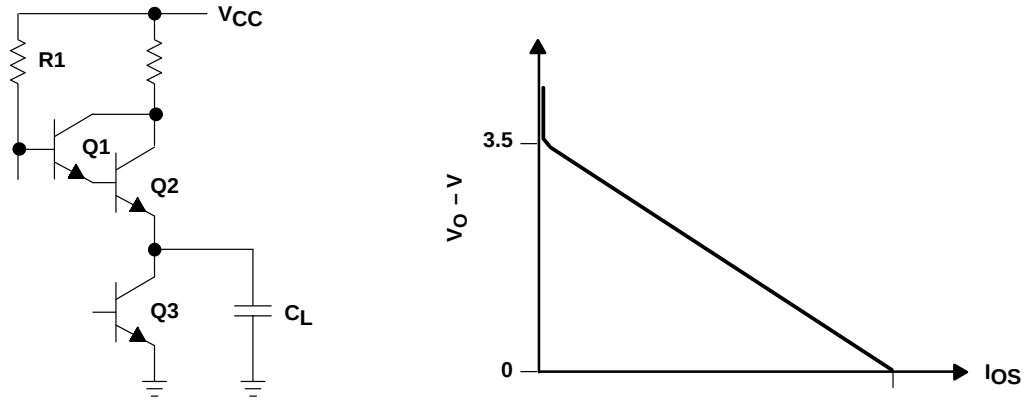

Figure 24. Bipolar Output Stage With Output Characteristics at a High Level

The short-circuit current of the output, when at a high level, is determined by the resistance (R1) and the saturation voltage of Darlington transistors Q1 and Q2 with collector-path resistance. Using the following equation, the internal resistance (R_O) of a circuit can be determined from the open-circuit output voltage (typically 3.5 V) and from the short-circuit current (I_{OS}) given in the data sheet:

$$R_O = \frac{3.5\ V}{I_{OS}} \quad (4)$$

With circuits that use MOS transistors in their output stages (SN74HC and 74AC/SN74AC), the output current is determined by the size of the transistors and the potential difference between gate and source. Since there is no linear relationship between this voltage and the output current, only an approximate indication of the output resistance can be made.

Table 2 shows I_{OS} and R_O for the most important device types.

Table 2. Short-Circuit Current and Internal Resistance of Logic Families

TYPE	SHORT-CIRCUIT CURRENT I_{OS} (mA)	INTERNAL RESISTANCE R_O (Ω)
SN7400	35	50
SN7440	45	75
SN74LS00	35	100
SN74LS40	65	53
SN74LS240	70	50
SN74S00	65	53
SN74S40	140	25
SN74S240	60	58
SN74ALS00	50	70
SN74ALS40	60	58
SN74ALS240	100	35
SN74ALS1000	120	29
SN74AS00	100	35
SN74AS240	140	24
SN74AS1000	160	21
SN74F00	85	41
SN74F40	140	25
SN74F240	140	25
SN74BCT240	140	25
SN74BCT25240	700	5
SN74ABT240	120	29
SN74HCT00	60	40–120
SN74HCT240	80	30–100
74ACT11000	220	4–25
74ACT11240	220	4–25
SN74LV00	35	35–100
SN74LV240	55	25–80
SN74LVC00	85	16–40
SN74LVC240	85	16–40
SN74LVT240	400	8

The typical output voltage of a bipolar device at a low level is about V_{OL} = 0.3 V. The increase of the delay time resulting from the capacitive load (C_L) is determined by the time until the external load capacitance has been charged by an external voltage source from V_{OL} to the threshold voltage of the circuit, typically V_S = 1.5 V. The external voltage source is described by an internal voltage (V_{OH}) and an internal resistance (R_O). In this way, the delay time (t_p) resulting from the load capacitance can be calculated from the following equation:

$$t_p = \ln\frac{V_{OH} - V_{OL}}{V_{OH} - V_S} \times R_O \times C_L = \ln\frac{5.5\ V - 0.3\ V}{3.5\ V - 1.5\ V} \times R_O \times C_L = 0.5 \times R_O \times C_L \quad \textbf{(5)}$$

Figure 25 shows the waveform of the positive edge at the output of a gate (SN74LS00) with various values of capacitive loads (C_L = 10 pF, 56 pF, and 616 pF). As expected, the rise time at the output and the resulting increase of the propagation delay time are determined by the time constant $R_O \times C_L$.

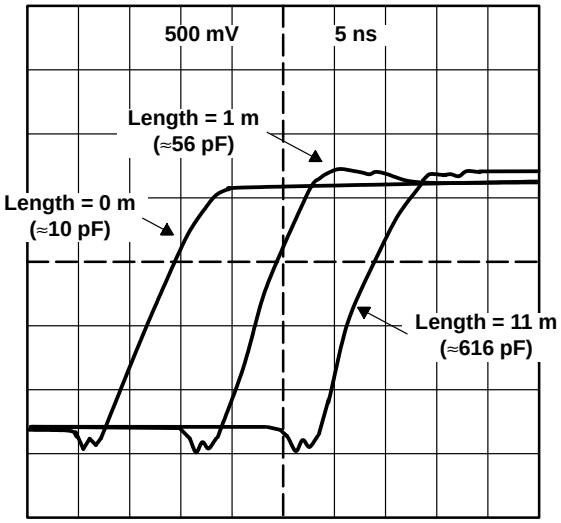

Figure 25. Waveform at SN74LS00 Output (C_L = 10 pF, 56 pF, and 616 pF)

The values for the low level of a bipolar device cannot be taken directly from data sheets. Transistor Q3 in Figure 24 is responsible for the output current I_{OL}. As with all semiconductor components, this parameter is nonlinear, and is influenced by the distribution of components in the circuit on such parameters as current gain, conductance, and resistance values. For this reason, only a rough calculation of the actual output current at low level is possible. As a first approximation, the internal resistance of the circuit at low level is lower than at high level. It follows that in the worst case, the increase of the delay time of the negative edge is always smaller than that of the positive edge (see equation 5). The precise value must be determined in individual cases by measurement.

6.4 Input and Output Capacitances of Digital Devices

All digital devices capacitively load the outputs of the circuits driving them. The input and output capacitances are given in Table 3. These are typical average values for the logic families shown. Different circuit configurations are used within a family, depending on the function and application. Therefore, wide variations from the values given in data sheets can occur with individual devices. In specific cases for new families, the values given in data sheets should be taken as a basis. If this data is not available, for example with older families, the user must make appropriate measurements if more precise values are needed.

The capacitances given in Table 3 are measured at the following voltages:

- Bipolar devices: V = 2.5 V
- CMOS devices: V = 0 V and V = 2.5 V

Table 3. Capacitances of Digital Devices

FAMILY	INPUT CAPACITANCE (pF)	OUTPUT CAPACITANCE (pF)	
		OPEN-COLLECTOR OUTPUT†	BUS DRIVER
SN74	3	5	–
SN74LS	3.5	3.5	5
SN74S	3.5	3.5	9
SN74ALS	2	4	5
SN74AS	4	–	10
SN74F	5	5	9
SN74HC	3	3	9
74AC/SN74AC	4	–	10
SN74BCT	6	–	12
SN74ABT	4	–	8
SN74LV	3	–	8
SN74LVC	4	–	8
SN74LVT	4	–	8

† Open-collector output of gates and other devices with low drive capability (e.g., SN74xx03). Open-collector outputs of bus drivers have the same output capacitance as totem-pole (3-state) outputs.

7 Bus Conflicts

If several bus drivers with 3-state outputs are connected to a single bus, it can often not be ensured that during the time when switching from one bus driver to another, both are not simultaneously active for a short time. For this short time, a short circuit of the outputs exists and, as a result, an overload of the circuit. This situation is known as *bus conflict*.

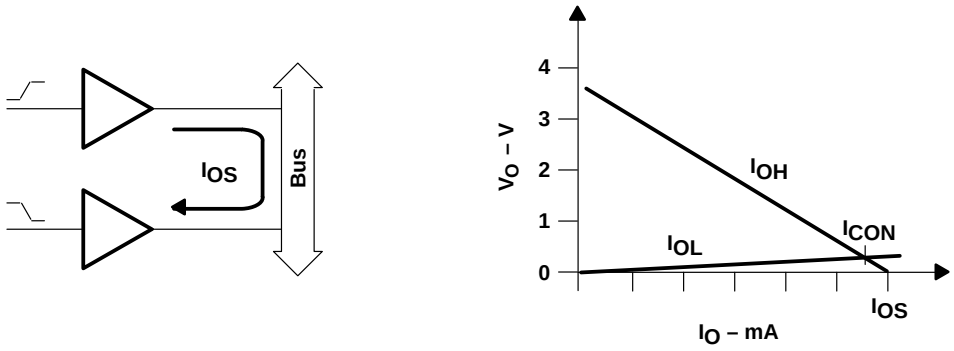

Figure 26. Determining the Short-Circuit Current With a Bus Conflict

The currents that result from bus conflict can be calculated by means of the output characteristics of the devices (see Table 2). As shown in Figure 26, the short-circuit current (I_{OS}) is limited by the high-output current of the devices involved in the bus conflict. With bus drivers having an output current of I_{OL} = 64 mA (SN74AS, SN74F, SN74BCT, SN74ABT, or SN74LVT), a current I_{OS} = 120 mA flows in such a case. The power dissipation (P_{conl}) of the output supplying the low level, as shown below, can be ignored.

$$P_{conl} = V_{OL} \times I_{OS} = 0.5\ V \times 120\ mA = 60\ mW \quad (6)$$

Even if all eight outputs of a bus driver are involved in a bus conflict, the total power dissipation is less than 500 mW. However, the situation is different at the outputs supplying the high level. In this case, the short-circuit power dissipation (P_{conh}) of each output is as follows:

$$P_{conh} = (V_{CC} - V_{OL}) \times I_{OS} = 4.5\ V \times 120\ mA = 0.54\ W \quad (7)$$

If all eight outputs of a bus driver are involved in this bus conflict, the total power dissipation is about 5 W. With Widebus circuits, it is 10 W and more.

To analyze the situation inside an IC under these extreme conditions, one has to know that the heat caused by this power dissipation is not immediately spread over the total chip. Rather, one has to consider a certain propagation speed of the heat, which is about 1 µm/µs. This means that during a bus conflict with a duration of only a few nanoseconds, the heat is not distributed over all the chip. In the first moment, the affected component inside the IC (the transistor or resistor) heats up. The resulting increase in temperature can be calculated by knowing the volume of the component in question and the thermal capacitance of silicon. By using the output stage of an ABT device (see Figure 27), this is shown in detail. Also, all voltages are shown in this circuit diagram that apply when the output, which should provide a high level, is forced to 0.5 V externally.

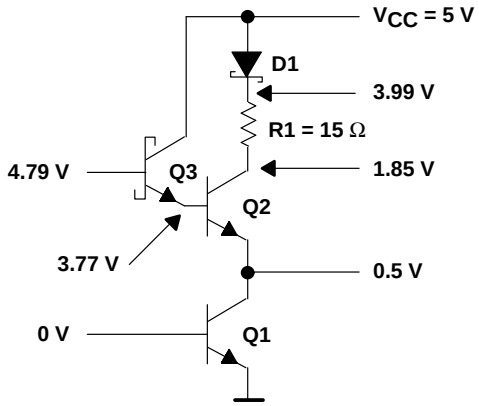

Figure 27. ABT Output-Stage Circuit Diagram

Table 4 shows the conditions in this output stage during a bus conflict. When calculating the volume of the single components, only that volume was considered that is related to the function of the component. For example, a transistor's total area was taken into account but the junction width only, where the heat is dissipated, was considered as the component's height.

Table 4. Output-Stage Conditions During a Bus Conflict

	VOLTAGE V (V)	CURRENT I (mA)	POWER DISSIPATION P (W)	VOLUME V (µm³)	POWER DISSIPATION/ VOLUME (W/µm³)
D1	1.01	142	0.156	3200	46×10^{-6}
R1	2.14	142	0.304	3840	79×10^{-6}
Q2	1.35	142	0.192	495	38×10^{-3}

According to this analysis, the highest power dissipation per volume unit is found in transistor Q2. This is because the junction width of only 0.5 µm was considered as height of this component. Using equation 8, calculate the temperature increase ($\Delta\vartheta$):

$$\Delta\vartheta = \frac{P \times t}{V \times c_P} \quad (8)$$

Where:

c_P = heat capacitance of silicon = 1.631×10^{-3} Ws/Kmm^3
P = power dissipation
t = time
V = volume

Considering a propagation speed of the heat of 1 µm/µs and a junction width of 0.5 µm, one can assume that during the first 500 ns of a bus conflict the heat is not distributed over the chip, but stays in the transistor junction. Under this condition, $\Delta\vartheta$ is as follows:

$$\Delta\vartheta = \frac{0.192\ \text{W} \times 500\ \text{ns}}{495\ \mu\text{m}^3 \times 1.631 \times 10^{-3} \frac{\text{W} \times \text{s}}{\text{K} \times \text{mm}^3}} = 119\ \text{K} \quad \textbf{(9)}$$

Short bus conflicts, with a duration of a few, or of a few tens of nanoseconds, cause a temperature increase of the component in question of about 10°C. Therefore, a degradation of the reliability of the component is unlikely. Furthermore, in well-designed systems, the period of bus conflicts is high compared to the duration of the bus conflict (period:duration > 10:1). Conservatively, the mean chip temperature should be calculated to ensure that this temperature does not increase beyond 150°C. Beyond this temperature, the thermal expansion coefficient of the plastic material of the package becomes different from the expansion coefficient of silicon. This fact is likely to lead to a mechanical stress at high temperatures, which may result in failure of the bond wire.

The total power dissipation (P_T) of a bus driver is calculated by the following equation:

$$P_T = P_O + (P_S \times t_S + P_C \times 2\tau + P_{con} \times t_{con}) \times f \times n \quad \textbf{(10)}$$

Where:

f	=	frequency
n	=	number of outputs at which a bus conflict occurs
P_{con}	=	power dissipation during bus conflict
P_C	=	power dissipation when discharging the bus capacitance
P_O	=	quiescent power dissipation
P_S	=	power dissipation resulting from current spikes when output switches
t_{con}	=	duration of bus conflict
t_S	=	duration of current spike
τ	=	signal propagation time on the bus

The power dissipation of a bus driver is calculated in a practical example in accordance with the following assumptions:

- Circuit: SN74F245
- P_O = 0.45 W (from data sheet)
- P_S = 5 V × 30 mA = 0.15 mW with t_s = 5 ns (measured)

To calculate the power dissipation (P_C) that occurs when charging the capacitance of the bus line, the voltage waveform at the output with the given load (the line impedance) must be known. The easiest way to determine this is to use the Bergeron diagram. With a line impedance of 30 Ω, a stable state is reached after double the time of the signal propagation with a positive edge. That is, for this time, a current is supplied into the line from the driver circuit. The amplitude of the preceding waveform and the output voltage of the circuit is about V_O = 2 V. The power dissipation during this time and under these load conditions is calculated as follows:

$$P_C = (V_{CC} - V_O) \times \frac{V_O}{Z_O} = (5\ \text{V} - 2\ \text{V}) \times \frac{2\ \text{V}}{30\ \Omega} = 0.2\ \text{W} \quad \textbf{(11)}$$

The signal propagation time on a backplane in a 19-inch rack (wire length about 40 cm) is τ = 10 ns.

Further, assuming a bus cycle time of 100 ns (f = 10 MHz), a duration of the bus conflict of 10 ns, and that all eight outputs of the device are involved, the resulting total power dissipation is as follows:

$$\begin{aligned} P_T &= 0.45\ \text{W} + (0.15\ \text{W} \times 5\ \text{ns} + 0.2\ \text{W} \times 2 \times 10\ \text{ns} + 0.53\ \text{W} \times 10\ \text{ns}) \times 10\ \text{MHz} \times 8 \\ &= 0.45\ \text{W} + (0.75\ \text{nW/s} + 4\ \text{nW/s} + 5.3\ \text{nW/s}) \times 10\ \text{MHz} \times 8 \\ &= 1.29\ \text{W} \end{aligned} \quad \textbf{(12)}$$

This power dissipation results in a rise of temperature of the chip, which, in turn, influences the reliability of the device. The chip temperature can be calculated as follows:

$$T_J = T_A + P_T \times R_{\Theta JA} \quad \textbf{(13)}$$

Where:

$R_{\Theta JA}$ = thermal resistance of package
T_A = ambient temperature
T_J = chip temperature

Table 5 shows the typical thermal resistance of the packages, which are mostly used for digital devices. These must be considered as typical values, because a number of factors determine the actual value, including chip size, lead-frame material, composition of the plastic, ambient air flow, and thermal properties of the circuit board. The values given apply if the device is soldered onto a PCB.

Table 5. Thermal Resistance of Plastic Packages in Still Air

NO. OF PINS	THERMAL RESISTANCE (°C/W)	
	DL PACKAGE	SO PACKAGE
14	86	117
16	80	110
20	78	95
24	73	85

According to Table 5, the thermal resistance of a 20-pin DL package is $R_{\Theta JA}$ = 78°C/W. This means that, in equation 8, the chip temperature would be about 100°C above the ambient temperature. The chip temperature must not be allowed to exceed 150°C, because the reliability would be reduced significantly. Therefore, the maximum permissible ambient temperature is, in this case, 150°C – 100°C = 50°C.

In cases in which bus conflict may occur, which is in most bus applications, power dissipation is of particular importance. There is usually nothing that can be done about dynamic conditions (the frequency of operation) without adversely affecting the performance of the system. Also, the overlap of operating states cannot always be prevented if worst-case conditions are taken into account. However, bus conflicts of a duration of a few, or of a few tens of nanoseconds should not be a problem. The choice of the most suitable components allows control of the quiescent power dissipation. With fast bipolar logic families (SN74S, SN74AS, and SN74F), the permissible total power dissipation might be exceeded because of their high quiescent power dissipation. Better, in this respect, are the SN74LS and SN74ALS series. Because of their lower quiescent-current requirements, bus conflicts do not result in overdissipation in most cases. Even better are devices from the BiCMOS series and all CMOS devices, although in CMOS parts, a part of the advantage of their low quiescent current is lost by their higher dynamic power dissipation.

One critical application area is bus conflicts during the power-on phase of a system. These bus conflicts occur because, during the power-on phase (system reset), the supervising circuit does not provide defined control signals even though the rest of the system may already be functional. Therefore, there is a high probability that various bus drivers may be accidentally activated at the same time. This, again, results in bus conflicts that may last several 100 ms (duration of the power-on phase or reset time). Because the thermal time constant of an IC is about 1ms to 5 ms, after this time expect the final temperature in the device to be determined by momentary power dissipation. If a total power dissipation of 5 W in an 8-bit device during this bus conflict is assumed, a theoretical 500°C overtemperature of the chip has to be considered. With Widebus circuits, the theoretical overtemperature is 1000°C. Mostly, these devices are immediately destroyed during these kinds of bus conflicts. Even if no defect is detected after such a bus conflict, a dramatic degradation of the device is expected, which leads to a final destruction of the component some time later.

An adequate design of the control logic prevents bus conflicts during the power-on phase of a system. Preventing bus conflicts is not easy because no defined supply voltage can be expected during the power-on phase. Therefore, no defined operation of the logic circuits can be expected. The supply-voltage range below 3 V usually is not critical. Many advanced bus drivers contain a supply-voltage monitor that disables the outputs (3-state) as long as the supply voltage is lower than about 3 V. Furthermore, below this voltage, an overload of the devices is unlikely, because under this condition, the drive capability is very limited. Above a supply voltage of 3 V, additional measures are necessary. One method is to connect a pullup resistor between the enable inputs of the bus-interface circuits and the positive supply rail. This may ensure a high level as long as the preceding control logic does not provide a defined logic level, but is not helpful if the control logic delivers a wrong logic level. A reliable solution is to disable all bus-interface circuits in question during the critical time with additional control logic (see Figure 28). In this circuit, a supply-voltage monitor (TLC7705) provides a signal that disables all bus drivers during the critical time period and may reset the main processor, which then resets the control logic of the system. For this kind of application, bus-interface circuits that provide two enable inputs, like the SN74ABT541, are advantageous. One control input controls the normal operation via the system-control logic. The other input is connected to the monitor device to disable the bus logic when an undefined system condition (e.g., during power on) is expected. If no second enable input is available, such as in a SN74ABT245, another gate is required to perform the additional disable function.

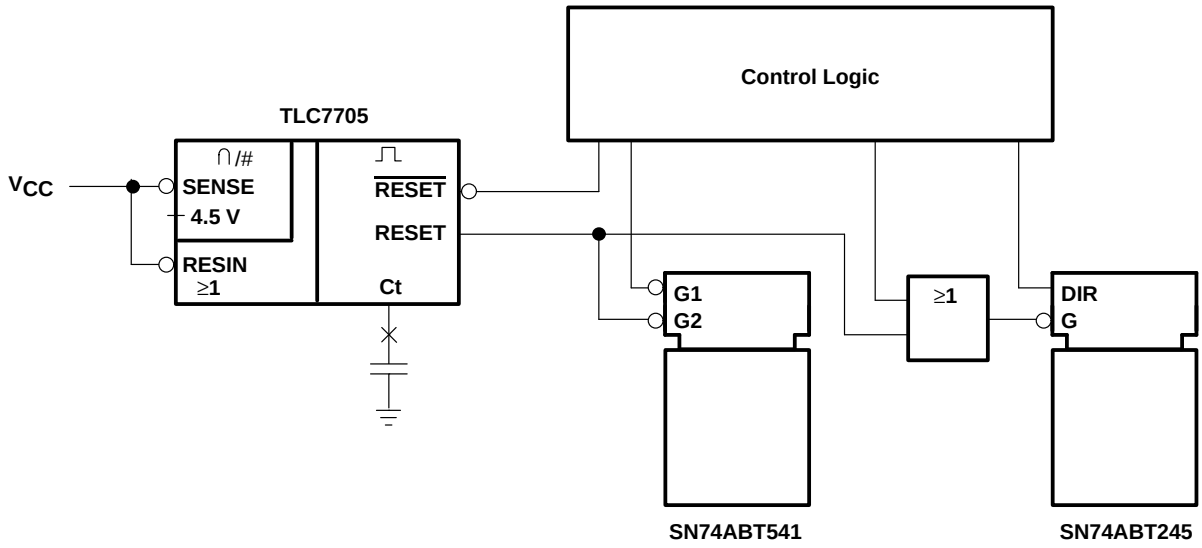

Figure 28. Bus Supervision During Power On

CAUTION:

Since considerably higher currents flow during bus conflicts on signal lines than with normal operation, the noise margin in the system is reduced accordingly. This can result in faulty operation and care should be taken to avoid bus conflicts.

8 Backdriving

The testing of highly complex electronic systems must ensure that the system or subsystem operates faultlessly. For this purpose, it is advantageous to install at the system level diagnostic programs that are able to recognize and localize faults. Certain limitations are unavoidable with self-testing because a defective system may no longer be able to seek and localize faults. This method usually breaks down completely when individual component groups are being tested because fault diagnosis on their own is generally too limited. In such cases, additional test equipment that stimulates the component group with special test signals, test samples, or patterns, and analyzes the results is necessary.

If all relevant circuit segments in the component group can be addressed via a defined interface, e.g., built-in testability (BIT), testing can be performed without additional test circuits and adapters. Test bus IEEE 1149.1 (JTAG), with an appropriate IC interface, allows testing of all circuits, the connections between them, and the complete subsystem.

If this option is not available, appropriate signals may be injected into the circuit from outside to achieve the required circuit stimulation. For this, the inputs to the circuits to be tested must be supplied with the necessary voltages (e.g., logic low or high) via nail-bed adapters and the reaction at the outputs of these circuits is monitored. In this way, the functions of complex systems can be tested step by step and the most common faults recognized, such as:

- Solder bridges and broken metallization
- Incorrect, faulty, damaged, or missing devices
- Functional disturbances and signal-processing faults

Because only a few single devices are accessed at a time, only the special, appropriate functions (e.g., the truth table of a gate) need to be known, not the function of the complete device group. In this way, standard test program libraries can be used to put together the complete test program. With this method, large systems also can be tested step by step without using excessively complex test procedures.

The stimulation of the circuit to be tested may present a problem. For example, the inputs of gate G3 (see Figure 29) must be switched to a particular potential. These same inputs are already controlled by other devices (G1 and G2), which supply their own signals to the gates to be tested. The test equipment must be able to force another voltage on to the same node as is supplied by the existing circuit. The expression commonly used here is *backdriving* or *node forcing*. The output of a device is forced from outside into a state not corresponding to its normal control-logic state.

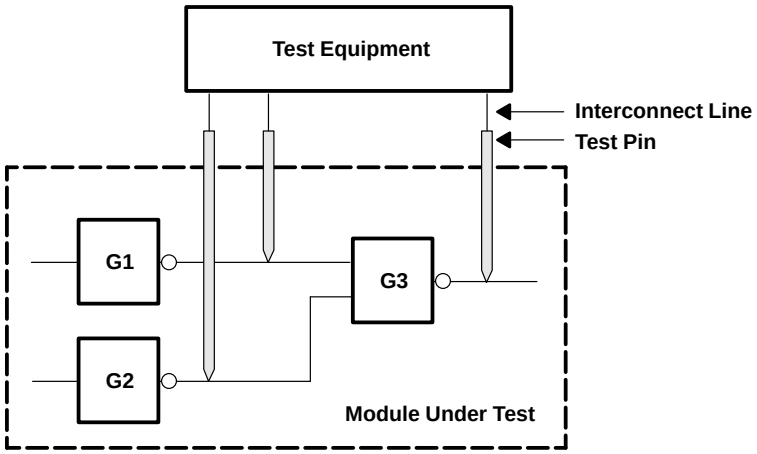

Figure 29. Feeding Test Signals Into a Node Test Point

The test equipment must have substantial drive capability to force the IC into another logic state. Table 2 gives the short-circuit current at high level of the most important logic families. The situation in which the test equipment must force an output to low level is not the most demanding requirement. Currents of up to several hundred milliamperes must be provided to force from outside an output that is supplying a low level into a high-level state.

Serious interference arises when the high currents are switched on or off and line reflections occur on the lines connecting the test equipment and the circuit being tested. All these effects can result in a real or apparent malfunction of the circuit being tested. This test method is of limited use when the precise timing of fast circuits must be assessed.

When injecting the test-signal current into the outputs, which must then be forced into an inverted state, the devices usually are driven far outside their maximum permissible ratings. This may damage or destroy the devices. At the very least, their reliability and, therefore, their operating life, is adversely affected. In recent years, the drive capability (maximum output currents) of ICs has been steadily increased in the interest of improved technical performance. Modern bus-driver currents of 500 mA and more are needed to force the outputs of devices to particular logic levels (see Figure 30). The high current densities in the internal connections of ICs can cause a drift of metallic ions, or so-called electromigration. This effect begins at current densities of 3×10^5 to 10^6 A/cm^2. Metallic ions are released from the grain boundaries and then drift in the inverse direction of current flow (in the direction of the electron flow). If the excessive current density lasts long enough, the interconnections are eroded.

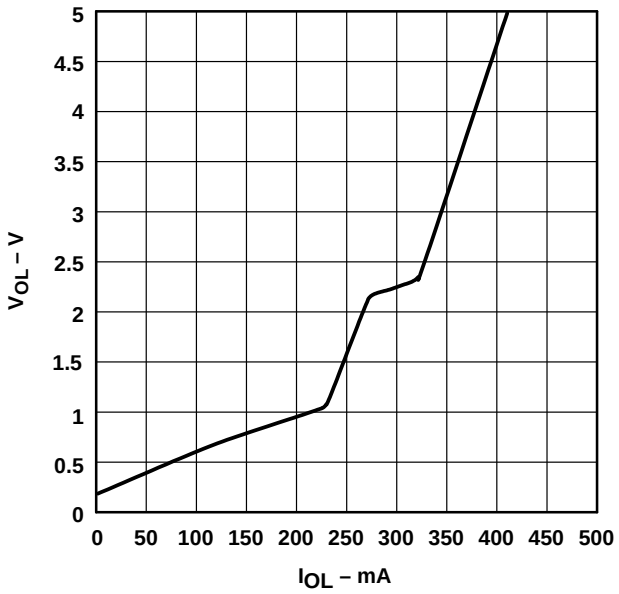

Figure 30. Low-Logic-Level Output Characteristics of SN74AS645

When backdriving, the most important effect is the extreme rise in temperature that occurs in the chip during the test. The heat that results must be conducted away via the package. The equivalent circuit of Figure 31 shows the thermal relationships in the package.

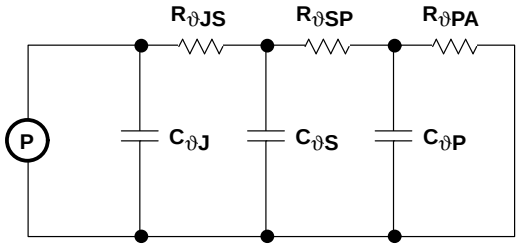

Figure 31. Thermal Resistances in an IC

The thermal source (P) first fills up the thermal capacitance of the semiconductor junction. The heat spreads, via $R_{\vartheta JS}$, in the complete substrate (chip) of the IC. From there, the heat flows, via the resistance ($R_{\vartheta SP}$), into the package and then, via the resistance ($R_{\vartheta PA}$), to the ambient environment. Only the sum of the thermal resistances $R_{\vartheta JU} = R_{\vartheta JS} + R_{\vartheta SP} + R_{\vartheta PA}$ (thermal-resistance junction ambient) is given in data books (see Table 5). This resistance is not helpful for the problem under consideration but it can be used to calculate the temperature in a stable state. Rapid temperature increases, such as result from backdriving, cannot be calculated from the sum of thermal resistances. The thermal capacitance and thermal conductivity of the chip can be calculated, but it is better to determine the thermal behavior through measurements (see Figure 32).

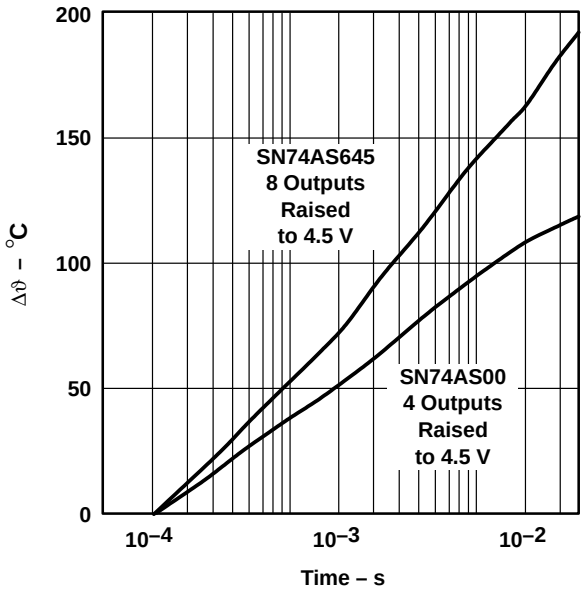

Figure 32. Thermal Behavior in an IC

Figure 32 shows that, with an SN74AS645, a temperature rise in the chip of 100°C must be expected after 2 ms. After 10 ms, temperatures are attained that are not permissible in plastic packages. CMOS and BiCMOS circuits have a very low power dissipation and do not behave better in this particular case. With these modern components, expect at least the same driving capability. The short-circuit current at the output of an ACL IC is >250 mA. It is ultimately these currents that are responsible for the high power dissipation during backdriving.

The following rules always should be observed when using the test methods discussed:

- Backdriving should be used only when the state required at the node point in question can be reached in no other way.
- The maximum permissible power dissipation of an IC should not, under any circumstances, be exceeded.
- Outputs that are at a low-level state, as a result of their logic functions, may be raised to a level of V_O = 3 V for a short period by backdriving. The energy, which as a result of this backdriving is injected into the device ($V_O \times I_{OL} \times t_{pd}$), must not exceed 25 mW/s. The current that results in an output should not exceed a value of I_{OL} = 300 mA. The pulse duration must not exceed t_d = 100 ms. To keep the thermal stress within acceptable limits, the duty cycle of the pulses (duration of the pulse ÷ duration of the period) should be less than 1:10.
- Outputs that are in a high-level state as a result of their logic functions may be lowered to a level of 0 V for a short time by means of backdriving. One output of a device may be short circuited to ground, in such a case, for maximum t_d = 100 ms. The product of the output current, the supply voltage, and the pulse duration ($I_{OH} \times V_{CC} \times t_{pd}$) must not exceed 25 mW/s. If n outputs are simultaneously short circuited to ground, limit the total energy injected into the device under test ($I_{OH} \times V_{CC} \times t_{pd}$) to 25 mW/s. To keep the thermal stress within reasonable limits, the duty cycle of the short circuit (short-circuit duration ÷ repetition time) should be less than 1:10.
- All voltages, including peak voltages of overshoots/undershoots, must be within the absolute maximum ratings on data sheets.
- Simultaneous backdriving of several outputs in parallel (wired OR) with a common current source is not permissible. Since current sharing cannot be predicted, there is danger of overloading the circuit.
- The chip temperature of the circuit under test must not exceed 125°C.
- Open-circuit (unterminated) lines should be avoided to prevent faults caused by reflection.

Semiconductor device manufacturers consider testing with backdriving as involving a measure of risk. The danger of overloading devices cannot be excluded since they are operated in regions that may lie far outside those for which they were designed. For this reason, no statement about the reliability of devices that are subjected to this test procedure can be made. TI does not use such test methods. Such test methods are not permissible in many (e.g., military) areas of application.

9 Summary

This report provides the designer of digital systems information that is not found in data books, but which is of interest and necessary in many applications. The differences between individual circuit families have been discussed. The circuit design techniques used with various devices, combined with the different technologies used to manufacture them, often make it difficult to give specific design rules; in many cases it is possible to give only very general guidance. In practice, few parameters are actually measured, particularly with older devices. In all such cases, this report provides guidelines that enable the designer to predict the behavior of circuits in a system.

Acknowledgement

The author of this document is Eilhard Haseloff.