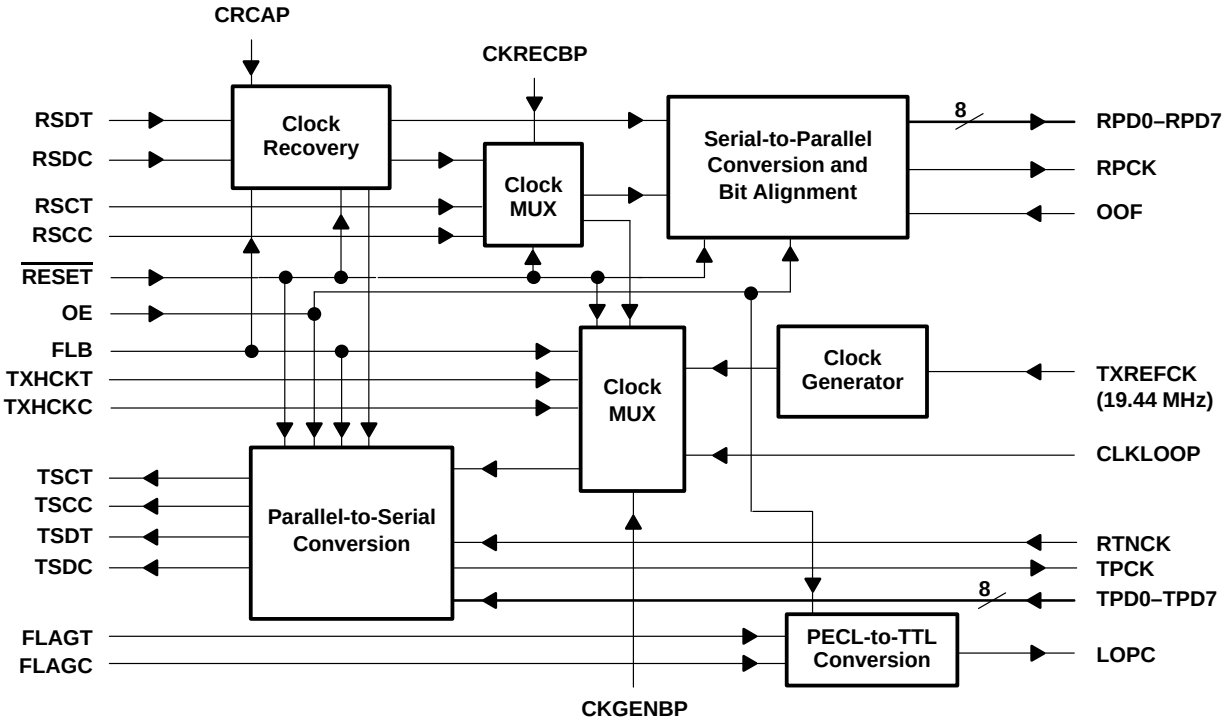
- **Serial-to-Parallel/Parallel-to-Serial Conversion for 622.08-Mbit/s Data Streams**
- **Selectable Transmit Clock Source**
- **Performs Clock Recovery From Received Data**
- **Performs Bit-Alignment Function for SONET/SDH Frames**
- **Loopback Capability Increases Product Versatility**
- **Conforms to SONET/SDH Standards**

description

The TNETA1610 STS-12c/STM-4 receiver/transmitter provides a versatile integrated solution for clock recovery and data serialization/deserialization for 622.08-Mbit/s data streams used in STS-12c/STM-4 systems. The TNETA1610 conforms to SONET/SDH standards and performs all the functionality necessary to simultaneously convert the serial data to and from byte-wide data and recover the embedded clock from received data. On the receive side, bit alignment is performed on the serial input data such that parallel data is output on SONET-/SDH-byte boundaries. In addition, loopback features and versatile clock-selection capabilities are included. The TNETA1610 is characterized for operation over a temperature range of –40°C to 85°C.

functional block diagram



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Terminal Functions

high-speed serial interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RSCT, RSCC		I (PECL)	Receive serial clock (true and complement). RSCT and RSCC are a differential 622.08-MHz clock that accompanies the incoming serial data on RSDT and RSDC when CKRECBP is high.
RSDT, RSDC		I (PECL)	Receive serial data (true and complement). RSDT and RSDC are differential data. When CKRECBP is high, RSDT/RSDC is accompanied by clock RSCT/RSCC such that RSDT/RSDC is valid on the rising edge of RSCT.
TSCT, TSCC		O (PECL)	Transmit serial clock (true and complement). TSCT and TSCC are a differential, phase-aligned 622.08-MHz clock.
TSDT, TSDC		O (PECL)	Transmit serial data (true and complement). TSDT and TSDC are differential data that is valid on the rising edge of TSCT.
TXHCKT, TXHCKC		I (PECL)	Transmit high-speed clock (true and complement). TXHCKT and TXHCKC are a differential 622.08-MHz clock source used when CKGENBP is high and CLKLOOP and FLB are low.

control signals (see Table 1)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CKGENBP		I (TTL)	Clock-generation bypass. When CKGENBP is low, the 622.08-MHz transmit clock is generated from the 19.44-MHz clock on TXREFCK. When CKGENBP is high, a 622.08-MHz clock provided on TXHCKT/TXHCKC is used for transmit operations.
CKRECBP		I (TTL)	Clock-recovery bypass. When CKRECBP is high, the 622.08-MHz clock on RSCT/RSCC is used in the receiver. No clock is recovered from the data.
CLKLOOP		I (TTL)	Transmit clock-source loop. When CLKLOOP is high, the clock used in the receive data stream is also used for transmit operations.
FLB		I (TTL)	Facility loopback. When FLB is high, the receive serial data and clock are looped back to the transmit serial clock and data output.
OE		I (TTL)	Output enable. OE enables or disables all TTL outputs. When OE is low, RPCK, RPD0–RPD7, LOPC, and TPCK are placed in the high-impedance state. When OE is high, these terminals function normally.
$\overline{\text{RESET}}$		I (TTL)	Reset. The TNETA1610 is reset by taking $\overline{\text{RESET}}$ low. This action can result in the loss of transmit or receive data that is being processed.
TXREFCK		I (TTL)	Transmit reference clock. TXREFCK is a 19.44-MHz clock that must be provided if CKGENBP, CLKLOOP, and FLB are low.

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Terminal Functions (Continued)

receive-parallel interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
OOF		I (TTL)	Out of frame. OOF is generated by subsequent processing elements to control bit alignment in the TNETA1610. When OOF goes high, the TNETA1610 begins a search of the received data for a string of twelve consecutive A1 bytes (i.e., twelve F6s). Once this sequence is found, the TNETA1610 aligns the byte-wide output data with the A1-byte boundaries. The TNETA1610 does not realign the output when OOF is low.
RPCK		O (TTL)	Receive parallel clock. RPCK accompanies the data on RPD0–RPD7 for timing purposes.
RPD0–RPD7		O (TTL)	Receive parallel (byte-wide) data. RPD0–RPD7 are valid on the rising edge of RPCK.

transmit-parallel interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RTNCK		I (TTL)	Return clock. RTNCK accompanies data on TPD0–TPD7 such that the data is read into the TNETA1610 on low-to-high transitions of RTNCK. RTNCK can be tied to TPCK if timing requirements between TPCK and TPD0–TPD7 can be met.
TPCK		O (TTL)	Transmit clock. TPCK is an output to subsequent processing elements that coordinates data transfers on TPD0–TPD7.
TPD0–TPD7		I (TTL)	Transmit parallel (byte-wide) data. TPD0–TPD7 are read into the TNETA1610 on low-to-high transitions of RTNCK.

miscellaneous signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CRCAP			Capacitor connection for clock-recovery PLL filter.
FLAGT/FLAGC		I (PECL)	Loss-of-optical-carrier alarm (true and complement). This differential input is connected to a fiber-optic receiver loss-of-optical-carrier output to provide a TTL-level signal (LOPC) indicating when the incoming optical signal is lost.
GND1			Ground. GND1 is the 0-V reference for TTL circuits.
GND2			Ground. GND2 is the 0-V reference for PECL circuits.
LOPC		O (TTL)	Loss-of-optical-carrier. LOPC is a TTL version of FLAGT/FLAGC. LOPC is high when FLAGT/FLAGC are at a high level.
NC			No connection. Leave open.
TEST			Manufacturing test. Leave open.
THGND			Thermal ground. THGND terminals are used as thermal connections to the board ground plane. There is no electrical connection in the TNETA1610.
V_{CC1}			Supply voltage. V_{CC1} is the 5 V ± 5 % supply for TTL circuits.
V_{CC2}			Supply voltage. V_{CC2} is the 5 V ± 5 % supply for PECL circuits.

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detailed description

transmit operation

The transmit parallel interface consists of TTL-compatible byte-wide input data (TPD0–TPD7), a TTL-compatible transmit output clock (TPCK), and a TTL-compatible return clock input (RTNCK). TPCK is an output to associated processing elements (i.e., a framer) that controls the output of byte-wide transmit data from such devices. The return clock and data are input to the TNETA1610 such that byte-wide transmit data (TPD0–TPD7) is clocked into the TNETA1610 on low-to-high transitions of RTNCK. If a return clock is not available, RTNCK can be tied toTPCK provided the timing requirements between TPCK and TPD0–TPD7 can be met.

The byte-wide data is converted to a 622.08-Mbit/s serial-data stream that is sent out differentially on transmit serial-data true (TSDT) and transmit serial-data complement (TSDC). In addition, a phase-aligned 622.08-MHz clock is sent out differentially on transmit serial-clock true (TSCT) and transmit serial-clock complement (TSCC). The serial output data is valid on the rising edge of TSCT. TSDT, TSDC, TSCT, and TSCC are pseudo-ECL-compatible outputs.

The transmit clock is generated from a 19.44-MHz input (TXREFCK) using an analog phase-lock loop. Two other clock sources can be utilized as alternatives. If CKGENBP is at a high logic level, an external 622.08-MHz clock is used. This clock is a differential input on pseudo-ECL-compatible terminals TXHCKT and TXHCKC. If CKRECBP is at a low logic level and CLKLOOP or FLB is at a high logic level, the clock recovered from the receive data stream is used for transmit operations. TXREFCK is used when CKGENBP, FLB, and CLKLOOP are at a low logic level.

A facility-loopback (FLB) option is also available. When FLB is at a high logic level, the data input into the receiver and the recovered clock are looped back to the transmitter outputs. This allows a method for loopback testing of a system and for testing the clock-recovery function.

Transmit functions are reset by taking $\overline{\text{RESET}}$ low. This action can result in the loss of both transmit and receive data.

receive operation

Serial data is provided to the TNETA1610 on true and complement, pseudo-ECL-compatible inputs RSDT and RSDC. A phase-locked loop is used to recover the embedded clock from the serial-data stream. If the clock-recovery function is bypassed (by setting CKRECBP to a high logic level), a 622.08-MHz pseudo-ECL-compatible clock must be provided as a differential signal on RSCT and RSCC. The RSCT and RSCC clock is not required if CKRECBP is at a low logic level.

The serial data is converted to byte-wide data and retimed to the recovered clock (or external clock if CKRECBP is at a high logic level). The byte-wide output data (RPD0-RPD7) is valid on the rising edge of RPCK. RPD0-RPD7 and RPCK are TTL-compatible outputs.

The TNETA1610 utilizes the out-of-frame (OOF) signal generated by subsequent processing elements for bit alignment. When OOF goes high, the TNETA1610 begins searching the received data for a string of 12 consecutive A1 bytes (twelve hex F6s). Once this sequence is found, the TNETA1610 aligns the byte-wide data output with the A1-byte boundaries so that subsequent data (i.e., the A2 bytes) is properly aligned. The subsequent processing element (i.e., a framer) must detect and monitor the byte-aligned data for complete SONET/SDH framing patterns (twelve A1s followed by twelve A2s) to ensure standards compliance for loss of frame, etc. The TNETA1610 does not realign the output when OOF is low.

The TNETA1610 also performs a pseudo-ECL-to-TTL conversion of the loss-of-optical-carrier signal available in many optical receivers. The TTL-compatible output (LOPC) goes high when the differential pseudo-ECL inputs (FLAGT and FLAGC) go active, indicating an error condition. Thus, other components can avoid pseudo-ECL circuitry by using the TNETA1610's LOPC output. Furthermore, when a loss-of-optical-carrier condition is detected, the processing of received data is interrupted such that receive data outputs (RPD0–RPD7) are held low, and the output clock (RPCK) may drift from 622.08 MHz.

receive operation (continued)

An output-enable (OE) terminal is provided to enable/disable all TTL outputs. When OE is low, RPCK, RPD0–RPD7, LOPC, and TPCK are held in the high-impedance state. When OE is high, these terminals function as previously described.

Receive functions are reset by taking $\overline{\text{RESET}}$ low. This action can result in the loss of any data being processed.

data/clock source control

There are five control inputs to the TNETA1610 that change the source of data (and/or clock) for a given output. The effects of these inputs (OE, FLB, CLKLOOP, CKGENBP, and CKRECBP) are indicated in Table 1.

Table 1. Data/Clock Source Control

STATE OF INPUTS					SOURCE OF DATA/CLOCK FOR OUTPUTS				
OE	FLB	CLKLOOP	CKGENBP	CKRECBP	TSDT/TSDC	TSCT/TSCC	TPCK	RPD0-RPD7	RPCK
0	0	0	0	0	N/A†	TXREFCK	High impedance	High impedance	High impedance
0	0	0	0	1	N/A†	TXREFCK	High impedance	High impedance	High impedance
0	0	0	1	0	N/A†	TXHCKT/ TXHCKC	High impedance	High impedance	High impedance
0	0	0	1	1	N/A†	TXHCKT/ TXHCKC	High impedance	High impedance	High impedance
0	0	1	0	0	N/A†	Receive recovered	High impedance	High impedance	High impedance
0	0	1	0	1	N/A†	RSCT/RSCC	High impedance	High impedance	High impedance
0	0	1	1	0	N/A†	Receive recovered	High impedance	High impedance	High impedance
0	0	1	1	1	N/A†	RSCT/RSCC	High impedance	High impedance	High impedance
0	1	0	0	0	RSDT/RSDC	Receive recovered	High impedance	High impedance	High impedance
0	1	0	0	1	RSDT/RSDC	RSCT/RSCC	High impedance	High impedance	High impedance
0	1	0	1	0	RSDT/RSDC	Receive recovered	High impedance	High impedance	High impedance
0	1	0	1	1	RSDT/RSDC	RSCT/RSCC	High impedance	High impedance	High impedance
0	1	1	0	0	RSDT/RSDC	Receive recovered	High impedance	High impedance	High impedance
0	1	1	0	1	RSDT/RSDC	RSCT/RSCC	High impedance	High impedance	High impedance
0	1	1	1	0	RSDT/RSDC	Receive recovered	High impedance	High impedance	High impedance
0	1	1	1	1	RSDT/RSDC	RSCT/RSCC	High impedance	High impedance	High impedance
1	0	0	0	0	TPD0-TPD7	TXREFCK	TXREFCK	RSDT/RSDC	Receive recovered
1	0	0	0	1	TPD0–TPD7	TXREFCK	TXREFCK	RSDT/RSDC	RSCT/RSCC
1	0	0	1	0	TPD0–TPD7	TXHCKT/ TXHCKC	TXHCKT/ TXHCKC	RSDT/RSDC	Receive recovered

† This is not a normal operating condition. As no clock is output on TPCK, valid data cannot be properly input on TPD0–TPD7. Thus, data output on TSDT/TSDC may be invalid.

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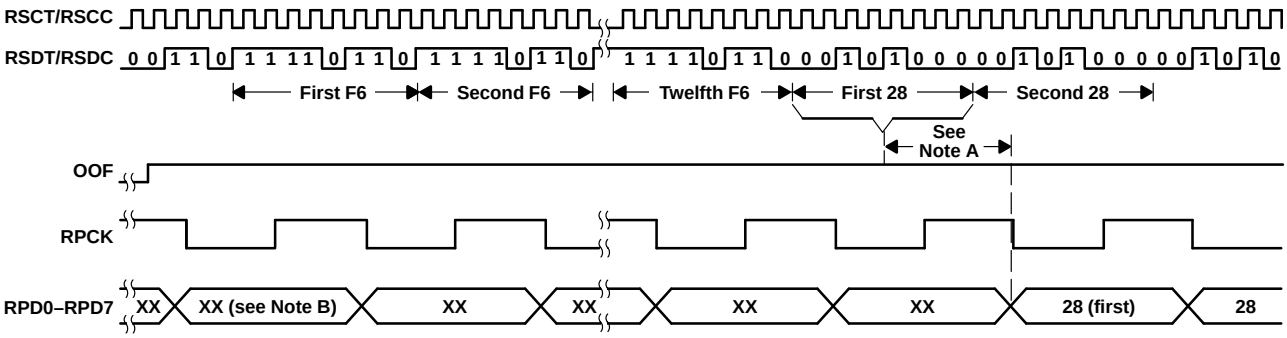
Table 1. Data/Clock Source Control (Continued)

STATE OF INPUTS					SOURCE OF DATA/CLOCK FOR OUTPUTS				
OE	FLB	CLKLOOP	CKGENBP	CKRECBP	TSDT/TSDC	TSCT/TSCC	TPCK	RPD0-RPD7	RPCK
1	0	0	1	1	TPD0–TPD7	TXHCKT/ TXHCKC	TXHCKT/ TXHCKC	RSDT/RSDC	RSCT/RSCC
1	0	1	0	0	TPD0–TPD7	Receive recovered	Receive recovered	RSDT/RSDC	Receive recovered
1	0	1	0	1	TPD0–TPD7	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	0	1	1	0	TPD0–TPD7	Receive recovered	Receive recovered	RSDT/RSDC	Receive recovered
1	0	1	1	1	TPD0–TPD7	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	1	0	0	0	RSDT/RSDC	Receive recovered	Receive recovered	RSDT/RSDC	Receive recovered
1	1	0	0	1	RSDT/RSDC	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	1	0	1	0	RSDT/RSDC	Receive recovered	Receive recovered	RSDT/RSDC	Receive recovered
1	1	0	1	1	RSDT/RSDC	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	1	1	0	0	RSDT/RSDC	Receive recovered	Receive recovered	RSDT/RSDC	Receive recovered
1	1	1	0	1	RSDT/RSDC	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	1	1	1	0	RSDT/RSDC	Receive recovered	Receive recovered	RSDT/RSDC	Receive recovered
1	1	1	1	1	RSDT/RSDC	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC

bit alignment

Figure 1 illustrates the bit-alignment function in the TNETA1610.



NOTES: A. After the 12th contiguous F6 is detected, the bit alignment is adjusted so that the next eight bits (the first A2 byte) are grouped together and sent out on RPD0–RPD7 after some delay time through the device.
B. Even when OOF is high, the TNETA1610 continues to convert the serial-input data to parallel-output data. While data is present at the output, XX is shown to indicate that the alignment of the serial data into bytes on RPD0–RPD7 may not be known.

Figure 1. Bit Alignment

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC1}: TTL (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range, V_{CC2}: PECL (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I: TTL . . . . . –1.2 V to 7 V
PECL . . . . . 0 V to V_{CC}
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC1}	Supply voltage, TTL		4.75	5.25	V
V_{CC2}	Supply voltage, PECL		4.75	5.25	V
V_{IH}	High-level input voltage	TTL	2		V
		PECL (see Note 2)	V_{CC}–1.15	V_{CC}–0.80	
V_{IL}	Low-level input voltage	TTL		0.8	V
		PECL (see Note 2)	V_{CC}–1.90	V_{CC}–1.50	
T_A	Operating free-air temperature		–40	85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_{IK} = – 18 mA			–1.2	V
V_{OH}	High-level output voltage‡	TTL	V_{CC} = 4.75 V,	I_{OH} = – 4 mA	4.25			V
		PECL–TSDT, TSDC	V_{CC} = 4.75 V to 5.25 V		V_{CC}–1.03		V_{CC}–0.85	
		PECL–TSCT, TSCC	V_{CC} = 5 V			V_{CC}–1.0		
V_{OL}	Low-level output voltage‡	TTL	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
		PECL–TSDT, TSDC	V_{CC} = 5 V to 5.25 V		V_{CC}–1.85		V_{CC}–1.62	
		PECL–TSCT, TSCC	V_{CC} = 5 V			V_{CC}–1.6		
$V_{O(PP)}$	Output voltage swing, PECL‡	PECL–TSCT, TSCC	V_{CC} = 4.75 V to 5.25 V		400			mV
I_I	Input current	TTL	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			± 300	µA
I_{IH}	High-level input current	PECL	V_{CC} = 5.25 V,	V_I = 4.45 V			25	µA
I_{IL}	Low-level input current	PECL	V_{CC} = 5.25 V,	V_I = 3.35 V			± 25	µA
I_{CC}	Supply current§		V_{CC} = 5.25 V,	I_O = 0				mA
I_{CC}	Supply current‡		V_{CC} = 5.25 V					mA
C_i	Input capacitance	TTL						pF

‡ PECL outputs are terminated with a 50-Ω resistor to V_{CC}–2 V.

§ PECL outputs are not terminated.

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timing requirements (see Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{su(RSDT/RSDC)}$	Setup time, RSDT/RSDC valid before RSCT/RSCC↑	500		ps
2	$t_{h(RSDT/RSDC)}$	Hold time, RSDT/RSDC valid after RSCT/RSCC↑	500		ps

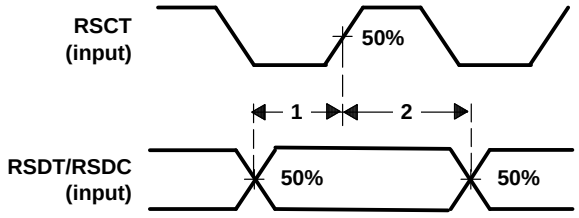

Figure 2. Receive Serial Interface

operating characteristics (see Figure 3)

NO.			MIN	MAX	UNIT
1	t_{csp}	Deviation of clock sampling point, receive parallel data	– 3.6	3.6	ns

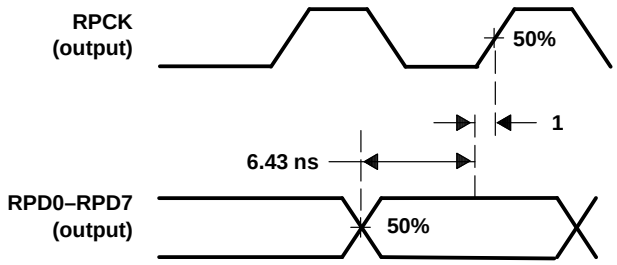

Figure 3. Receive Parallel Interface

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operating characteristics (see Figure 4)

NO.			MIN	MAX	UNIT
1	t_{csp}	Deviation of clock sampling point, transmit serial data	– 200	200	ps

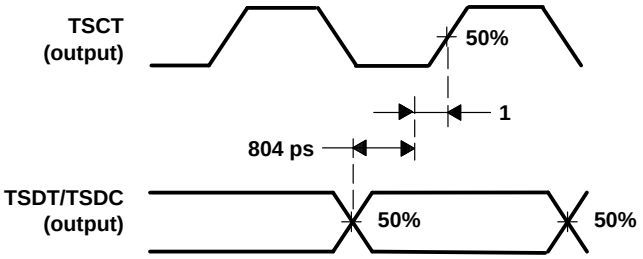

Figure 4. Transmit Serial Interface

timing requirements (see Figure 5)

NO.			MIN	MAX	UNIT
1	t_{csp}	Delay time, TPCK↑ to TPD0–TPD7 valid (RTNCK tied to TPCK)	2	10	ns

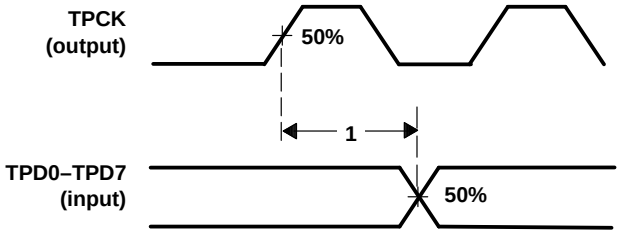

Figure 5. Transmit Parallel Interface

timing requirements (see Figure 6)

NO.			MIN	MAX	UNIT
1	$t_{su(TPD0–TPD7)}$	Setup time, TPD0–TPD7 valid before RTNCK↑	3.6		ns
2	$t_{h(TPD0–TPD7)}$	Hold time, TPD0–TPD7 valid after RTNCK↑	3.6		ns

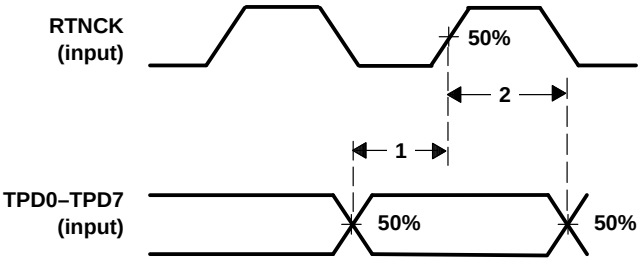

Figure 6. Transmit Parallel Interface Using Return Clock

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