- **Termination/Generation of 155.52-Mbit/s or 622.08-Mbit/s SONET/SDH Frames Carrying ATM Cells; Including:**
  - **Frame Scrambling/Descrambling**
  - **Pointer Processing**
  - **ATM-Cell Delineation**
  - **ATM-Cell Extraction/Insertion**
  - **ATM-Cell Payload Scrambling/Descrambling**
  - **Cell-Rate Decoupling**
- **Access to Receive and Transmit Transport-Overhead (TOH) and Path-Overhead (POH) Bytes Through the Controller Interface**
- **Detects Multiple-Bit Errors and Corrects Single-Bit Errors in the 5-Byte ATM Headers of Incoming ATM Cells**
- **Separate Serial Receive- and Transmit-Data Communication Ports Allow Access to Data Communications and Orderwire-Overhead Bytes**
- **Alarm Generation/Checking in Accordance With BellCore, ANSI, and ITU-T Specifications**
- **Performance Monitors/Counters Provide Statistics on B1/B2/B3 Coding Violations, B1/B2/B3 Block Errors, Line and Path Far-End Block Errors (Line FEBEs and Path FEBEs) and Other Status Data**
- **Supports Boundary Scan Through a 5-Wire JTAG Interface in Accordance With IEEE Std 1149.1-1990 (Includes IEEE Std 1149.1a-1993) IEEE Standard Test-Access Port and Boundary-Scan Architecture**

description

The synchronous optical network (SONET)/synchronous digital hierarchy (SDH) asynchronous transport mode (ATM) line-interface receiver/transmitter provides a versatile solution for transporting ATM cells over the SONET/SDH network at 155.52 Mbit/s or 622.08 Mbit/s.

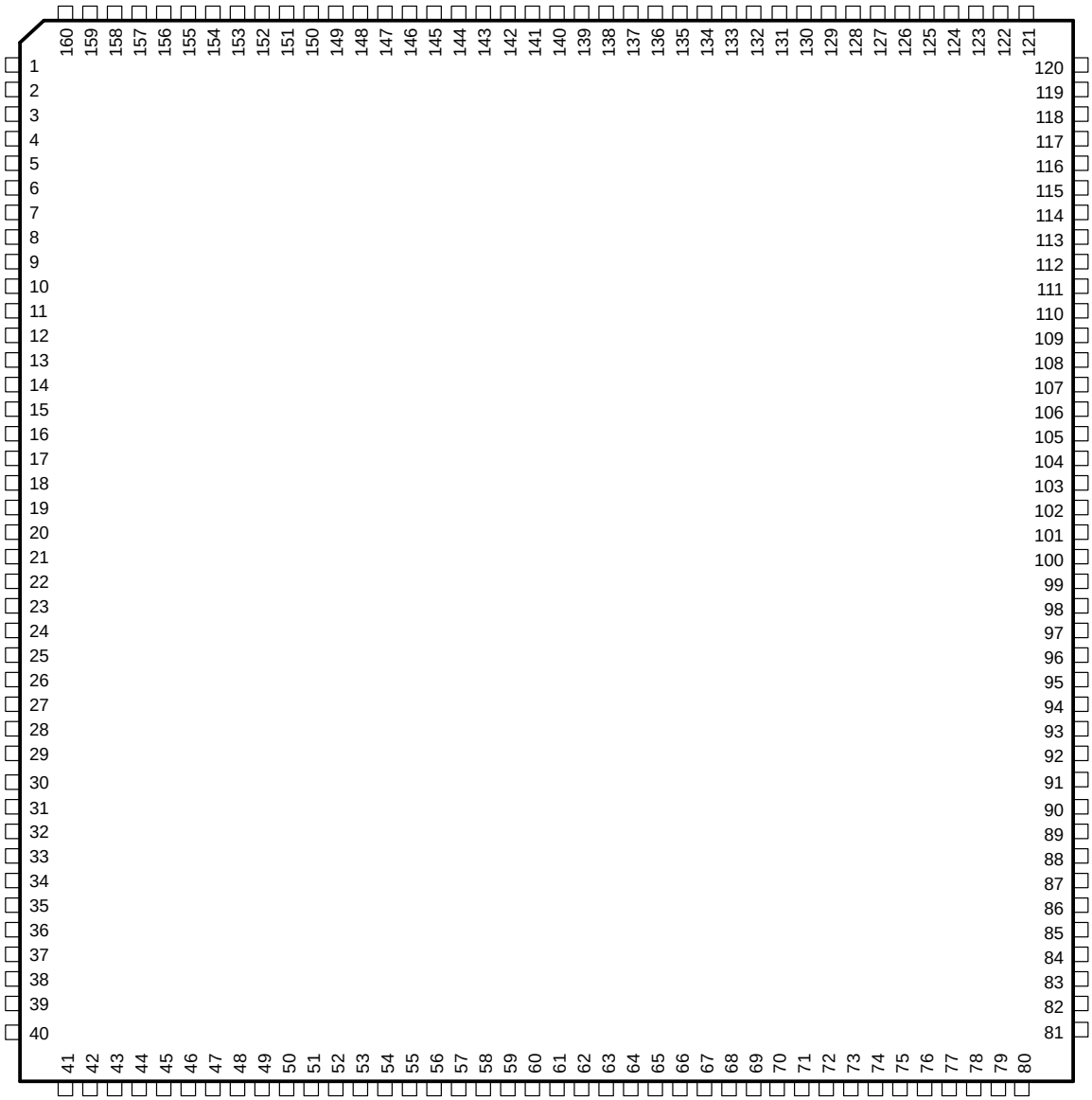
On the receive side, the TNETA1600 accepts byte-wide data aligned to proper SONET- /SDH-byte boundaries, performs frame alignment and descrambling, and extracts SONET/SDH payload and overhead. The overhead is placed in the receive-overhead RAM where each byte can be accessed through the controller interface. Cell boundaries are established in the payload and ATM cells are extracted, descrambled, and passed to the receive output FIFO for output to the ATM-layer device (i.e., a reassembly device).

On the transmit side, complete ATM cells are scrambled and placed in a SONET/SDH synchronous payload envelope (SPE). Transport- and path- overhead bytes are programmable through the transmit-overhead RAM. The overhead and payload are scrambled and sent out as a byte-wide data stream.

The TNETA1600 is characterized for operation over a temperature range of –40°C to 85°C.

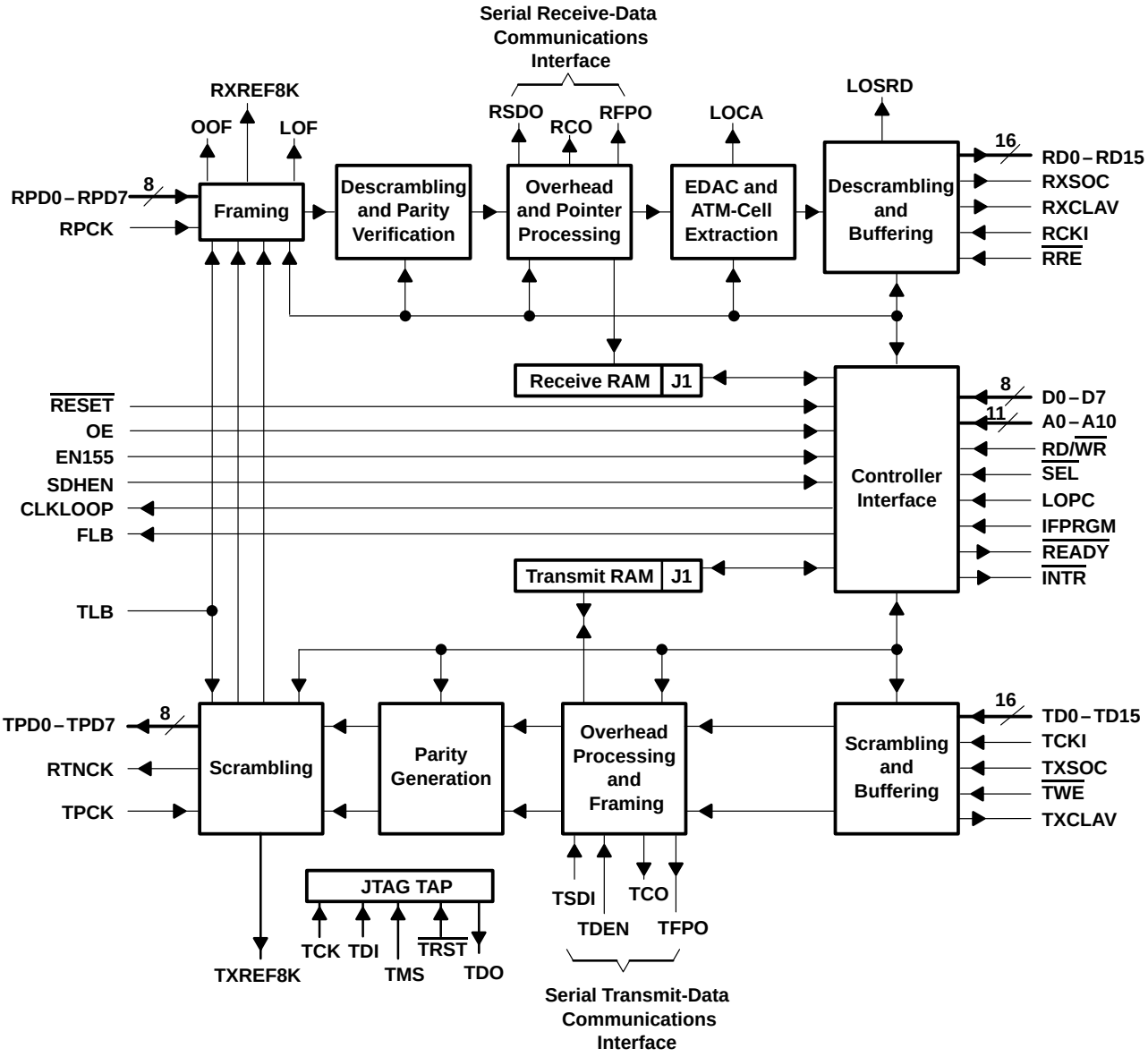
PRODUCT PREVIEW

PQFP PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

Terminal Functions

line-side parallel interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RPD0–RPD7		I	Receive parallel data. This byte-wide data is clocked into the TNETA1600 on low-to-high transitions of RPCK. Bit 7 is the most-significant bit.
RPCK		I	Receive parallel clock. Data on RPD0–RPD7 is clocked into the TNETA1600 on low-to-high transitions of RPCK. The frequency of RPCK is nominally 77.76 MHz for 622.08-Mbit/s operation or 19.44 MHz for 155.52-Mbit/s operation.
TPCK		I	Transmit-parallel clock. Data is clocked out of the TNETA1600 on TPD0–TPD7 on low-to-high transitions of TPCK. The frequency of TPCK is 77.76 MHz for 622.08-Mbit/s operation or 19.44 MHz for 155.52-Mbit/s operation.
TPD0–TPD7		O	Transmit-parallel data. This byte-wide data is clocked out of the TNETA1600 on low-to-high transitions of TPCK and is accompanied by a return clock (RTNCK). TPD0–TPD7 is valid on low-to-high transitions of RTNCK. Bit 7 is the most-significant bit.
RTNCK		O	Return clock. RTNCK is a retimed version of TPCK that accompanies data output on TPD0–TPD7. TPD0–TPD7 is valid on the rising edge of RTNCK.

alarm indicators

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LOCA		O	Loss-of-cell alignment. LOCA goes high when seven consecutive ATM cell slots occur with a mismatch between the calculated header-error check (HEC) byte and the fifth byte of the ATM header, indicating invalid ATM headers. LOCA goes low when valid ATM headers are detected in seven consecutive cell slots.
LOF		O	Loss of frame. LOF goes high when an out-of-frame (OOF) condition persists for 3 ms. LOF goes low when the OOF condition is cleared for 1 ms.
LOSRD		O	Loss-of-receive data. LOSRD goes high when the receive output FIFO overflows, resulting in a loss of data. The receive output FIFO can store a maximum of three complete ATM cells. If a cell is not extracted on the receive output before additional cells arrive on the receive input, the arriving cells are discarded.
OOF		O	Out of frame. OOF goes high when four consecutive erred framing patterns are received. OOF goes low when two successive error-free framing patterns are received.

Terminal Functions (Continued)

control signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN155		I	155.52-Mbit/s enable. When EN155 is high, data operations at 155.52 Mbit/s are enabled for both the receiver and transmitter. In 155.52-Mbit/s mode, both the transmit- and receive-cell interfaces are byte wide such that data are transmitted and received on TD0–TD7 and RD0–RD7, respectively. TD8–TD15 and RD8–RD15 are not used. When EN155 is low, operations at 622.08 Mbit/s are enabled and all 16 bits of the transmit-cell and receive-cell interfaces are utilized. Changing the mode between 155.52 Mbit/s and 622.08 Mbit/s during normal operation may result in the loss of data.
OE		I	Output enable. When OE is low, all outputs on the TNETA1600 go into the high-impedance state. This feature facilitates board-level testing.
$\overline{\text{RESET}}$		I	Device reset. When $\overline{\text{RESET}}$ goes low, the device is reset. This reset causes the receive side to restart the frame search and forces OOF, LOF, and LOCA high. The reset also flushes any ATM cells stored in the input and output FIFOs and causes the transmit side to begin building SONET frames from the A1 byte. A valid clock must be present on TPCK when $\overline{\text{RESET}}$ transitions from low to high because this transition starts the initialization of the transmit-overhead RAM.
SDHEN		I	SDH enable. When SDHEN is high, frames are transmitted with SDH overhead. SDHEN is logically ORed with a bit in the control register such that both the bit and SDHEN must be low to transmit frames with SONET overhead. A change in the logically ORed combination of SDHEN and the associated control bit causes the transmit-RAM overhead to be overwritten with new SONET or SDH values, depending on the logically ORed combination of SDHEN and the control bit as previously described. Because the overhead is altered, this could result in the loss of data being processed in the transmitter.
TLB		I	Terminal loopback. TLB is logically ORed with a bit in the control register. If either or both are high, the data received at the transmit-cell interface flows normally through the transmit path to the scrambling function, where it is passed to the receive-framing function. The data is then processed through the receive path and output on RD0–RD15. Data being received on RPD0–RPD7 is blocked. However, transmit operation is not affected and output data is available on TPD0–TPD7.

receive-cell interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCKI		I	Receive clock input. Output data is valid on the receive-cell interface on positive transitions of RCKI when $\overline{\text{RRE}}$ is low.
RD0–RD15		O	Receive output data. When EN155 is low (622.08-Mbit/s operation), ATM cell data is clocked out of the TNETA1600 through RD0–RD15 on positive transitions of RCKI, beginning with the first two bytes of the ATM header. When EN155 is high (155.52-Mbit/s operation), cells are clocked out on RD0–RD7 (RD8–RD15 are not used). RD0 is the least-significant bit.
$\overline{\text{RRE}}$		I	Receive read enable. A low level on $\overline{\text{RRE}}$ enables the reading of data from the receive-cell interface.
RXSOC		O	Receive start of ATM-cell indicator. RXSOC goes high identifying the first byte (or first two bytes in 622.08-Mbit/s operation) of an ATM cell on the receive-cell interface. RXSOC is low during the remainder of that cell's output.
RXCLAV		O	Receive-cell available. RXCLAV goes high denoting that the receive output FIFO is capable of transferring a complete ATM cell. RXCLAV goes low when the receive output FIFO is empty and the current output data on RD0–RD15 is invalid.

PRODUCT PREVIEW

Terminal Functions (Continued)

transmit-cell interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCKI		I	Transmit clock input. Input signals are clocked into the transmit-cell interface and output signals are valid at the transmit-cell interface on positive transitions of TCKI, when $\overline{\text{TWE}}$ is low.
TD0–TD15		I	Transmit input data. When EN155 is low (622.08-Mbit/s operation), ATM cells are clocked into the TNETA1600 through TD0–TD15 on positive transitions of TCKI, provided $\overline{\text{TWE}}$ is low. If EN155 is high and $\overline{\text{TWE}}$ is low (155.52-Mbit/s operation), cells are clocked in on TD0–TD7 (TD8–TD15 are not used). TD0 is the least-significant bit.
$\overline{\text{TWE}}$		I	Transmit write enable. A low level on $\overline{\text{TWE}}$ enables the writing of ATM cells into the transmit-cell interface.
TXCLAV		O	Transmit-cell available. TXCLAV goes high when the transmit input FIFO is capable of accepting the transfer of a complete ATM cell. TXCLAV goes low when the TNETA1600 can accept only four more write cycles (four bytes during 155.52-Mbit/s operation or eight bytes during 622.08-Mbit/s operation) from the ATM-layer device without overflowing the transmit input FIFO.
TXSOC		I	Transmit start-of-cell indicator. A high level on TXSOC identifies the first byte (or first two bytes in 622.08-Mbit/s operation) of an incoming ATM cell on the transmit-cell interface. TXSOC is held low during the remainder of that cell's input. Once a valid TXSOC indication is detected, subsequent TXSOC indications are ignored until the full 53 bytes of an ATM cell are received.

controller interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A0–A10		I	Address lines. A0–A10 provide the address for accessing the internal registers and RAM. A10 is the most-significant bit.
D0–D7		I/O	Data I/O. D0–D7 provides access to the contents of the device's internal registers and RAM. D7 is the most-significant bit.
$\overline{\text{INTR}}$		O	Interrupt (open drain). $\overline{\text{INTR}}$ goes low to indicate that an unmasked condition has occurred.
RD/$\overline{\text{WR}}$		I	Read/write control. A high-level input on RD/$\overline{\text{WR}}$ indicates a read operation and a low-level input indicates a write operation.
$\overline{\text{READY}}$		O	Ready. $\overline{\text{READY}}$ goes low to indicate that the device is ready to complete the requested transaction.
$\overline{\text{SEL}}$		I	Device select. A low-level input on $\overline{\text{SEL}}$ enables the access of the device's internal registers and RAM.
IFPRGM		I	Interface program mode. IFPRGM is logically ORed with a bit (place TX O/H RAM in program mode) in the control register. If either or both are high, the automatic write operations to transmit overhead by the TNETA1600 are disabled. During this condition, overhead values can be written into the TNETA1600 via the controller interface. Since these values are not automatically overwritten, the user is given the capability to transmit any value in any overhead-byte location. Overhead RAM addresses, which are not written to, retain their values. While in the program mode, the transmit data-communications port is disabled (TFPO is held low). When both IFPRGM and the associated control bit are low, specified overhead bytes are automatically overwritten each frame after the first row's overhead has been transmitted.
LOPC		I	Loss of optical carrier. When LOPC goes high, a bit is set in the status register, and if not masked, an interrupt is generated on $\overline{\text{INTR}}$. This provides an interrupt through the controller interface to the host indicating that the incoming optical signal has been lost. When LOPC goes low, the bit in the status register goes low and an interrupt is (again) generated on $\overline{\text{INTR}}$.
CLKLOOP		O	Clock loopback. CLKLOOP is at a high level when the corresponding bit in the control register is at a high level. Similarly, if the control register bit is low, CLKLOOP is low. This allows a clock-loopback function on a line-side device (i.e., a TNETA1510, TNETA1610, or TNETA1611) to be controlled through the controller interface of the TNETA1600.
FLB		O	Facility loopback. FLB is at a high level when the corresponding bit in the control register is at a high level. Similarly, if the control register bit is low, FLB is low. This allows a facility-loopback function on a line-side device (i.e., a TNETA1510, TNETA1610, or TNETA1611) to be controlled through the controller interface of the TNETA1600.

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Terminal Functions (Continued)

serial-receive data-communications interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RSDO		O	Receive serial-data output. The 14 data-communications and orderwire bytes are output serially on RSDO in the following order: E1, D1 – D12, and E2. The most-significant bit (MSB) of each byte is sent out first. Data is valid on the rising edge of RCO. RFPO goes high to identify the concurrent output of the first bit (MSB) of E1. The remaining seven bits of E1 and the 13 other data-communications and orderwire bytes are then shifted out on consecutive clock cycles.
RCO		O	Receive clock output. RSDO and RFPO are valid on the rising edge of RCO. RCO is a continuous clock with a frequency of 1.215 MHz. Once the first A1 byte of a frame is received, all 14 orderwire and data-communications bytes from the previous frame are serially transmitted in a burst, such that traffic is not always present on the interface.
RFPO		O	Receive framing-pulse output. RFPO identifies the presence of the first output bit (MSB) of the E1 byte. When a high signal is clocked out on RFPO, the MSB of E1 is simultaneously clocked out on RSDO.

serial-transmit data-communications interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TSDI		I	Transmit serial-data input. When TDEN is high at the time that the first bit of a given byte is to be input, all eight bits of that byte are input serially on TSDI. Bytes are read in the following order: E1, D1 – D12, and E2. The MSB of each byte is input first. Data is clocked into the device on the rising edge of TCO. TFPO goes high to identify the subsequent input of the first bit (MSB) of E1. The remaining seven bits of E1 and the 13 other data-communications and orderwire bytes are then input on consecutive clock cycles, provided TDEN is high for the MSB of each byte.
TDEN		I	Transmit data-communications enable. If TDEN is low when the MSB of a given byte is to be input, the TNETA1600 does not read that byte on TSDI. If TDEN is high when the MSB of a given byte is to be input, all eight bits of that byte are read on contiguous clock cycles. TDEN is examined for the MSB of E1 on the first rising edge of TCO, following the rising edge that clocks out a high signal on TFPO.
TCO		O	Transmit clock output. TSDI is clocked in and TFPO is valid on the rising edge of TCO. TCO is a continuous 1.215-MHz clock signal. However, the data is input in a burst, such that traffic is not always present on the interface.
TFPO		O	Transmit framing-pulse output. TFPO identifies the subsequent input of the first bit (MSB) of the E1 byte. When a high signal is clocked out on TFPO, the MSB of E1 is clocked in on the next rising edge of TCO, provided TDEN is high. TFPO is valid on the rising edge of TCO.

Terminal Functions (Continued)

JTAG test access port

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCK		I	Test clock. TCK is one of four terminals required by IEEE Standard 1149.1. TCK samples data on TDI, outputs data on TDO, and clocks the test-access-port (TAP) controller. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK.
TDI		I	Test-data input. TDI is one of four terminals required by IEEE Standard 1149.1. TDI is the serial input for shifting information into the instruction register or selected data register. TDI is captured on the rising edge of TCK.
TDO		O	Test-data output. TDO is one of four terminals required by IEEE standard 1149.1. TDO is the serial output for shifting information out of the instruction register or selected data register. TDO is updated on the falling edge of TCK.
TMS		I	Test-mode select. TMS is one of four terminals required by IEEE Standard 11.49.1. TMS directs the TAP controller through its states. TMS is captured on the rising edge of TCK.
$\overline{\text{TRST}}$		I	Test reset. $\overline{\text{TRST}}$ is the active-low input that implements the optional reset terminal of IEEE Standard 1149.1. When asserted (low), $\overline{\text{TRST}}$ causes the TAP controller to asynchronously enter the test-logic-reset state and configure the instruction register and test data registers to their default values. A high-level on $\overline{\text{TRST}}$ allows normal TAP controller operation. $\overline{\text{TRST}}$ should be held low during device power up.

miscellaneous signals†

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND			Ground. GND1 is the 0-V reference for TTL circuits.
V_{CC}			Supply voltage. V_{CC1} is the 5 V ±5% supply for the TTL circuits.
RXREF8K		O	Receive-side 8-kHz reference. Pulse duration is approximately 450 ns.
TXREF8K		O	Transmit-side 8-kHz reference. Pulse duration is approximately 450 ns.
NC			No connection. These terminals are left open.
TEST0†		I	Test mode 0. TEST0 activates the short-frame test mode.
TEST1†		I	Test mode 1. TEST1 disables the TX SONET scrambler.
TEST2†		I	Test mode 2. TEST2 disables the RX SONET descrambler.
TEST3†		I	Test mode 3. TEST3 disables the TX ATM cell scrambler.
TEST4†		I	Test mode 4. TEST4 disables the RX ATM cell descrambler.
TEST5†		I	Test mode 5. TEST5 activates the UTOPIA loopback mode.

† All test mode inputs are mirrored by bits in the control registers. A logical OR function provides the resulting control signal. For example, the TX SONET scrambler is disabled when a high-level signal is applied to TEST1 terminal or when the associated control register bit is set high for the TX SONET scrambler.

PRODUCT PREVIEW

detailed description

transmit operation

The TNETA1600 operates at either 155.52 Mbit/s or 622.08 Mbit/s. The choice of operation is made through the EN155 input. When the device is programmed to operate at 155.52 Mbit/s, the device transmits a STS-3c/STM-1 frame. When the device is programmed to operate at 622.08 Mbit/s, the device transmits a STS-12c/STM-4c frame. Both the STS-3c/STM-1 and STS-12c/STM-4c outputs are byte wide.

transmit-cell interface

The transmit-cell interface consists of an 8-/16-bit-wide input data (TD0-TD15), input clock (TCKI), start of ATM cell input (TXSOC), transmit write-enable input ($\overline{\text{TWE}}$), and transmit cell-available output (TXCLAV). Input data is clocked into the TNETA1600 on low-to-high transitions of TCKI when $\overline{\text{TWE}}$ is low. TXCLAV goes active when the transmit input FIFO is capable of accepting the transfer of a complete ATM cell. TXCLAV goes inactive when the transmit input FIFO is within four write cycles (four bytes during 155.52-Mbit/s operation or eight bytes during 622.08-Mbit/s operation) of being full. The FIFO holds three complete ATM cells. The reception of a high signal on TXSOC indicates the first byte (or first two bytes in a 16-bit cell interface) of an ATM cell. Once the input FIFO receives a high TXSOC signal indicating the start of an ATM cell, the interface ignores subsequent TXSOC indications until each byte of the incoming ATM cell is received. Receiving a TXSOC indication in the middle of a cell does not reset the input-byte counters and the device groups the first 53 bytes (54 bytes for 622-Mbit/s operation) received after the initial TXSOC indication into a single ATM cell. The transmit-cell interface is fully synchronous. All signals associated with the interface are either sampled or valid on the rising edge of TCKI. The design goal for the interface is to operate at frequencies up to 50 MHz over worst-case supply voltage, process control, and temperature. The data input on the transmit-cell interface is 16 bits wide for 622.08-Mbit/s operation and 8 bits wide for 155.52-Mbit/s operation. The width of the datapath is set when the user chooses either 155.52-Mbit/s or 622.08-Mbit/s operation through the EN155 input. For the 16-bit data input, the device can be configured to accept data in two different input formats. For the first format, data is input as 54 bytes per ATM cell with two user-defined bytes (UDBs) separating the four bytes of the ATM header from the cell payload. The second format has one UDB separating the four bytes of the ATM header from the cell payload and a second UDB at the end of the cell payload. These two formats are illustrated in Figure 1. In each format, the second UBD is discarded so that the 53-byte ATM cell can be mapped into a SONET/SDH frame. The selection of the data format is made via the control register, which is accessible through the controller interface. When a hardware or software reset occurs, the device is set to accept format 1. For the 8-bit data interface, data is input as a 53-byte ATM cell with one UDB separating the four bytes of the ATM header from the 48-byte cell payload.

FORMAT NO. 1

MSB BITS 15	LSB BIT 0
Header Byte No. 1	Header Byte No. 2
Header Byte No. 3	Header Byte No. 4
UDB No. 1	UDB No. 2
Payload Byte No. 1	Payload Byte No. 2
:	:
:	:
Payload Byte No. 47	Payload Byte No. 48

FORMAT NO. 2

MSB BIT 15	LSB BIT 0
Header Byte No. 1	Header Byte No. 2
Header Byte No. 3	Header Byte No. 4
UDB No. 1	Payload Byte No. 1
Payload Byte No. 2	Payload Byte No. 3
:	:
:	:
Payload Byte No. 48	UDB No. 2

Figure 1. Transmit-Cell Interface Formats for 16-Bit Input Data

PRODUCT PREVIEW

transmit-cell interface (continued)

The 48-byte information field of the ATM cell is scrambled using a self-synchronizing scrambler polynomial of $x^{43} + 1$ to improve the efficiency of the cell-delineation procedure. At startup, the scrambler is initialized to an all-ones state. The 5-byte ATM header is not scrambled. TXSOC identifies the first byte of the ATM cell and disables the scrambler. The input data is stored in the transmit input FIFO and multiplexer into the SONET payload after all 53 bytes of the ATM cell are received. If the FIFO does not contain 53 bytes of information at the start of a cell-insertion cycle, an idle or unassigned cell is sent depending upon the configuration of the control register. An idle cell is defined as an ATM cell with the 5-byte header set to 00 00 00 01 52 (hex) and all 48 bytes of the payload set to a hex value of 6A. An unassigned cell is defined as an ATM cell with the 5-byte header set to 00 00 00 00 55 (hex) and all 48 bytes of the payload set to a hex value of 6A.

The transmit section is initialized on reset to calculate the header-error-check (HEC) byte in the ATM header. When this feature is active, the fifth byte of the ATM cell that is input through the transmit-cell interface is ignored. The HEC byte is calculated in accordance with the appropriate ANSI, CCITT, and ATM Forum specifications and placed in the fifth byte of the ATM cell. This feature can be disabled for test purposes by setting a bit in the control register.

transmit overhead

The transmit operation can be controlled to send either a SONET frame or an SDH frame. When both SDHEN and the enable SDH frames bit in the control register are low, a SONET frame is transmitted. When either SDHEN or the enable SDH frames bit (or both) are high, an SDH frame is transmitted. A valid clock must be present at TPCK when the framing mode is changed, as this clock is used to change the overhead-RAM contents. Because overhead contents are altered, toggling the mode during operation can result in the loss of transmit-frame alignment and loss of any data being processed in the TNETA1600 transmitter. A hardware or software reset also causes the overhead RAM to be rewritten with SONET or SDH values, depending on the status of SDHEN.

For both SONET and SDH transmitted frames, the location of the J1 byte in the path overhead is fixed. The J1 byte always comes after the last C1 byte of the transport overhead. This results in a fixed value for the first H1 byte of 0110 0010 for SONET frames or 0110 1010 for SDH frames. The first H2 byte has a fixed value of 0000 1010 (10 0000 1010 binary is equal to 522 decimal) for both SONET and SDH frames. The H3 bytes are set to zero. The transport- and path-overhead bytes are multiplexed into the output-byte stream from the transmit-overhead RAM. All transmit-overhead bytes with values that must be calculated by the TNETA1600 are placed in the transmit-overhead RAM prior to being added to the output data stream. The user has access to the transmit-overhead RAM through the controller interface and can preset the values of many overhead bytes. The user can also insert the D1–D12, E1, and E2 bytes into the transmit-data stream through the serial transmit data-communications port.

The values of the transmit-overhead bytes are initialized at reset or upon a framing-mode change (SONET/SDH) to the values given in Table 1. Overhead bytes not shown in the table are initialized to all zeroes (0000 0000). Although the user can program the value of any overhead byte by writing to the transmit-overhead RAM, several of the values will be automatically overwritten by the TNETA1600. This overwrite occurs after the first row's overhead is transmitted (e.g., after J1 at 155.52 Mbit/s). Table 1 denotes the bytes to which this applies. For example, the B2-byte values are calculated by the TNETA1600 and written into RAM regardless of whether or not a value was written to B2 via the controller interface. These automatic write operations by the TNETA1600 are disabled when the transmit-overhead RAM is placed in program mode (accomplished by setting a bit in the control register or by taking the interface programming mode (IFPRGM) input high). While in the program mode, overhead values can be written into the TNETA1600 via the controller interface. Since no values are automatically overwritten, this gives the user the capability to transmit any value in any overhead-byte location. Specified bytes are automatically overwritten when the program mode is exited.

Table 1. Transmit Overhead

OVERHEAD BYTE	SONET-FRAME VALUE INITIALIZED AT RESET OR FRAME-MODE CHANGE	SDH-FRAME VALUE INITIALIZED AT RESET OR FRAME-MODE CHANGE	VALUE OVER-WRITTEN EACH FRAME?
A1	1111 0110 (F6 hex)	1111 0110 (F6 hex)	Y
A2	0010 1000 (28 hex)	0010 1000 (28 hex)	Y
C1/1	0000 0001	0000 0001	N
C1/2	0000 0010	0000 0010 (0000 0000 for 155.52-Mbit/s mode)	N
C1/3	0000 0011	0000 0011 (0000 0000 for 155.52-Mbit/s mode)	N
C1/4†	0000 0100	0000 0000	N
C1/5†	0000 0101	0000 0000	N
C1/6†	0000 0110	0000 0000	N
C1/7†	0000 0111	0000 0000	N
C1/8†	0000 1000	0000 0000	N
C1/9†	0000 1001	0000 0000	N
C1/10†	0000 1010	0000 0000	N
C1/11†	0000 1011	0000 0000	N
C1/12†	0000 1100	0000 0000	N
B1	Calculated from previous frame	Calculated from previous frame	Y
E1	0111 1111	0111 1111	N
F1	0000 0000	0000 0000	N
D1–D3	0111 1111	0111 1111	N
First H1	Normal operation: 0110 0010 Path AIS: 1111 1111‡	Normal operation: 0110 1010 Path AIS: 1111 1111‡	Y
H1	Normal operation: 1001 0011 Path AIS: 1111 1111‡	Normal operation: 1001 1011 Path AIS: 1111 1111‡	N
First H2	Normal operation: 0000 1010 Path AIS: 1111 1111‡	Normal operation: 0000 1010 Path AIS: 1111 1111‡	Y
H2	Normal operation: 1111 1111 Path AIS: 1111 1111‡	Normal operation: 1111 1111 Path AIS: 1111 1111‡	N
H3	Normal operation: 0000 0000 Path AIS: 1111 1111‡	Normal operation: 0000 0000 Path AIS: 1111 1111‡	N
B2	Calculated from previous frame	Calculated from previous frame	Y
K1	0000 0000	0000 0000	N
First K2	Normal operation: 0000 0000 Line AIS: 1111 1111 Line FERF: 0000 0110	Normal operation: 0000 0000 Line AIS: 1111 1111 Line FERF: 0000 0110	Bits 1–5: N Bits 6–8: Y§
D4–D12	0111 1111	0111 1111	N
Z1/1–Z1/3	0000 0000	0000 0000	N
Z1/4–Z1/12†	0000 0000	0000 0000	N
Third Z2	B2 error count; range of legal values for Z2 is: 0000 0000 – 0110 0000	B2 error count; range of legal values for Z2 is: 0000 0000 – 0110 0000	Y
E2	0111 1111	0111 1111	N

† These bytes are used only in 622.08-Mbit/s applications.

‡ For the transmission of a line AIS or path AIS, an all-ones pattern is put in the data stream in place of certain overhead bytes. The all-ones pattern is not, however, written to or reflected in the transmit-overhead RAM. Upon deactivation of the AIS condition, the original values (still in the RAM) are returned to the data stream.

§ For the transmission of a line FERF, a 110 is put in the data stream in place of bits 6–8 of the K2 byte. These values are not, however, written to or reflected in the transmit-overhead RAM. Upon deactivation of the line FERF condition, the original values (still in the RAM) are returned to the data stream.

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Table 1. Transmit Overhead (Continued)

OVERHEAD BYTE	SONET-FRAME VALUE INITIALIZED AT RESET OR FRAME-MODE CHANGE	SDH-FRAME VALUE INITIALIZED AT RESET OR FRAME-MODE CHANGE	VALUE OVER WRITTEN EACH FRAME?
J1 (64 bytes)	Default value: 0000 0000 J1 can be modified via controller interface.	Default value: 0000 0000 J1 can be modified via controller interface.	N
B3	Calculated from previous SPE	Calculated from previous SPE	Y
C2	0001 0011	0001 0011	Y
G1 bits 1–4 G1 bits 5–6 G1 bits 7–8	B3 error count (0000 – 1000); Path FERF: 1001 PRDI: 01 PLM; 10 PAIS, LOP, LOCA; 11 UNEQ 00	B3 error count (0000 – 1000); Path FERF: 1001 PRDI: 01 PLM; 10 PAIS, LOP, LOCA; 11 UNEQ 00	Y

Calculation of parity bytes B1, B2 (twelve bytes), and B3 are as follows:

- **B1.** B1 is a bit-interleaved parity 8 (BIP-8) code using even parity. B1 is calculated over all bits of the previous frame after scrambling. The calculated value of B1 is placed in the frame before the frame is scrambled.
- **B2.** For an STS-12c frame, the twelve B2 bytes combine to form a BIP-96 code. For an STS-3c frame, the three B2 bytes form a BIP-24 code. However, each B2 byte is calculated as if the frame is composed of individual STS-1s. Each B2 is calculated, using even parity, over all bits of the line overhead and STS-1 envelope capacity of the previous STS-1 frame before scrambling. The computed value is placed in the appropriate B2-byte location before scrambling. The line overhead consists of the six rows of transport-overhead bytes beginning with the first H1 byte and ending before the row containing the first A1 byte.
- **B3.** The B3 byte is calculated over all bits of the previous SPE before scrambling. B3 is a BIP-8 code using even parity. The computed value is placed in the B3 location prior to scrambling.

The TNETA1600 transmits path and line far-end block-error (path FEBEs and line FEBEs) counts via the transmit G1 and third Z2 bytes. The transmit G1-byte (bits 1–4) contains the number of B3 errors detected in the incoming (receive) frame. The third Z2-byte (bits 2–8) contains the number of B2 errors detected in the incoming (receive) frame.

The TNETA1600 transmits a line far-end receive-failure (LFERF)† indication via the K2 byte when a receive loss-of-frame (LOF), loss-of-signal (LOS), or line-alarm indication signal (LAIS) is detected. An LFERF is indicated by setting bits 6–8 of the transmit K2 byte to 110. The TNETA1600 also transmits a path FERF (PFERF)† indication if a receive LOF, LOS, LAIS, loss-of-pointer (LOP), or path-alarm indication signal (PAIS) is detected. A path FERF is indicated by setting bits 1–4 of the transmit G1-byte to 1001. A path remote-defect indication (PRDI)† is transmitted if a payload-label mismatch (PLM), PAIS, loss-of-pointer (LOP), or path-unequipped (UNEQ) defect is detected. PRDI is also transmitted if the amount of time that a loss-of-cell alignment (LOCA) condition persists exceeds the value of the LOCA soak counter, provided that the soak counter is enabled via the control register. A PRDI is indicated by setting bits 5 and 6 of the transmit G1 byte as shown below.

G1 BIT 5	G1 BIT 6	DEFECT
0	0	None
0	1	PLM
1	0	PAIS, LOP, LOCA soak
1	1	UNEQ

† LFERF, PFERF, and PRDI conditions can also be forced by setting bits in the control register. For example, LFERF is transmitted if the force-transmit-line FERF bit in control register 2 (address 008 hex) is set to a one, or if LOS, LOF, or LAIS is detected, as described previously.

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transmit overhead (continued)

In addition, the TNETA1600 can be programmed to transmit a LAIS or a PAIS by writing to specified bits in the control registers. A LAIS is generated by the TNETA1600 as a valid SOH and a scrambled all-ones pattern for the remainder of the signal. During a PAIS condition, the synchronous payload envelope (SPE) as well as the H1, H2, and H3 pointer bytes are set to all ones before scrambling. When either the LAIS or PAIS condition is transmitted, ATM cells loaded into the transmit-input FIFO are not inserted into the outgoing frame. This causes the input FIFO to fill up once three ATM cells are input and the device does not accept additional ATM cells until the device returns to normal operating mode. At that point, the device begins inserting ATM cells into the outgoing frame. During a PAIS condition, all transport-overhead bytes (except H1, H2, and H3) in the outgoing frame are calculated and inserted normally. Since the pointer bytes are set to all ones, the receiving station is not able to locate the SPE and path-overhead bytes.

The TNETA1600 provides a serial-transmit data-communications port that allows data-communications and orderwire bytes to be inserted into the outgoing transport overhead. The transmit data-communications interface consists of a data-communication enable (TDEN) input, a serial data input (TSDI), a serial clock output (TCO), and a framing pulse output (TFPO). TCO is a continuous clock signal that clocks out the framing pulse and clocks in the serial data. The framing pulse is valid on the rising edge of TCO and is used to identify the subsequent input of the most significant bit of the E1 byte. If TDEN is low when the MSB of a byte is to be input, that byte is not read into the data-communications interface. If TDEN is high when the MSB of a given byte is to be input, all eight bits of that byte are read into the transmit data-communications interface (on TSDI) on contiguous clock cycles, MSB first. Bytes are read into the interface in the following order: E1, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, E2. Provided TDEN is high, the MSB of the E1 byte is clocked into the device on the first rising edge of TCO, immediately following the rising-clock edge that clocks out the framing pulse. TCO has a frequency of 1.215 MHz. However, traffic is present on the data-communications interface only about 75% of the time as there are only 14 bytes (plus the framing pulse) to process each frame (125 μs), and all 14 bytes are read contiguously once TFPO is clocked out high. Orderwire- and data-communications bytes that are input through the data-communications interface are written into the TNETA1600 internal RAM. The values are then used in the overhead of subsequent frames, provided they are not overwritten through the controller interface or by subsequent input through the data-communications port.

The TNETA1600 provides an 8-kHz reference output (TXREF8K) that is derived from the transmit-side incoming clock signal. TXREF8K is a pulse that goes high during the period when the SONET scrambler is disabled for the A1, A2, and C1 bytes. TXREF8K is low for the remainder of the frame. The pulse duration for this signal is approximately 450 ns.

Prior to transmission, the output frame is scrambled using a generating polynomial of $x^7 + x^6 + 1$. The A1, A2, and C1 overhead bytes are not scrambled and the scrambler is reset to 11111111 on the MSB of the byte immediately following the last C1 byte. The scrambler runs continuously throughout the remainder of the frame.

The byte-wide data is output from the TNETA1600 upon detection of the rising edge of TPCK. The data is accompanied by a return clock (RTNCK) such that the data is valid on the rising edge of RTNCK. This interface runs at 19.44 MHz for 155.52-Mbit/s operation and 77.76 MHz for 622.08-Mbits/s operation. TPCK provides the clock signal for the entire transmit-side operation, except for the transmit-cell-interface clock, which uses TCKI.

A terminal-loopback (TLB) feature is also provided on the TNETA1600. When the TLB bit in the control register is set (or when TLB goes high), the ATM cells received on the transmit input flow normally through the transmit path to the scrambling function where they are passed to the framing function in the receiver. The cells are then processed through the receive path and output on RD0–RD15. Data received on RPD0–RPD7 is blocked. However, the transmit operation is not affected in this mode and data is output on TPD0–TPD7 as well as being passed to the receive path.

receive operation

The TNETA1600 receive section accepts a byte-wide data input (RPD0–RPD7) and a byte clock (RPCK) input operating at 77.76 MHz for 622.08-Mbit/s operation or 19.44 MHz for 155.52-Mbit/s operation. The input to the TNETA1600 must be aligned on correct byte boundaries before it is passed to the device. For example, all eight bits of a given A1 byte must be simultaneously received on RPD0–RPD7. The TNETA1600 does not perform a bit search to establish byte boundaries. Upon receiving the byte-wide input, a framing circuit searches for the correct sequence of SONET/SDH framing bytes A1 and A2, where A1 has a value of F6 hex and A2 has a value of 28 hex. The exact framing pattern for a 622.08-Mbit/s signal is twelve A1 bytes followed by twelve A2 bytes. The framing pattern for a 155.52-Mbit/s signal is three A1 bytes followed by three A2 bytes.

The TNETA1600 provides loss-of-signal (LOS), out-of-frame (OOF), and loss-of-frame (LOF) alarms through the controller interface in accordance with BellCore Specification GR-253-CORE, Issue 1, December 1994. The LOS alarm goes active when no transitions are detected in the receive data for 3.2-μs time period. The LOS alarm goes inactive when two consecutive framing patterns are detected and, during the intervening time (one frame), a lack of signal transitions for a 3.2-μs time period is not detected. The OOF alarm goes active when four consecutive erred framing patterns are received. The OOF alarm clears when two valid framing patterns are received consecutively. If the OOF condition fails to clear within 3 ms, the LOF alarm goes active. The LOF alarm goes inactive 1 ms after the OOF alarm clears, provided another OOF condition is not detected in that 1-ms time period. In addition to bits in the status registers, the OOF and LOF alarms are also represented by the external pins. Setting unmasked bits in the status registers causes the $\overline{\text{INTR}}$ output of the controller interface to go active to signal an interrupt.

The TNETA1600 provides an 8-kHz reference output (RXREF8K) that is derived from the receive-side incoming clock signal. RXREF8K is a pulse that goes high during the period when the SONET descrambler is disabled for the A1, A2, and C1 bytes. RXREF8K is low for the remainder of the frame. The pulse duration for the signal is approximately 450 ns. RXREF8K is disabled (remains low) when an OOF condition is present (i.e., OOF is high).

After the SONET/SDH frame is established, the B1 BIP-8 parity is calculated over the scrambled SONET frame. This value is compared with the value contained in the B1 overhead location of the next frame. If the two values do not match, the B1 parity error bit in the status register goes active, denoting that a B1 parity error has occurred. This causes the interrupt ($\overline{\text{INTR}}$) line to go active.

Next, the SONET/SDH frame is unscrambled, except for the A1, A2, and C1 bytes, which were not scrambled by the transmitter. The transport-overhead bytes are copied from the SONET/SDH frame into the receive-overhead RAM after descrambling. In addition, the data-communications and orderwire bytes are output through the receive data-communications interface. This interface consists of a serial data output (RSDO), a serial clock output (RCO), and a framing pulse output (RFPO). Orderwire and data-communications bytes in a frame are internally stored until the first A1 byte of the next frame is received, at which time all 14 bytes are continuously output in the following order: E1, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, E2. The serial-data and framing pulse are valid on the rising edge of the RCO with the MSB of each byte clocked out first and the least-significant bit (LSB) clocked out last. RFPO goes high to identify the concurrent output of the MSB (first output bit) of the E1 byte. The remaining seven bits of E1 and the other13 data-communications and orderwire bytes are then output on contiguous clock cycles. RCO is a continuous 1.215-MHz signal derived from the receive-byte clock. However, traffic is present on the interface only about 75% of the time as there are only 14 bytes to process each frame (125 μs).

The B2 BIP-96 (BIP-24 for 155.52-Mbit/s operation) value is calculated over all bits of line overhead and the envelope capacity and compared to the value contained in the next frame. If a B2 parity error occurs, the B2-parity-error bit in the status register is set and the interrupt ($\overline{\text{INTR}}$) line goes active to notify the controller that a parity error has occurred.

receive operation (continued)

The location of the J1 byte in the SPE must be determined from the H1 and H2 bytes in the transport overhead. The location of the J1 byte does not change from the previous frame unless the first four bits of H1 are set to 1001 (the new-data flag) or the pointer value contained in H1 and H2 is different for three consecutive frames. The location of J1 also can be incremented or decremented one byte slot by inverting certain bits in the H1 and H2 byte pointer. If at least three of the five bits 7, 9, 11, 13, and 15 are inverted, the location of J1 is incremented one slot. If at least three of the five bits 8, 10, 12, 14, and 16 are inverted, the location of J1 is decremented one slot. Subsequent pointers contain the new offset.

The TNETA1600 provides a loss-of-pointer (LOP) alarm in the controller interface to indicate that either an invalid pointer is detected for eight consecutive frames in the incoming H1 and H2 bytes or a new-data flag (NDF) that is set to a value of 1001 (the first four bits of H1) is found in eight consecutive frames. The LOP alarm goes inactive when a valid pointer (with the NDF set to 0110) is detected in three consecutive frames. The TNETA1600 provides a PAIS alarm in the controller interface to indicate that a path PAIS condition is detected in the H1 and H2 bytes. A PAIS condition is detected as an all ones condition in bytes H1 and H2 for three consecutive frames. The PAIS alarm goes inactive when a valid, identical pointer (with the NDF set to 0110) is detected for three consecutive frames or when a valid pointer is observed with NDF set to 1001. The LOP alarm is not set if a PAIS condition is detected. Decoding of the NDF is performed by majority voting (i.e., the NDF is detected as being set if three or four of the bits match the 1001 code).

The TNETA1600 evaluates the incoming receive transport- and path-overhead bytes for error reporting from the transmitting system. The TNETA1600 checks for a LAIS, LFERF, PFERF, and PRDI. The LAIS alarm is activated when bits 6–8 of the incoming K2 byte are set 111 for five† consecutive frames. The LAIS alarm is deactivated when bits 6–8 of K2 byte are set to any pattern other than 111 for five† consecutive frames. The LFERF alarm is activated when bits 6–8 of K2 byte are set to 110 for five† consecutive frames. The LFERF alarm is deactivated when bits 6–8 of the K2 byte are set to any pattern other than 110 for five† consecutive frames. The path FERF alarm is activated when bits 1–4 of the G1 byte are set to 1001. The path PRDI alarm is activated when bit 5 or bit 6 (or both) of the G1 byte is set to 1 for ten† consecutive frames. The PRDI alarm is deactivated when bits 5 and 6 of the G1 byte are set to 00 for ten† consecutive frames or when a PAIS defect is detected on the affected path.

The B3 BIP-8 byte is calculated over the contents of the SPE, which begins with the J1 byte. The value calculated for B3 is compared with the value found in the next frame. If a B3 parity error occurs, the B3 parity error bit is set in the status register and $\overline{\text{INTR}}$ goes active to notify the external controller.

Cumulative counts of receive B1, B2 and B3 errors are provided by counters accessible through the controller interface. Running totals of both B1, B2, and B3 block errors and coding violating are maintained. The block-error counters maintain a count of the number of frames that are received with B1, B2, and B3 errors. The coding-violation counters count the exact number of B1, B2, and B3 bit-interleaved parity (BIP) errors that occur. The TNETA1600 also provides counters that accumulate the line-far-end and path-far-end block errors reported by the incoming Z2 and G1 bytes. When any of these counters reach maximum count, a bit is set in the status registers and an interrupt is generated. These counters are all rollover counters (i.e., they roll over to zero after the maximum count occurs and an interrupt is generated).

Once the SPE is located, the TNETA1600 extracts the path-overhead bytes and stores them in the receive overhead RAM. The TNETA1600 provides for the storage of 64 consecutive J1 bytes, allowing an external device to read the last 64 bytes received in the J1 position and check for the proper path trace. The TNETA1600 checks the C2 byte to determine if signal-label mismatch has occurred. Two signal-label-mismatch conditions are monitored via the C2 byte. A path-unequipped defect is indicated when C2 = 00 (hex) for five consecutive frames, while a payload-label-mismatch defect is indicated when C2 is any value other than 00, 01, or 13 (hex) for five consecutive frames. Each defect is independently represented by a bit in the status register.

† The number of frames in which an event must occur to activate or deactivate the LAIS, LFERF, and PRDI signals is programmable for each signal, independently, via the control registers. Default values are shown in the above text but can be changed to any whole number between one and fifteen.

receive operation (continued)

Next, ATM cells are identified and extracted. Cell delineation is accomplished by computing the header error check (HEC) value for the first four bytes of the payload and comparing the calculated value with the fifth byte. If the values do not match, the process advances one byte and is repeated. This process continues until a match between the calculated value and the fifth byte occurs. Cell alignment is assumed to occur when seven consecutive matches occur on cell boundaries. Until cell alignment occurs, the loss of cell alignment (LOCA) alarm remains active. Once cell alignment is established, it is monitored constantly for a LOCA condition. A LOCA condition is declared (LOCA goes active) when seven consecutive cells occur with a mismatch between the calculated HEC and the fifth byte of the ATM header. At this point, the hunting process starts over.

The receive side provides the capability to detect multiple bit errors and correct single bit errors occurring in the 5-byte ATM header by using the HEC byte. This feature is deactivated by setting a bit in the control register. ATM cells with multiple-bit header errors are dropped after descrambling, unless a bit is set in the control register to disable the dropping of cells with uncorrectable errors. Two 16-bit counters (accessible through the controller interface) are provided to kept EDAC statistics. One counter accumulates the number of ATM cells with single bit errors. A second counter accumulates the number of ATM cells that are received with multiple bit errors. When any of the counters reach maximum count, a bit is set in the status register and an interrupt is generated. These counters are rollover counters, (i.e., they roll over to zero after the maximum count occurs and an interrupt is generated).

After the ATM cells are extracted, they are descrambled. The 48-byte payload in the ATM cell is scrambled at the transmitter using a $x^{43} + 1$ polynomial to further distinguish the payload from the header bytes and improve the efficiency of the cell-delineation algorithm. The $x^{43} + 1$ polynomial is also used to descramble the payload so that it can be sent to the next device.

The TNETA1600 provides the capability of dropping idle and unassigned cells from the receive data stream. An idle cell is defined as a cell with the 5-byte ATM header set to a value of 00 00 00 01 52 (hex) and an unassigned cell is defined as a cell with a 5-byte header of 00 00 00 00 55 (hex). In both cases, the payload is ignored. To identify and treat a received cell as an idle or unassigned cell, the header must exactly match the respective pattern shown above (i.e., all five bytes are examined). The dropping of idle and/or unassigned cells can be disabled through control register 1 (CR1) in the controller interface. A 24-bit counter is provided to count the number of idle/unassigned cells that are dropped. Another 24-bit counter is provided to count the total number of cells received that are not dropped and are placed in the receive output FIFO. When either of these counters reaches maximum count, a bit is set in the status register and an interrupt is generated. These counters are rollover counters (i.e., they roll over to zero after the maximum count occurs and an interrupt is generated).

After descrambling, the ATM cell is passed to the output buffer, which operates as a FIFO. The receive-cell interface consists of the 8-/16-bit-wide output data (RD0-RD15), receive clock input (RCKI), receive-read-enable ($\overline{\text{RRE}}$) input, receive-cell-available (RXCLAV) output, and beginning of ATM cell indicator (RXSOC) output. Output data is valid on the rising edge of RCKI when $\overline{\text{RRE}}$ is low and RXCLAV is high. The loss-of-receive-data (LOSRD) alarm goes active in the controller interface and on an external pin when the receive-output FIFO overflows. In this case, data placed into the FIFO is lost. The output FIFO holds three complete ATM cells.

The RXCLAV output goes active when the output FIFO is capable of transferring a complete ATM cell. RXCLAV goes inactive when the receive-output FIFO is empty and the data currently being output on RD0-RD15 is invalid. The receive-cell interface is fully synchronous and all signals associated with the interface are either sampled or valid on the rising edge of RCKI. The design goal for the interface is to operate at frequencies up to 50 MHz over the worst-case V_{CC}, worst-case process, and worst-case temperature.

† The number of frames in which an event must occur to activate or deactivate the LAIS, LFERF, and PRDI signals is programmable for each signal, independently, via the control registers. Default values are shown in the above text but can be changed to any whole number between one and fifteen.

receive operation (continued)

The data output on the receive-cell interface is 16 bits wide for 622.08-Mbit/s operation and 8 bits wide for 155.52-Mbit/s operation. The width of the datapath is set when the user chooses either 155.52- or 622.08-Mbit/s operation through the EN155 input. For the 16-bit data output, the TNETA1600 is configured to transfer data in two different formats. For the first format, data is output as 54 bytes per ATM cell with two user-defined bytes (UDBs) separating the four bytes of the ATM header from the cell payload. The second format has one UDB separating the four bytes of the ATM header from the cell payload and a second UDB at the end of the cell payload. These two formats are shown in Figure 2. The selection of the data format is made via the control register that is accessible through the controller interface. When a hardware or software reset occurs, the TNETA1600 is set up to output data using format no. 1. In each format, the second UDB is an all-zeroes pattern. For the 8-bit data interface, data is output as a 53-byte ATM cell with one UDB separating the four bytes of the ATM header from the 48-byte cell payload.

FORMAT NO. 1

MSB Bit 15	LSB Bit 0
Header Byte No. 1	Header Byte No. 2
Header Byte No. 3	Header Byte No. 4
UDB No. 1	UDB No. 2
Payload Byte No. 1	Payload Byte No. 2
:	:
:	:
Payload Byte No. 47	Payload Byte No. 48

FORMAT NO. 2

MSB Bit 15	LSB Bit 0
Header Byte No. 1	Header Byte No. 2
Header Byte No. 3	Header Byte No. 4
UDB No. 1	Payload Byte No. 1
Payload Byte No. 2	Payload Byte No. 3
:	:
:	:
Payload Byte No. 48	UDB No. 2

Figure 2. Receive Cell-Interface Formats for 16-Bit Output Data

When the receive side enters a LOCA state, a PRDI can be sent out the transmit side through the outgoing G1 byte. If enabled through a bit in the control registers, a PRDI is transmitted when a LOCA state is persistent for an amount of time (known as soak time) that has not yet been specified by any of the standards organizations. To provide maximum flexibility to this unspecified soak time, an 8-bit counter is provided through the controller interface that allows the user to program soak time for a PRDI alarm in increments of 125 µs. This counter is preset to a value of 4 ms when a device reset occurs.

controller interface

The controller interface provides access to the internal memory locations that contain the control registers, status registers, interrupt-mask registers, ID register, receive- and transmit-overhead registers, and performance counters. The controller interface consists of eight data (D0–D7) I/O pins, eleven address (A0–A10) input pins, a $\overline{\text{SEL}}$ input, a RD/$\overline{\text{WR}}$ input, a $\overline{\text{READY}}$ output, and an open-drain $\overline{\text{INTR}}$ output. The interface also provides an IFPRGM input that, along with a bit in the control register, can be used to place the device in the program mode. While in the program mode, transmit-overhead values (i.e., parity bytes) are not automatically updated by the TNETA1600.

Table 2 shows a memory map of the TNETA1600 controller interface, broken into the four major areas. This map is valid for both 155.52- and 622.08-Mbit/s operation.

Table 2. TNETA1600 Memory Map

MEMORY BLOCK	BEGINNING ADDRESS (HEX)
Control and status registers	000
Performance counters	100
Receive-overhead bytes	200
Transmit-overhead bytes	400

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control and status registers

The control and status registers contain the operational-state information of the TNETA1600. These registers provide the user with the ability to program the operation of the TNETA1600 and to monitor the status of the receive data stream through software. Table 3 shows the addresses of the various registers in the internal RAM.

Table 3. TNETA1600 Register Addresses

ADDRESS (HEX)	REGISTER
000	Status register no. 1
001	Status register no. 2
002	Status register no. 3
003	Status register no. 4
004	Not implemented
005	Not implemented
006	ID register
007	Control register no. 1
008	Control register no. 2
009	Control register no. 3
00A	Control register no. 4
00B	Control register no. 5
00C	Not implemented
00D	Not implemented
00E	Not implemented
00F	Not implemented
010	Interrupt-mask register no. 1
011	Interrupt-mask register no. 2
012	Interrupt-mask register no. 3
013	Interrupt-mask register no. 4
014	Not implemented
015	Not implemented
016	Line-AIS consecutive-frame count
017	Line-FERF consecutive-frame count
018	Path-RDI consecutive-frame count
019	LOCA-to-path RDI-soak count
01A – OFF	Not implemented

status registers

The status registers, located at hex addresses 000, 001, 002, and 003, contain information on the receive-data-stream condition(s) that cause the interrupt flag ($\overline{\text{INTR}}$) to become active. The coding for the status registers is given in Table 4.

Table 4. Status-Register Coding

CAUSE OF INTERRUPT	SR1 CODING (ADDRESS 000)	SR2 CODING (ADDRESS 001)	SR3 CODING (ADDRESS 002)	SR4 CODING (ADDRESS 003)
B1 parity error	xxxx xxx1	–	–	–
B2 parity error	xxxx xx1x	–	–	–
B3 parity error	xxxx x1xx	–	–	–
Loss-of-cell alignment	xxxx 1xxx	–	–	–
Loss-of-incoming signal	xxx1 xxxx	–	–	–
Out of frame	xx1x xxxx	–	–	–
Loss of frame	x1xx xxxx	–	–	–
Loss-of-optical carrier	1xxx xxxx	–	–	–
Line AIS	–	xxxx xxx1	–	–
Line FERF	–	xxxx xx1x	–	–
Loss-of-receive data	–	xxxx x1xx	–	–
Loss of pointer	–	xxxx 1xxx	–	–
Path AIS	–	xxx1 xxxx	–	–
B1 block error-counter overflow	–	xx1x xxxx	–	
B2 block error-counter overflow	–	x1xx xxxx	–	–
B3 block error-counter overflow	–	1xxx xxxx	–	–
B1 CV-counter overflow	–	–	xxxx xxx1	–
B2 CV-counter overflow	–	–	xxxx xx1x	–
B3 CV-counter overflow	–	–	xxxx x1xx	–
Path RDI	–	–	xxxx 1xxx	–
Path FERF	–	–	xxx1 xxxx	–
Line FEBE-counter overflow	–	–	xx1x xxxx	–
Path FEBE-counter overflow	–	–	x1xx xxxx	–
Output ATM-cell-counter overflow	–	–	1xxx xxxx	–
Discarded-Idle/unassigned-cell-counter overflow	–	–	–	xxxx xxx1
Single-bit-error ATM-cell-counter overflow	–	–	–	xxxx xx1x
Multiple-bit-error ATM-cell-counter overflow	–	–	–	xxxx x1xx
Payload-label mismatch	–	–	–	xxxx 1xxx
Path unequipped	–	–	–	xxx1 xxxx

The following description of the actions and various conditions causes bits to be set in the status registers, thereby causing the open-drain $\overline{\text{INTR}}$ output to go active. All of the conditions that cause a bit in the status registers to set are associated with the receive-data stream.

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B1/B2/B3 parity error, B1/B2/B3 block error-counter overflow, B1/B2/B3 CV-counter overflow

The status bits for these errors indicate that the specified error condition has occurred. The status bits in the status registers for these conditions are set when the error condition occurs and remain set until the status register is read. If a B1, B2, or B3 parity error is detected on an incoming frame, the corresponding status bit is set in the status register, the $\overline{\text{INTR}}$ output goes active, and the status bit remains set until a read of the status register occurs. Once a read of the status register occurs, the status bit for the error condition is cleared until the next error condition is detected. A software or hardware reset causes these bits to clear.

loss-of-cell alignment (LOCA)

This bit is set when the device cannot find valid ATM headers in seven consecutive cell slots. This bit is cleared when the device detects valid ATM headers in seven consecutive cell slots. A hardware or software reset causes this bit to set. When the logic in the TNETA1600 detects that the LOCA condition has cleared, the status bit in the status register is cleared. A change in the status bit causes $\overline{\text{INTR}}$ to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

loss-of-incoming signal (LOS)

This bit is set when no signal transitions are detected on the incoming data signal for 3.2 μs. LOS is cleared when the device detects two valid SONET/SDH framing patterns without an intervening period (3.2 μs or longer) without signal transitions. The LOS is set as long as the LOS condition exists. When the logic in the TNETA1600 detects that the LOS condition has cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers. A software or hardware reset causes this bit to clear.

out of frame (OOF)

This bit is set when the device cannot find a valid SONET/SDH framing pattern in four consecutive frames. OOF is cleared when the device detects a valid SONET/SDH framing pattern in two consecutive frames. A hardware or software reset causes this bit to set. This bit is set as long as the OOF condition exists. When the logic in the TNETA1600 detects that the OOF condition is cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

loss of frame (LOF)

This bit is set when an OOF condition persists for 3 ms (24 frames). LOF is cleared 1 ms after the OOF condition clears, if the OOF condition does not reappear in that 1-ms time period. A hardware or software reset causes this bit to set. This bit is set as long as the LOF condition exists. When the logic in the TNETA1600 detects that the LOF condition is cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

loss-of-optical carrier (LOPC)

This bit is set when LOPC goes high. The LOPC bit clears when LOPC goes low. This provides an interrupt through the controller interface to the host indicating that the incoming optical signal was lost. A change in the status bit in the status register for this alarm causes $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers. A hardware or software reset has no effect on the state of this bit.

line-alarm-indication signal (LAIS)

This bit is set when the LAIS activation counter reaches a programmable value (one to fifteen) representing the number of consecutive frames in which the condition occurs. The LAIS bit is cleared when the LAIS deactivation counter reaches an independently programmable value (one to fifteen) representing the number of consecutive frames occurring without the condition. The LAIS condition is detected by the counters as a 111 pattern in bits 6–8 of the K2 byte. A hardware of software reset causes this bit to clear. This bit is set as long as the LAIS condition exists. When the logic in the TNETA1600 detects that the LAIS condition has cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

line far-end receive failure (LFERF)

This bit is set when the LFERF activation counter reaches a programmable value (one to fifteen) representing the number of consecutive frames in which the condition occurs. The LFERF is cleared when the LFERF deactivation counter reaches an independently programmable value (one to fifteen) representing the number of consecutive frames occurring without the condition. The LFERF condition is detected by the counters as a 110 pattern in bits 6–8 of the K2 byte. A hardware or software reset causes this bit to clear. This bit is set as long as the LFERF condition exists. When the logic in the TNETA1600 detects that the LFERF condition has cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

loss-of-received data (LOSRD)

This bit is set when the receive output FIFO overflows. The output FIFO can store three complete ATM cells. However, if a cell is not removed from the output FIFO before a fourth cell arrives, the arriving cell is discarded. This bit is cleared when an incoming cell is not discarded due to a full FIFO. A hardware or software reset causes this bit to be cleared. This bit is set as long as the LOSRD condition exists. When the logic in the TNETA1600 detects that the LOSRD condition has cleared, the status bit in the status register is cleared. A change in the status bit causes $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

loss of pointer (LOP)

This bit is set when the device detects an invalid pointer for eight consecutive frames in the H1 and H2 bytes of the incoming frame. This bit also is set if a new-data flag (NDF) is detected in eight consecutive frames. This bit is cleared when a valid pointer with a normal NDF is detected in three consecutive frames or a PAIS condition is detected. The decoding of NDF is performed by majority voting (i.e., the NDF is detected as being set if three or four of the bits match the 1001 code). A hardware or software reset causes this bit to clear. This bit is set as long as the LOP condition exists. When the logic in the TNETA1600 detects that the LOP condition has cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any status register.

path alarm-indication signal (PAIS)

This bit is set when the device receives three consecutive frames with the H1 and H2 bytes set to all ones. This bit is cleared when the device receives three consecutive frames with a valid pointer in bytes H1 and H2 with the NDF set to 0110 or when a valid pointer is observed with NDF set to 1001. The decoding of the NDF is performed by majority voting (i.e., the NDF is detected as being set if three or four of the bits match the 1001 code). A hardware or software reset causes this bit to clear. This bit is set as long as the PAIS condition exists. When the logic in the TNETA1600 detects that the PAIS conditions has cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

path remote-defect indicator (PRDI)

This bit is set when the PRDI activation counter reaches a programmable value (one to fifteen) representing the number of consecutive frames in which the condition occurs. The bit is cleared when the PRDI deactivation counter reaches an independently programmable value (one to fifteen) representing the number of consecutive frames occurring without the condition. The PRDI condition is detected by the counters as a one in bit five or bit six (or both) of the G1 byte. A hardware or software reset causes this bit to clear. This bit is set as long as the PRDI condition exists. When the logic in the TNETA1600 detects that the PRDI condition has cleared, the status bit in the status register is cleared. A change in the status bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

path far-end receive failure (PFERF)

This bit is set when the device receives a frame with bits 1–4 of the G1 byte set to 1001. This bit is cleared when the device receives a frame with bits 1–4 of the G1 byte set to any pattern other than 1001. A hardware or software reset causes this bit to clear. This bit is set as long as the PFERF condition exists. When the logic in the TNETA1600 detects that the PFERF condition has cleared, the status bit in the status register is cleared. A change in the status bit causes $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

line FEBE-counter overflow

This status bit indicates that the line FEBE counter has rolled over because of counter overflow. The $\overline{\text{INTR}}$ output goes active and this bit is set when the counter overflows.

path FEBE-counter overflow

This status bit indicates that the path FEBE counter has rolled over because of counter overflow. The $\overline{\text{INTR}}$ output goes active and this bit is set when the counter overflows.

output ATM-cell-counter overflow

This status bit indicates that the output ATM-cell counter has rolled over because of counter overflow. The $\overline{\text{INTR}}$ output goes active and this bit is set when the counter overflows.

discarded-idle/unassigned-cell-counter overflow

This status bit indicates that the discarded-idle/unassigned-cell counter has rolled over because of counter overflow. The $\overline{\text{INTR}}$ output goes active and this bit is set when the counter overflows.

single-bit-error ATM-cell-counter overflow

This status bit indicates that the single-bit-error ATM-cell counter has rolled over because of counter overflow. The $\overline{\text{INTR}}$ output goes active and this bit is set when the counter overflows.

multiple-bit-error ATM-cell-counter overflow

This status bit indicates that the multiple-bit-error ATM-cell counter has rolled over because of counter overflow. The $\overline{\text{INTR}}$ output goes active and this bit is set when the counter overflows.

payload-label mismatch

This bit is set when a C2 byte is received that contains a value other than 00, 01, or 13 hex for five consecutive frames, provided a PAIS or LOP condition is not detected on the incoming signal. The bit is cleared when the C2 byte is received that contains 01 hex (indicating equipped nonspecific) or 13 hex (indicating mapping for ATM) for five consecutive frames or when a path-unequipped PAIS or LOP defect is detected. A hardware or software reset causes this bit to clear. This bit is set as long as the mismatch condition exists. When the logic in the TNETA1600 detects that the mismatch has cleared, the status bit in the status register is cleared. A change in the bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

path unequipped

This bit is set when the C2 byte contains a value of 00 hex in five consecutive frames, provided a PAIS or LOP is not detected on the incoming signal. The bit is cleared when the C2 byte contains any value other than 00 hex for five consecutive frames or when a PAIS or LOP is detected. A hardware or software reset causes this bit to be cleared. This bit is set as long as the condition exists. When the logic in the TNETA1600 detects that the condition has cleared, the status bit in the status register is cleared. A change in the bit causes the $\overline{\text{INTR}}$ output to go active. When the status bit makes a low-to-high transition, the $\overline{\text{INTR}}$ output goes active. The $\overline{\text{INTR}}$ output also goes active when the status bit makes a high-to-low transition. Reading the status register does not clear the status bit for this alarm. However, the $\overline{\text{INTR}}$ output goes inactive on a read of any of the status registers.

interrupt-mask registers

All of the interrupts in the status registers can be masked by setting bits in the corresponding interrupt-mask registers, which are located at hex addresses 010–013. The coding of the interrupt-mask registers is the same as the coding for the status registers. For instance, if it is desired to mask only the interrupt associated with a B2 parity error, a value of 0000 0010 is written to interrupt-mask register 1 (IMR1). To mask all the interrupts for status register 1, a value of 1111 1111 is written to interrupt-mask register 1. Table 5 shows the coding for the interrupt-mask registers.

Table 5. Interrupt-Mask-Register Coding

INTERRUPT TO BE MASKED	IMR1 CODING (ADDRESS 010)	IMR2 CODING (ADDRESS 011)	IMR3 CODING (ADDRESS 012)	IMR4 CODING (ADDRESS 013)
B1 parity error	xxxx xxx1	–	–	–
B2 parity error	xxxx xx1x	–	–	–
B3 parity error	xxxx x1xx	–	–	–
Loss-of-cell alignment	xxxx 1xxx	–	–	–
Loss-of-incoming signal	xxx1 xxxx	–	–	–
Out of frame	xx1x xxxx	–	–	–
Loss of frame	x1xx xxxx	–	–	–
Loss-of-optical carrier	1xxx xxxx	–	–	–
Line AIS	–	xxxx xxx1	–	–
Line FERF	–	xxxx xx1x	–	–
Loss-of-receive data	–	xxxx x1xx	–	–
Loss of pointer	–	xxxx 1xxx	–	–
Path AIS	–	xxx1 xxxx	–	–
B1-block error overflow	–	xx1x xxxx	–	–
B2-block error overflow	–	x1xx xxxx	–	–
B3-block error overflow	–	1xxx xxxx	–	–
B1 CV overflow	–	–	xxxx xxx1	–
B2 CV overflow	–	–	xxxx xx1x	–
B3 CV overflow	–	–	xxxx x1xx	–
Path RDI	–	–	xxxx 1xxx	–
Path FERF	–	–	xxx1 xxxx	–
Line FEBE-counter overflow	–	–	xx1x xxxx	–
Path FEBE-counter overflow	–	–	x1xx xxxx	–
Output ATM-cell-counter overflow	–	–	1xxx xxxx	–
Discarded-idle/unassigned-cell-counter overflow	–	–	–	xxxx xxx1
Single-bit-error ATM-cell-counter overflow	–	–	–	xxxx xx1x
Multiple-bit-error ATM-cell-counter overflow	–	–	–	xxxx x1xx
Payload label mismatch	–	–	–	xxxx 1xxx
Path unequipped	–	–	–	xxx1 xxxx

control registers

The control registers are located at addresses 007 to 00B (hex). The control registers provide a means of controlling the operation of the device through the controller interface. A reset operation, initiated either by taking $\overline{\text{RESET}}$ active (low) or by performing a write operation to the ID register, clears the control registers. The bit definitions for the control registers are shown in Table 6. Several of the modes shown are test modes. These modes may not be suitable for normal use of the device as they may enable or disable receive and/or transmit functions of the device.

Table 6. Coding for Control Registers

ACTION	CONTROL REGISTER 1 (ADDRESS 007)	CONTROL REGISTER 2 (ADDRESS 008)	CONTROL REGISTER 3 (ADDRESS 009)	CONTROL REGISTER 4 (ADDRESS 00A)	CONTROL REGISTER 5 (ADDRESS 00B)
Disable-error correction for receive ATM-cell headers	xxxx xxx1	–	–	–	–
Disable-transmit ATM-cell header HEC-byte generation	xxxx xx1x	–	–	–	–
Enable-terminal loopback (TLB)	xxxx x1xx	–	–	–	–
Enable-facility loopback (FLB) output	xxxx 1xxx	–	–	–	–
Disable the dropping of ATM cells with multiple-bit header errors	xxx1 xxxx	–	–	–	–
Disable the dropping of ATM idle cells from the receive data stream	xx1x xxxx	–	–	–	–
Disable the dropping of ATM unassigned cells from the receive data stream	x1xx xxxx	–	–	–	–
Not implemented	1xxx xxxx	–	–	–	–
Enable-clock-loop output	–	xxxx xxx1	–	–	–
Transmit ATM unassigned cells as filler	–	xxxx xx1x	–	–	–
Place transmit-overhead RAM in program mode	–	xxxx x1xx	–	–	–
Cell-interface 16-bit alternate-data format	–	xxxx 1xxx	–	–	–
Force-transmit line AIS	–	xxx1 xxxx	–	–	–
Force-transmit line FERF	–	xx1x xxxx	–	–	–
Force-transmit path FERF	–	x1xx xxxx	–	–	–
Enable LOCA to path RDI soak count	–	1xxx xxxx	–	–	–
Force-transmit path AIS	–	–	xxxx xxx1	–	–
Disable receive SONET descrambler	–	–	xxxx xx1x	–	–
Disable receive ATM descrambler	–	–	xxxx x1xx	–	–
Disable transmit SONET scrambler	–	–	xxxx 1xxx	–	–
Disable transmit ATM scrambler	–	–	xxx1 xxxx	–	–
Enable short-frame-test mode	–	–	xx1x xxxx	–	–
Enable increment-counter-test mode	–	–	x1xx xxxx	–	–
Enable RAM-access-test mode	–	–	1xxx xxxx	–	–
Enable UTOPIA-loopback-test mode	–	–	–	xxxx xxx1	–
Force-transmit path RDI – 01	–	–	–	xxxx xx1x	–
Force-transmit path RDI – 10	–	–	–	xxxx x1xx	–

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Table 6. Coding for Control Registers (Continued)

ACTION	CONTROL REGISTER 1 (ADDRESS 007)	CONTROL REGISTER 2 (ADDRESS 008)	CONTROL REGISTER 3 (ADDRESS 009)	CONTROL REGISTER 4 (ADDRESS 00A)	CONTROL REGISTER 5 (ADDRESS 00B)
Force-transmit path RDI – 11	–	–	–	xxxx 1xxx	–
Enable SDH frames†	–	–	–	–	xxxx xxx1

† Changing the state of this bit can result in the loss of any data being processed by the transmitter (see the enable SDH frames bit description).

disable-error correction for receive ATM-cell headers

When set to a high level, this bit causes the error-detection and correction function to stop correcting single-bit errors that are detected in the headers of incoming ATM cells. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 provides single-bit error correction on the headers of incoming ATM cells; an action must be taken to disable this operation.

disable-transmit ATM-cell header HEC-byte generation

When set to a high level, this bit causes the transmit section to stop generating the header-error-check (HEC) byte in the 5-byte header of ATM cells being transmitted. When a reset operation occurs, this bit is cleared (set to 0). The normal operating mode of the TNETA1600 calculates the HEC byte from the first four bytes of the ATM cell that is transmitted and inserts the calculated value in the HEC-byte location.

enable-terminal loopback (TLB)

When set to a high level, this bit causes the ATM cells input through the transmit-cell interface to be looped through the device and output through the receive-cell interface. In this mode, ATM cells received on the transmit input flow normally through the transmit path to the scrambling function, where they are passed to the framing function in the receiver. The cells are then processed through the receive path and output on RD0–RD15. The receive input-data stream is blocked. However, the transmit section operates normally and the device continues to transmit ATM cells inserted in a STS-3c/STM-1 or STS-12c/STM-4c frame. Internally, this bit is logically ORed with TLB, allowing a terminal loopback to be enabled through either the external input pin or through the control register. When a reset operation occurs, the bit in the control register is cleared.

enable facility-loopback (FLB) output

When set to a high level, this bit causes the FLB output to go active (high). The FLB output can be connected to the FLB input on the TNETA1510/1610, and when it goes active, the TNETA1510/1610 facility loopback is enabled. This allows the FLB function on the TNETA1510/1610 to be controlled through the controller interface of the TNETA1600. When a reset operation occurs, the bit in the control register is cleared causing the FLB output to be inactive.

disable the dropping of ATM cells with multiple-bit header errors

When set to a high level, this bit causes the receive section to stop dropping ATM cells that contain multiple-bit header errors. When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1600 drops ATM cells that contain multiple-bit header errors by not placing them into the receive-output FIFO.

disable the dropping of ATM idle cells from the receive-data stream

When this bit is set, the receive section does not drop ATM idle cells from the receive-data stream. An idle cell is defined as an ATM cell with the 5-byte header set to a value of 00 00 00 01 52 (hex). When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1600 drops idle cells from the receive-data stream.

disable the dropping of ATM unassigned cells from the receive-data stream

When this bit is set, the receive section does not drop ATM unassigned cells from the receive-data stream. An unassigned cell is defined as an ATM cell with the 5-byte header set to a value of 00 00 00 00 55 (hex). When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1600 drops unassigned cells from the receive-data stream.

enable clock looping

When this bit is set, the CLKLOOP output goes high. The CLKLOOP output on the TNETA1600 can be connected to the CLKLOOP input on the TNETA1510/1610. When the CLKLOOP input on the TNETA1510/1610 is active, the clock-loop function on the TNETA1510/1610 is enabled. This allows the clock-loop function on the TNETA1510/1610 to be controlled through the controller interface on the TNETA1600. When a reset operation occurs, this bit is cleared.

transmit the ATM unassigned cells as filler

When this bit is set, the transmit side sends ATM unassigned cells for cell-rate decoupling when a user data cell is not available in the transmit FIFO. An unassigned cell is defined as a cell with the 5-byte header set to a value of 00 00 00 00 55 (hex). The payload is set to all 6A (hex) bytes. When this bit is not set, the device sends idle cells as filler cells for cell-rate decoupling. An idle cell is defined as a cell with the 5-byte header set to a value of 00 00 00 01 52 (hex) and the payload set to all 6A (hex) bytes. When a reset operation occurs, this bit is cleared.

place transmit-overhead RAM in program mode

This bit is logically ORed with IFPRGM. If either or both are high, the automatic write operations to transmit overhead by the TNETA1600 are disabled. During this condition, overhead values can be written into the TNETA1600 via the controller interface, and since these values are not automatically overwritten, this gives the user the capability to transmit any value in any overhead-byte location. Overhead-RAM addresses that are not written to retain their values. While in the program mode, the transmit data-communications port is disabled (TFPO is held low). When both IFPRGM and the associated control bit are low, specified overhead bytes are automatically overwritten each frame. Other bytes in the transmit-overhead RAM retain their programmed values until changed manually or by a reset.

cell-interface 16-bit alternate-data format

When this bit is set, the data format for both the transmit and receive 16-bit cell interface is set to format no. 2 in Figure 3. When this bit is cleared, the data format for both the transmit and receive 16-bit cell interface is set to format no. 1. This bit is cleared when a hardware or software reset occurs.

FORMAT NO. 1

MSB Bit 15	LSB Bit 0
Header Byte No. 1	Header Byte No. 2
Header Byte No. 3	Header Byte No. 4
UDB No. 1	UDB No. 2
Payload Byte No. 1	Payload Byte No. 2
:	:
:	:
Payload Byte No. 47	Payload Byte No. 48

FORMAT NO. 2

MSB Bit 15	LSB Bit 0
Header Byte No. 1	Header Byte No. 2
Header Byte No. 3	Header Byte No. 4
UDB No. 1	Payload Byte No. 1
Payload Byte No. 2	Payload Byte No. 3
:	:
:	:
Payload Byte No. 48	UDB No. 2

Figure 3. Cell-Interface 16-Bit Data Formats

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force-transmit line AIS

When set to a high level, this bit causes the insertion of valid SOH and a scrambled all-ones pattern for the remainer of the transmit signal. Also, ATM cells input to the transmit FIFO are not inserted into the outgoing frame. Once the FIFO is full, the device does not accept additional data on the transmit input until the device is returned to normal operating mode. When this bit is low, normal processing occurs. When a reset operation is performed, this bit is cleared (set to 0).

force-transmit line FERF

When set to a high level, this bit causes the insertion of a 110 in bits 6–8 of the transmit K2 byte. When this bit is low, normal processing dictates the values inserted in bits 6–8 of the K2 byte. When a reset operation is performed, this bit is cleared (set to 0).

force-transmit path FERF

When set to a high level, this bit causes the insertion of a 1001 pattern in bits 1–4 of the transmit G1 byte. When this bit is low, normal processing dictates the values inserted in bits 1–4 of the G1 byte. When a reset operation is performed, this bit is cleared (set to 0).

enable LOCA to path RDI soak count

When set to a high level, this bit enables the LOCA to path-RDI soak counter such that a persistent LOCA condition causes the automatic generation of a path RDI. When this bit is low, a persistent LOCA condition does not cause the transmission of a path RDI. When a reset operation occurs, this bit is cleared. The normal operation of the TNETA1600 is not to generate a path RDI as a result of a persistent LOCA condition.

force-transmit path AIS

When set to a high level, this bit causes the insertion of an all-ones signal in H1, H2, H3, and the entire transmit synchronous payload envelope (SPE) before scrambling. All transport-overhead bytes, other than H1–H3, are calculated and inserted normally. However, the receiving station is not able to locate the SPE and path-overhead bytes, since the pointer bytes are all ones. Also, ATM cells input to the transmit FIFO are not inserted into the outgoing frame. Once the FIFO is full, the device does not accept additional data on the transmit input until the device is returned to normal operating mode. When this bit is low, normal processing occurs. When a reset operation is performed, this bit is cleared (set to 0).

disable receive SONET descrambler

This bit is logically ORed with the TEST2 terminal. If either or both are set to a high level, SONET descrambling ($x^7 + x^6 + 1$) in the receiver is disabled. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to provide SONET descrambling in the receiver; an action must be taken to disable this function.

disable receive ATM descrambler

This bit is logically ORed with the TEST4 terminal. If either or both are set to a high level, ATM descrambling ($x^{43} + 1$) in the receiver is disabled. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to provide ATM descrambling in the receiver; an action must be taken to disable this function.

disable transmit SONET scrambler

This bit is logically ORed with the TEST1 terminal. If either or both are set to a high level, SONET scrambling ($x^7 + x^6 + 1$) in the transmitter is disabled. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to provide SONET scrambling in the transmitter; an action must be taken to disable this function.

disable transmit ATM scrambler

This bit is logically ORed with the TEST3 terminal. If either or both are set to a high level, ATM scrambling ($x^{43} + 1$) in the transmitter is disabled. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to provide ATM scrambling in the transmitter; an action must be taken to disable this function.

enable short-frame test mode

This bit is logically ORed with the TEST0 terminal. If either or both are set to a high level, the short-frame test mode is enabled. This causes the receive side to support frames consisting of 36 bytes of TOH and 84 bytes of SPE per row at 622.08 Mbit/s or 9 bytes of TOH and 21 bytes of SPE per row at 155.52 Mbit/s. Normal receive operation is also supported in this mode, including pointer processing only to the extent of valid J1 locations. When a reset operation is performed, this bit is cleared (set to 0). The normal operation state of the TNETA1600 is to support only normal frames, not shortened frames.

enable increment-counter test mode

When set to a high level, this bit causes all counters to be incremented by internal clocks without the occurrence of the associated conditions. The internal clocks used for this operation are derived from RPCK. When this mode is enabled, all block-error and ATM-cell counters are incremented by one on every two rising edges of RPCK. All coding-violation and FEBE counters are incremented by one on every four rising edges of RPCK. This allows the counters to be exercised without repeatedly generating the associated conditions. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to support counter increments only upon the occurrence of the associated condition.

enable RAM-access test mode

When set to a high level, this bit causes the controller interface to enter a special RAM-access mode. In this mode, read and write access to transmit- and receive-overhead RAM are provided through the controller interface. Internal access to the RAM is disabled. Consequently, transmit and receive circuitry is nonfunctional. When this mode is exited, the transmit side resets and default-overhead values are written to RAM. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to support the internal access to the RAM required for transmit and receive operations.

enable UTOPIA-loopback test mode

This bit is logically ORed with the TEST5 terminal. If either or both are set to a high level, a UTOPIA-loopback mode is enabled where ATM cells in the receiver are looped back from the receive-cell-interface FIFO output to the transmit-cell-interface FIFO input where they propagate through the transmit path. The transmit-input FIFO frequency is still set by TCKI, to avoid the loss of cells looped from the receiver to the transmitter. RCKI and TCKI must have the same frequency. When a reset operation is performed, this bit is cleared (set to 0). The normal operating state of the TNETA1600 is to disable this loopback capability.

force-transmit path RDI -01

When set to high level, this bit forces the transmission of a 0 in bit 5 and a 1 in bit 6 of the transmit G1 byte. When this bit is low, normal processing occurs such that the value inserted in bits 5 and 6 of the G1 byte follows, provided that they are not otherwise altered through the controller interface. When a reset operation is performed, this bit is cleared (set to 0).

force transmit path RDI -10

When set to a high level, this bit forces the transmission of a 1 in bit 5 and a 0 in bit 6 of the transmit G1 byte. When this bit is low, normal processing occurs such that the value inserted in bits 5 and 6 of the G1 byte follows, provided that they are not otherwise altered through the controller interface. When a reset operation is performed, this bit is cleared (set to 0).

force-transmit path RDI -11

When set to a high level, this bit forces the transmission of a 1 in bit 5 and a 1 in bit 6 of the transmit G1 byte. When this bit is low, normal processing occurs such that the value inserted in bits 5 and 6 of the G1 byte follows, provided that they are not otherwise altered through the controller interface. When a reset operation is performed, this bit is cleared (set to 0).

enable SDH frames

The bit is logically ORed with the SDHEN terminal. SDH frames are processed if this bit is set to a high level, if SDHEN is high, or if both are high. SONET frames are processed only if both SDHEN and this bit are low. To change the framing mode, a valid clock must be present on TPCK as new values are written to the transmit-overhead RAM. The transmit-framing functions are reset when the SONET/SDN mode is changed. Transmit-frame alignment may be lost, along with any data being processed in the transmit circuitry. When a hardware or software reset occurs, this bit is cleared (set to 0) and new values are written to overhead. These new overhead values are SONET values if SDHEN is low. If SDHEN is high, these new overhead values are SDH values.

ID register

The ID register is located at address 006 (hex). The register identifies the chip revision. It also provides a means of performing a software reset. The contents of this register are hardwired to a hexadecimal value of 5x (binary 0101 XXXX), where x (XXXX) denotes the chip revision. A software reset on the TNETA1600 device can be initiated by performing a write to the ID register through the controller interface. Since the contents of the ID register are hardwired, the write does not change the contents of the register. The software-reset function is logically ORed with the $\overline{\text{RESET}}$ input, so a reset of the TNETA1600 device can be initiated by taking the external pin low or by writing to the ID register. Because default SONET or SDH values are written to the overhead RAM, a valid clock must be present at TPCK when a software reset is executed. Similarly, a valid clock must be available to TPCK when the hardware-reset signal (on the $\overline{\text{RESET}}$ terminal) transitions from the low state back to the high (normal) state. For example, if operating the TNETA1600 with the TNETA1610, a common hardware-reset signal sent to each device's $\overline{\text{RESET}}$ terminal must remain low for at least TBD ms to ensure that the TNETA1610 TPCK clock output (to the TNETA1600) is valid when the RESET terminal returns high.

consecutive-event counts

The TNETA1600 contains several frame counters that provide a way to program the number of consecutive frames required to activate and deactivate alarms in the status registers. Table 7 lists the registers available through the TNETA1600 controller interface for such programmability. All registers have eight bits.

Table 7. Event Consecutive-Frame Counts

ADDRESS (HEX VALUE)	REGISTER
016	Line-AIS consecutive-frame count
017	Line-FERF consecutive-frame count
018	Line-RDI consecutive-frame count
019	LOCA to path-RDI soak count

line-AIS consecutive-frame count

A line-AIS condition is detected in a frame as a 111 in bits 6–8 of the K2 byte. Any other pattern is not an LAIS pattern. The input to this register represents the number of consecutive frames in which the condition must occur for activation and, independently, the required number of consecutive frames without the condition for deactivation of the LAIS bit in status register 2. As activation (and deactivation) may occur upon the detection of the condition for up to 15 consecutive frames, the four most-significant bits of the register are used to represent the number of consecutive frames (with the condition) required for activation while the four least-significant bits represent the number of consecutive frames (without the condition) required for deactivation. For example, to activate an interrupt through the status registers upon the detection of a condition

line-AIS consecutive-frame count (continued)

for seven consecutive frames and to deactivate upon the absence of the condition for two consecutive frames, 0111 0010 would be written to the register. The default value for LAIS activation and deactivation is five frames. When a reset operation is performed, a value of 0101 0101 is placed in the register.

line-FERF consecutive-frame count

A line-FERF condition is detected in a frame as a 110 in bits 6–8 of the K2 byte. Any other pattern is not an LFERF pattern. The input to this register represents the number of consecutive frames in which the condition must occur for activation and, independently, the required number of consecutive frames without the condition for deactivation of the LFERF bit in status register 2. As activation (and deactivation) may occur upon the detection of a condition for up to 15 consecutive frames, the four most-significant bits of the register are used to represent the number of consecutive frames (with the condition) required for activation while the four least-significant bits represent the number of consecutive frames (without the condition) required for deactivation. For example, to activate an interrupt through the status registers upon the detection of a condition for seven consecutive frames and to deactivate upon the absence of the condition for two consecutive frames, 0111 0010 is written to the register. The default value for LFERF activation and deactivation is five frames. When a reset operation is performed, a value of 0101 0101 is placed in the register.

path-RDI consecutive-frame count

A path-RDI condition is detected in a frame as a 1 in bit 5 or bit 6 (or both) of the G1 byte. A 00 in these bits indicates the absence of the condition. The input to this register represents the number of consecutive frames in which the condition must occur for activation and, independently, the required number of consecutive frames without the condition for deactivation of the PRDI bit in status register 3. As activation (and deactivation) may occur upon the detection of a condition for up to 15 consecutive frames, the four most-significant bits of the register are used to represent the number of consecutive frames (with the condition) required for activation while the four least-significant bits represent the number of consecutive frames (without the condition) required for deactivation. For example, to activate an interrupt through the status registers upon the detection of a condition for seven consecutive frames and to deactivate upon the absence of the condition for two consecutive frames, 0111 0010 is written to the register. The default value for PRDI activation and deactivation is ten frames. When a reset operation is performed, a value of 1010 1010 is placed in the register.

LOCA to path-RDI soak count

The input to this register provides a present to a counter that controls the amount of time, in increments of 125 μs that a LOCA condition must be present before a path-RDI condition is sent via the outgoing G1 byte. The exact amount of time required is not currently specified by any of the standard's organizations. This register is preset to a value of 32 (decimal) when a reset operation occurs. This corresponds to a soak time of 4 ms. The soak time can be modified by writing a new value to this register. For instance, in order to set the value in the counter to 1 ms, a value of eight (8 x 125 μs = 1 ms) is written in this register. However, the value has to be rewritten if a reset operation occurs, as the present value revert to 4 ms. This feature automatically generates a path RDI due to a LOCA condition when enabled (only if the appropriate bit is set in the control registers).

performance counters

The TNETA1600 contains several performance counters that provide running sums and statistics of various parameters. Table 8 lists the performance counters accessible through the TNETA1600 controller interface. All counters are 16-bit counters except the line-FEBE counter, the output ATM cell counter, and the discarded idle/unassigned-cell counter, which are 24-bit counters.

All counters are read/write and their contents can be sampled or preset. The counters are reset to zero when a device-reset operation occurs (i.e., when $\overline{\text{RESET}}$ goes low). The counters can also be effectively reset by writing zeroes to the register. The counters do not reset when they are read.

Table 8. TNETA1600 Counters

ADDRESS (HEX VALUE)	REGISTER
100	B1 coding-violation counter (lower 8 bits)
101	B1 coding-violation counter (upper 8 bits)
102 – 103	Not implemented
104	B2 coding-violation counter (lower 8 bits)
105	B2 coding-violation counter (upper 8 bits)
106 – 109	Not implemented
10A	B3 coding-violation counter (lower 8 bits)
10B	B3 coding-violation counter (upper 8 bits)
10C – 10D	Not implemented
10E	B1-block error counter (lower 8 bits)
10F	B1-block error counter (upper 8 bits)
110 – 111	Not implemented
112	B2-block error counter (lower 8 bits)
113	B2-block error counter (upper 8 bits)
114 – 115	Not implemented
116	B3-block error counter (lower 8 bits)
117	B3-block error counter (upper 8 bits)
118 – 119	Not implemented
11A	Line FEBE counter (lower 8 bits)
11B	Line FEBE counter (middle 8 bits)
11C	Line FEBE counter (upper 8 bits)
11D – 11F	Not implemented
120	Path FEBE counter (lower 8 bits)
121	Path FEBE counter (upper 8 bits)
122 – 123	Not implemented
124	Output ATM-cell counter (lower 8 bits)
125	Output ATM-cell counter (middle 8 bits)
126	Output ATM-cell counter (upper 8 bits)
127 – 129	Not implemented
12A	Discarded-idle/unassigned-cell counter (lower 8 bits)
12B	Discarded-idle/unassigned-cell counter (middle 8 bits)
12C	Discarded-idle/unassigned-cell counter (upper 8 bits)
12D – 12F	Not implemented
130	Single-bit-error ATM-cell counter (lower 8 bits)
131	Single-bit-error ATM-cell counter (lower 8 bits)
132 – 133	Not implemented
134	Multiple-bit-error ATM-cell counter (lower 8 bits)
135	Multiple-bit-error ATM-cell counter (upper 8 bits)
136 – 1FF	Not implemented

B1-/B2-/B3-coding-violation counters

These counters keep a total of the number of receive B1, B2, and B3 bit-interleaved parity (BIP) bits that are erred. When one of the counters reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counters automatically roll over to zero when they reach their maximum count.

B1-/B2-/B3-block-error counters

These counters keep a total of the number of frames received with B1, B2, and B3 errors. These counters track the number of frames with errors, but not the number of actual B1, B2, and B3 bits in error. When they reach their maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counters automatically roll over to zero when they reach their maximum count.

line-FEBE counter

This counter maintains a cumulative count of the number of incoming line FEBE reported through the receive third Z2 byte. When the counter reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and bit in the status register is set. The counter automatically rolls over to zero when it reaches its maximum count.

path-FEBE counter

This counter maintains a cumulative count of the number of incoming path FEBE reported through the receive G1 byte (bits 1-4). When the counter reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counter automatically rolls over to zero when it reaches its maximum count.

output ATM-cell counter

This counter provides a count of the number of cells placed in the receive output FIFO for subsequent output on the receive cell interface. Cells dropped in the receive path (i.e., idle cells if bit 5 at address 007 hex is a zero) are not included in this count. When the counter reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counter automatically rolls over to zero when it reaches it maximum count.

discarded-idle unassigned-cell counter

This counter provides a count of the number of idle, unassigned, or both idle and unassigned cells dropped, dependent upon the configuration of the device as given in the control register. When the counter reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counter automatically rolls over to zero when it reaches its maximum count.

single-bit-error ATM-cell counter

This counter provides a count of the number of ATM cells received with single-bit header errors. When the counter reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counter automatically rolls over to zero when it reaches its maximum count.

multiple-bit-error ATM-cell counter

This counter provides a count of the number of received ATM cells with multiple-bit header errors. When the counter reaches its maximum count, the $\overline{\text{INTR}}$ output goes active and a bit in the status register is set. The counter automatically rolls over to zero when it reaches its maximum count.

receive-overhead RAM

The TNETA1600 stores the receive-overhead bytes in the receive-overhead RAM beginning at address 200. There are 324 bytes in the transport overhead of a STS-12c signal and 36 bytes in the path overhead, for a total of 360 overhead bytes in a STS-12c signal. In addition, the data-communications bytes (D1–12) and orderwire bytes (E1 and E2) are also available through the serial receive data-communications port. Table 9 shows the overhead bytes and their addresses in the receive-overhead RAM. If EN155 is high, only every fourth address of the transport and path overhead is used (i.e., the three A1s are written to addresses 200, 204, and 208).

PRODUCT PREVIEW

Table 9. Receive-Overhead RAM

Transport Overhead (byte name / hex address) | **Path-Overhead Name/Address**

A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	J1	†	†	†
200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	211	212	213	214	215	216	217	218	219	21A	21B	21C	21D	21E	21F	220	221	222	223	224	225	226	227
B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	B3	†	†	†
228	229	22A	22B	22C	22D	22E	22F	230	231	232	233	234	235	236	237	238	239	23A	23B	23C	23D	23E	23F	240	241	242	243	244	245	246	247	248	249	24A	24B	24C	24D	24E	24F
D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	C2	†	†	†
250	251	252	253	254	255	256	257	258	259	25A	25B	25C	25D	25E	25F	260	261	262	263	264	265	266	267	268	269	26A	26B	26C	26D	26E	26F	270	271	272	273	274	275	276	277
H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	K2	G1	†	†	†
278	279	27A	27B	27C	27D	27E	27F	280	281	282	283	284	285	286	287	288	289	28A	28B	28C	28D	28E	28F	290	291	292	293	294	295	296	297	298	299	29A	29B	29C	29D	29E	29F
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K2	K2	K2	K2	K2	K2	K2	K2	K2	K2	K2	K2	F2	†	†	†
2A0	2A1	2A2	2A3	2A4	2A5	2A6	2A7	2A8	2A9	2AA	2AB	2AC	2AD	2AE	2AF	2B0	2B1	2B2	2B3	2B4	2B5	2B6	2B7	2B8	2B9	2BA	2BB	2BC	2BD	2BE	2BF	2C0	2C1	2C2	2C3	2C4	2C5	2C6	2C7
D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	K2	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	H4	†	†	†
2C8	2C9	2CA	2CB	2CC	2CD	2CE	2CF	2D0	2D1	2D2	2D3	2D4	2D5	2D6	2D7	2D8	2D9	2DA	2DB	2DC	2DD	2DE	2DF	2E0	2E1	2E2	2E3	2E4	2E5	2E6	2E7	2E8	2E9	2EA	2EB	2EC	2ED	2EE	2EF
D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	D9	D9	D9	D9	D9	D9	D9	D9	D9	D9	D9	D9	Z3	†	†	†
2F0	2F1	2F2	2F3	2F4	2F5	2F6	2F7	2F8	2F9	2FA	2FB	2FC	2FD	2FE	2FF	300	301	302	303	304	305	306	307	308	309	30A	30B	30C	30D	30E	30F	300	311	312	313	314	315	316	317
D10	D10	D10	D10	D10	D10	D10	D10	D10	D10	D10	D10	D11	D11	D11	D11	D11	D11	D11	D11	D11	D11	D11	D11	D12	D12	D12	D12	D12	D12	D12	D12	D12	D12	D12	D12	Z4	†	†	†
318	319	31A	31B	31C	31D	31E	31F	320	321	322	323	324	325	326	327	328	329	32A	32B	32C	32D	32E	32F	330	331	332	333	334	335	336	337	338	339	33A	33B	33C	33D	33E	33F
Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	E2	E2	E2	E2	E2	E2	E2	E2	E2	E2	E2	E2	Z5	†	†	†
340	341	342	343	344	345	346	347	348	349	34A	34B	34C	34D	34E	34F	350	351	352	353	354	355	356	357	358	359	35A	35B	35C	35D	35E	35F	360	361	362	363	364	365	366	367

64-Byte Path Trace (J1s‡) (byte name / hex address)

J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1
380	381	382	383	384	385	386	387	388	389	38A	38B	38C	38D	38E	38F	390	391	392	393	394	395	396	397	398	399	39A	39B	39C	39D	39E	39F									
J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1
3A0	3A1	3A2	3A3	3A4	3A5	3A6	3A7	3A8	3A9	3AA	3AB	3AC	3AD	3AE	3AF	3B0	3B1	3B2	3B3	3B4	3B5	3B6	3B7	3B8	3B9	3BA	3BB	3BC	3BD	3BE	3BF									

† The single daggers (†) in the path overhead represent fixed stuff patterns present in 622.08-Mbit/s signals.

‡ J1 in the path overhead is incrementally written to the 64 path-trace (J1) bytes in RAM. The cycle repeats after 64 J1s are processed, such that the 65th J1 is written to the same address as the 1st.

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transmit-overhead RAM

The TNETA1600 retrieves the transmit-overhead bytes from the transmit-overhead RAM beginning at hex address 400. During normal operation, the device calculates or sets the values of many of the transmit-overhead bytes. However, the user can program the values of many overhead bytes through the controller interface. The device also provides a serial-transmit data-communications port through which the data-communications (D1 – 12) and orderwire (E1 and E2) bytes can be input. When the device is placed in program mode, the user can set the values of all the transport- and path-overhead bytes. When the device is returned to normal operation, the device calculates or sets those bytes necessary to ensure the proper transmission of the frame. Table 10 shows the transmit-overhead bytes and their addresses in the transmit-overhead RAM. If EN155 is high, only every fourth address of the transport and path overhead is used (the three A1s are extracted from addresses 400, 404, and 408).

Table 10. Transmit-Overhead RAM

Transport Overhead (byte name / hex address) | **Path-Overhead Name/Address**

A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	C1	J1	†	†	†
400	401	402	403	404	405	406	407	408	409	40A	40B	40C	40D	40E	40F	410	411	412	413	414	415	416	417	418	419	41A	41B	41C	41D	41E	41F	420	421	422	423	42 4	425	426	427
B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1	E1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	F1	B3	†	†	†
428	429	42A	42B	42C	42D	42E	42F	430	431	432	433	434	435	436	437	438	439	43A	43B	43C	43D	43E	43F	440	441	442	443	444	445	446	447	448	449	44A	44B	44C	44D	44E	44F
D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D2	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	C2	†	†	†
450	451	452	453	454	455	456	457	458	459	45A	45B	45C	45D	45E	45F	460	461	462	463	464	465	466	467	468	469	46A	46B	46C	46D	46E	46F	470	471	472	473	474	475	476	477
H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	K2	G1	†	†	†
478	479	47A	47B	47C	47D	47E	47F	480	481	482	483	484	485	486	487	488	489	48A	48B	48C	48D	48E	48F	490	491	492	493	494	495	496	497	498	499	49A	49B	49C	49D	49E	49F
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K1	K2	K2	K2	K2	K2	K2	K2	K2	K2	K2	K2	K2	F2	†	†	†
4A0	4A1	4A2	4A3	4A4	4A5	4A6	4A7	4A8	4A9	4AA	4AB	4AC	4AD	4AE	4AF	4B0	4B1	4B2	4B3	4B4	4B5	4B6	4B7	4B8	4B9	4BA	4BB	4BC	4BD	4BE	4BF	4C0	4C1	4C2	4C3	4C4	4C5	4C6	4C7
D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D4	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	D5	K2	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	D6	H4	†	†	†
4C8	4C9	4CA	4CB	4CC	4CD	4CE	4CF	4D0	4D1	4D2	4D3	4D4	4D5	4D6	4D7	4D8	4D9	4DA	4DB	4DC	4DD	4DE	4DF	4E0	4E1	4E2	4E3	4E4	4E5	4E6	4E7	4E8	4E9	4EA	4EB	4EC	4ED	4EE	4EF
D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	D9	D9	D9	D9	D9	D9	D9	D9	D9	D9	D9	D9	Z3	†	†	†
2F0	4F1	4F2	2F3	4F4	4F5	4F6	4F7	4F8	4F9	4FA	4FB	4FC	4FD	4FE	4FF	500	501	502	503	504	505	506	507	508	509	50A	50B	50C	50D	50E	50F	500	511	512	513	514	515	516	517
D10	D10	D10	D10	D10	D10	D10	D10	D10	D10	D10	D10	D11	D11	D11	D11	D11	D11	D11	D11	D11	D11	D11	D11	D12	D12	D12	D12	D12	D12	D12	D12	D12	D12	D12	D12	Z4	†	†	†
518	519	51A	51B	51C	51D	51E	51F	520	521	522	523	524	525	526	527	528	529	52A	52B	52C	52D	52E	52F	530	531	532	533	534	535	536	537	538	539	53A	53B	53C	53D	53E	53F
Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	E2	E2	E2	E2	E2	E2	E2	E2	E2	E2	E2	E2	Z5	†	†	†
540	541	542	543	544	545	546	547	548	549	54A	54B	54C	54D	54E	54F	550	551	552	553	554	555	556	557	558	559	55A	55B	55C	55D	55E	55F	560	561	562	563	564	565	566	567

64-Byte Path Trace (J1s‡) (byte name / hex address)

J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1
580	581	582	583	584	585	586	587	588	589	58A	58B	58C	58D	58E	58F	590	591	592	593	594	595	596	597	598	599	59A	59B	59C	59D	59E	59F

J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1	J1
5A0	5A1	5A2	5A3	5A4	5A5	5A6	5A7	5A8	5A9	5AA	5AB	5AC	5AD	5AE	5AF	5B0	5B1	5B2	5B3	5B4	5B5	5B6	5B7	5B8	5B9	5BA	5BB	5BC	5BD	5BE	5BF

† The single daggers (†) in the path overhead represent fixed stuff patterns present in 622.08-Mbit/s signals.

‡ J1 in the path overhead is incrementally extracted from the 64 path-trace (J1) bytes in RAM. The cycle repeats after 64 J1s are processed, such that the 65th J1 is taken from the same address as the 1st.

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IEEE Std 1149.1 (JTAG) test access port

The TNETA1600 supports IEEE Std 1149.1-1990 (includes IEEE Std 1149.1a-1993). The boundary-scan feature can be used to facilitate testing of complex circuit-board assemblies. Scan access to the test-access-port (TAP) controller and the four test registers (instruction, bypass, device identification, and boundary scan) is accomplished via the five-wire TAP interface.

Five dedicated test terminals control the operation of the test circuitry: test data input TDI, test data output (TDO), test-mode select (TMS) input, test clock (TCK) input, and the test reset ($\overline{\text{TRST}}$) input. TDI is the serial input for shifting information into the instruction register or selected data register. TDO is the serial output for shifting information out of the instruction register or selected data register. TMS is used to direct the TAP controller through its states. TCK is used to sample data on TDI, output data on TDO, and clock the TAP controller. Data on the device inputs is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. $\overline{\text{TRST}}$ is an active-low input that can be asserted asynchronously to cause the TAP controller to enter the test-logic-reset state and configure the test-instruction register and test-data registers to their default values. $\overline{\text{TRST}}$ is held low during device power up.

The TNETA1600 boundary-scan architecture is comprised of the TAP controller and the four test registers: the instruction register with instruction decode, the bypass register, the device-identification register, and the boundary-scan register.

TAP controller

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This ensures that data (to be captured) is valid for fully one-half of the TCK clock cycle. The TAP controller extracts the TCK and TMS signals from the interface and generates the appropriate on-chip control signals for the test structures in the device. The TAP-controller state machine is clocked on the rising edge of TCK. Figure 5 illustrates the state transitions of the TAP controller.

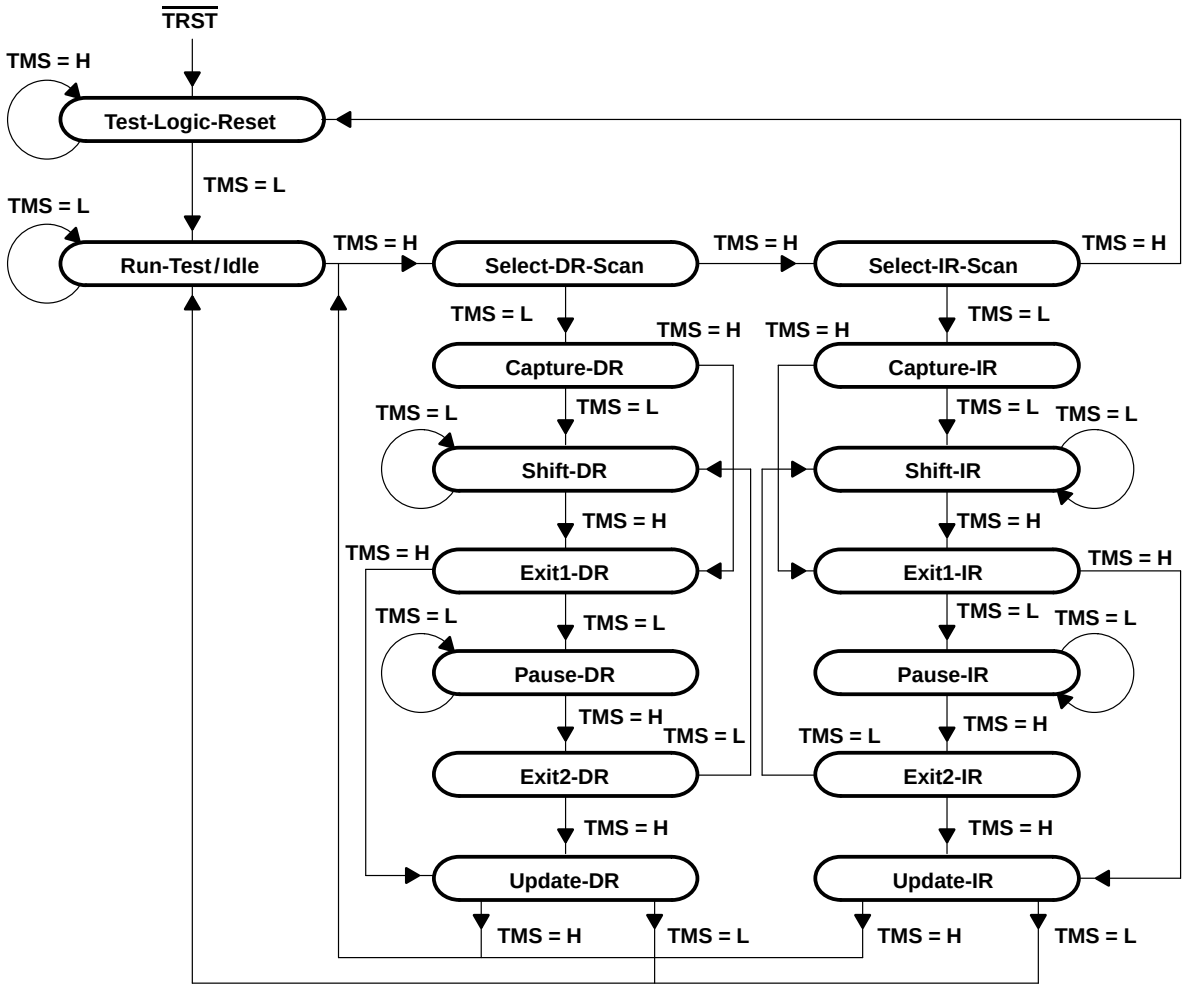

Figure 4. TAP-Controller State Diagram

The definitions of the states associated with the TAP controller follow:

test-logic-reset

$\overline{\text{TRST}}$ should be held low during device power-up to cause the TAP controller to enter the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and disabled so that the normal function of the device is performed. This state is entered asynchronously by asserting $\overline{\text{TRST}}$. This state is entered synchronously in no more than five TCK cycles if TMS is left high. While in this state, the instruction register is set to the IDCODE instruction. Each bit in the boundary-scan register is reset to logic zero, except bits TBD, which are reset to logic one.

run-test/idle

The controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. the Run-Test/Idle state can also be entered following data-register (DR) or instruction-register (IR) scans. This is a stable state in which the test logic is idle.

select-DR-scan, select-IR-scan

No specific function is performed in these states and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

capture-DR

In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits this state.

shift-DR

In the Shift-DR state, the selected test-data register shifts by one stage on the rising edge of TCK. Shifting is from most-significant bit (the bit nearest TDI) to least-significant bit (the bit nearest TDO).

exit1-DR, exit2-DR

These states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state can suspend and resume data-register scan operations without loss of data.

update-DR

If the current instruction calls for the selected data register to be updated with current data, such an update occurs on the falling edge of TCK following entry into the Update-DR state.

capture-IR

In the Capture-IR state, the instruction register captures the fixed binary value 1000 0001. The capture occurs on the rising edge of TCK, upon which the TAP controller exits this state.

shift-IR

In the Shift-IR state, the instruction register shifts by one stage on the rising edge of TCK. Shifting is from most-significant bit (the bit nearest TDI) to least-significant bit (the bit nearest TDO).

exit1-IR, exit2-IR

These states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state can suspend and resume instruction-register scan operations without loss of data.

update-IR

In the Update-IR state, the new instruction is loaded into the instruction register and takes effect on the falling edge of TCK following entry into the Update-IR state.

instruction register

The instruction register (IR) is eight bits long and specifies the instruction to be executed. Information contained in the instruction includes: 1) the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), 2) the test operation to be performed, 3) which of the four data registers is to be selected for inclusion in the scan path during data-register scans, and 4) the source of data to be captured into the selected data register during the Capture-DR state.

Table 11 lists the instructions supported by the TNETA1600. When in the Test-Logic-Reset state, the IR is reset to the binary value 1000 0001, which selects the IDCODE instruction.

Table11. Instruction-Register Decoding

BINARY CODE	INSTRUCTION	SELECTED REGISTER	MODE
0000 0000	EXTEST	Boundary Scan	Test
1000 0001	IDCODE	Device Identification	Normal
1000 0010	SAMPLE/PRELOAD	Boundary Scan	Normal
0000 0011	BYPASS	Bypass	Normal
1000 0100	BYPASS	Bypass	Normal
0000 0101	BYPASS	Bypass	Normal
0000 0110	HIGHZ	Bypass	Modified Test
1000 0111	CLAMP	Bypass	Test
1000 1000	BYPASS	Bypass	Normal
0000 1001	BYPASS	Bypass	Normal
0000 1010	BYPASS	Bypass	Normal
1000 1011	BYPASS	Bypass	Normal
0000 1100	CELLTST	Boundary Scan	Normal
1000 1101	BYPASS	Bypass	Normal
1000 1110	BYPASS	Bypass	Normal
0000 1111	BYPASS	Bypass	Normal
X111 0XXX	PRIVATE†	Private	Private†
All others	BYPASS	Bypass	Normal

† PRIVATE instructions are intended for manufacturing use only. These instructions may cause the device to enter unknown states and/or operate abnormally during and after the period when the PRIVATE instruction is active.

The descriptions of the instructions shown in Table 11 follow. Each instruction selects a test-data register in the scan path between TDI and TDO.

EXTEST

The external test instruction allows testing of board-level interconnections. When EXTEST is the current instruction, the boundary-scan register is selected in the scan path. TNETA1600 inputs are captured in the boundary-scan register in the Capture-DR state. These captured values are output by shifting the register in the Shift-DR state. Outputs of the TNETA1600 are set to a desired state by loading specific patterns (input through TDI during the Shift-DR state) into the boundary-scan register using the Update-DR state. The device operates in the test mode.

IDCODE

The IDCODE instruction connects the device-identification register in the scan path for serial access in the Shift-DR state. For the TNETA1600, the identification code is 0003202F (hex). The device operates in the normal mode.

SAMPLE/PRELOAD

The sample/preload instruction provides a sampling method for examining device inputs and outputs without interfering with the normal operation of the system logic in the device. The boundary-scan register is selected in the scan path. The TNETA1600 inputs and outputs are captured by loading the boundary-scan register in the Capture-DR state. These values are output by shifting the register through TDO in the Shift-DR state. This instruction also includes a preload function that allows a desired data pattern to be placed at the outputs of the boundary-scan register cells. The device operates in the normal mode.

BYPASS

This instruction allows system-level test data to be quickly passed through the TNETA1600 with a single clock-period delay. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during the Capture-DR state. The device operates in the normal mode.

HIGHZ

This instruction is used to place the TNETA1600 into a modified test mode in which all device output pins are placed in the high-impedance state. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during the Capture-DR state. Device input pins remain operational, and the normal on-chip logic is exercised.

CLAMP

The CLAMP instruction allows device outputs to be set and held at a desired state. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during the Capture-DR state. When the CLAMP instruction is selected, outputs are defined by data held in the boundary-scan register. These outputs do not change as long as the CLAMP instruction is selected. Device input pins remain operational, and the normal on-chip logic is exercised. The device operates in the test mode.

CELLTST

This instruction connects the boundary-scan register in the scan path. All boundary-scan cells capture the inverse of their current values during the Capture-DR state. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the boundary-scan register. The device operates in normal mode.

bypass register

The bypass register is a 1-bit scan path offering a single-bit delay from TDI to TDO. This register can be selected in the device scan path to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During the Capture-DR state, the bypass register captures a logic 0.

device-identification register

The device-identification register is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device. For the TNETA1600, the binary value (MSB to LSB) 0000 0000 0000 0011 0010 0000 0010 1111 (0003202F hex) is captured during the Capture-DR state in the device-identification register to identify the device as Texas Instruments TNETA1600. The device-identification register order of scan is from TDI through bits 31–0 to TDO.

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boundry-scan register

The boundary-scan register forces values on device-output terminals and/or captures data that appears at the inputs and/or outputs of the normal on-chip logic. The source of data to be captured into the boundary-scan register during the Capture-DR state is determined by the current instruction. While in the Test-Logic-Reset state, each bit in the boundary-scan register is reset to logic 0 except bits TBD which are reset to logic 1. The boundary-scan register order of scan is from TDI, through bits 109–0, to TDO. Table 12 shows the boundary-scan register bits and their associated device-pin signals.

pointer-processing test functionality

The TAP interface accesses pointer-processing circuitry for a more efficient manufacturing test and a more comprehensive fault coverage on certain portions of this circuitry. The following paragraphs are primarily intended for use by the manufacturer.

This special test functionality tests circuitry for the address generation and comparison of all valid J1 pointer locations, as well as the path-overhead column locations. The synchronous payload envelope-counter operation and x-column position counter operation are also verified. Algorithms used to check the validity of pointer addressing, identifying NDF, LOP and other pointer-processing functions are not verified in this test mode.

When placed into this test mode, the circuitry is first reset and placed into the decrement mode beginning at J1 = 0. Each pulse of the test clock then increments the SPE counter, while every third clock decrements the J1-pointer value. For STS-3c, only every third SPE location is used for J1. No comparison is performed during this time, since the address values are running in the opposite direction from the SPE values. However, the decrements must happen properly or the remainder of the test procedure fails. After a specified number of test clock cycles, J1 is decremented through the entire range of values returning to J1 = 0.

Next, the circuitry must be placed into the increment mode and incremented through the J1 range. During this phase, the SPE counter and incremented addresses are compared. This should result in a matched signal on every third position. This matched signal is scanned into a signature register and also used as feedback to control the clock signal. Any failure on this comparison causes the SPE counter and address increment to get out of step, resulting in no further matches for the remainder of the test. At the end of this procedure if all J1 values are valid, a test result signature is scanned out, verifying the test results.

Table 12. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
109	TXCLAV	72	IFPRGM	35	RD13
108	TWE	71	RDWR	34	RD12
107	TXSOC	70	SEL	33	RD11
106	TCKI	69	READY	32	RD10
105	TDEN	68	INTR	31	RD9
104	TFPO	67	RTNCK	30	RD8
103	TCO	66	TPD0	29	RD7
102	TSDI	65	TPD1	28	RD6
101	TXREF8K	64	TPD2	27	RD5
100	A10	63	TPD3	26	RD4
99	A9	62	TPD4	25	RD3
98	A8	61	TPD5	24	RD2
97	A7	60	TPD6	23	RD1
96	A6	59	TPD7	22	RD0
95	A5	58	TPCK	21	LOCA
94	A4	57	LOPC	20	LOSRD
93	A3	56	CLKLOOP	19	RXCLAV
92	A2	55	FLB	18	RXSOC
91	A1	54	RESET	17	RRE
90	A1	53	RPCK	16	RCKI
89	D7	52	RPD0	15	TD15
88	D6	51	RPD1	14	TD14
87	D5	50	RPD2	13	TD13
86	D4	49	RED3	12	TD12
85	D3	48	RPD4	11	TD11
84	D2	47	RPD5	10	TD10
83	D1	46	RPD6	9	TD9
82	D0	45	RPD7	8	TD8
81	TEST5	44	OOF	7	TD7
80	TEST4	43	TLB	6	TD6
79	TEST3	42	LOF	5	TD5
78	TEST2	41	RXREF8K	4	TD4
77	TEST1	40	RSDO	3	TD3
76	TEST0	39	RCO	2	TD2
75	SDHEN	38	RFPO	1	TD1
74	EN155	37	RD15	0	TD0
73	OE	36	RD14		

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC1}: TTL (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range, V_{CC2}: PECL (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I: TTL . . . . . –1.2 V to 7 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage, TTL		4.75	5.25	V
V_{IH}	High-level input voltage	TTL	2		V
V_{IL}	Low-level input voltage	TTL		0.8	V
T_A	Operating free-air temperature		–40	85	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_{IK} = – 18 mA		–1.2	V
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OH} = – 4 mA	4.25		V
V_{OL}	Low-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OL} = 4 mA		0.5	V
I_I	Input current	TTL	V_{CC} = 5.25 V,	$V_I = V_{CC}$ or GND		± 300	µA
I_{CC}	Supply current		V_{CC} = 5.25 V, I_O = 0	f = 155.52 Mbit/s			mA
				f = 622.08 Mbit/s			
C_i	Input capacitance	TTL					pF

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timing requirements (see Figure 5)

NO.			MIN	MAX	UNIT
	$f_{clock(TCKI)}$	Clock frequency, TCKI			MHz
1,2		Duty cycle, TCKI, Percent			
1,2	$t_{r(TCKI)}$	Rise time, TCKI			ns
1,2	$t_{f(TCKI)}$	Fall time, TCKI			ns
3	$t_{su(TWE)}$	Setup time, $\overline{TWE}\uparrow$ before TCKI$\uparrow$			ns
4	$t_{su(TXSOC)}$	Setup time, TXSOC$\uparrow$ before TCKI$\uparrow$			ns
5	$t_{su(TD0–TD15)}$	Setup time, TD0–TD15 valid before TCKI$\uparrow$			ns
6	$t_{h(TWE)}$	Hold time $\overline{TWE}\downarrow$ after TCKI$\uparrow$			ns
7	$t_{h(TXSOC)}$	Hold time, TXSOC$\downarrow$ after TCKI$\uparrow$			ns
8	$t_{h(TD0–TD15)}$	Hold time, TD0–TD15 valid after TCKI$\uparrow$			ns

operating characteristics (see Figure 5)

NO.	PARAMETER		MIN	MAX	UNIT
9	$t_{d(TXCLAV)1}$	Delay time, TCKI$\uparrow$ to TXCLAV$\downarrow$			ns
10	$t_{d(TXCLAV)2}$	Delay time, TCKI$\uparrow$ to TXCLAV$\uparrow$			ns

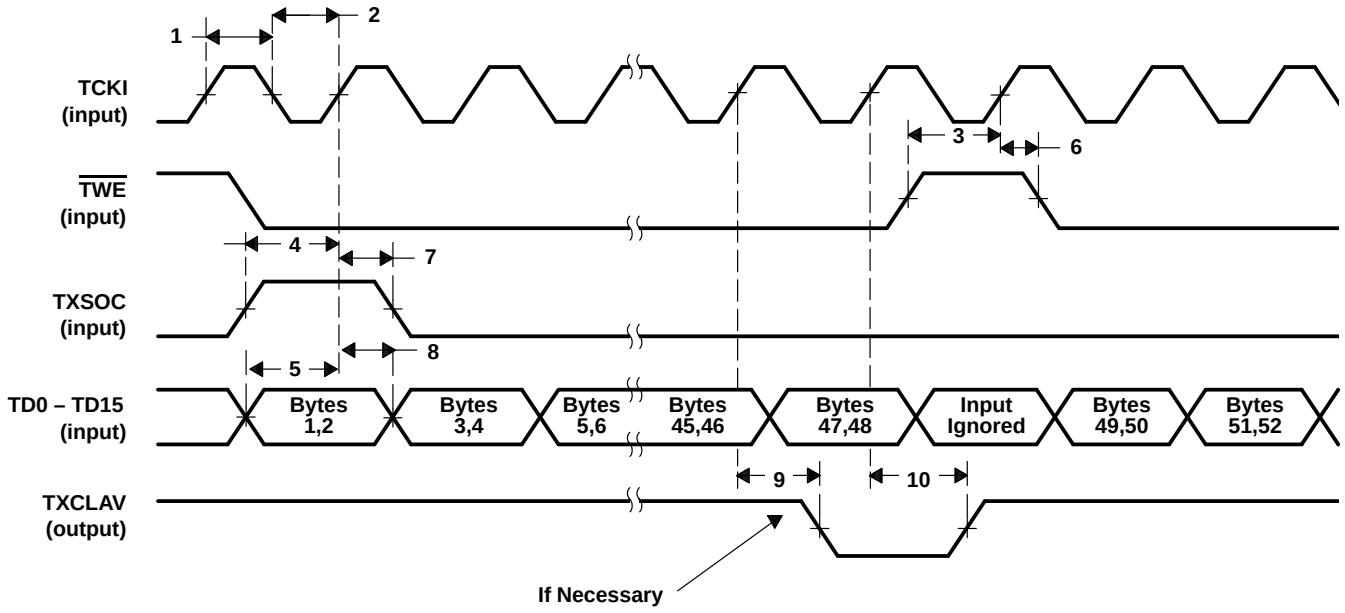

Figure 5. Transmit-Cell Interface

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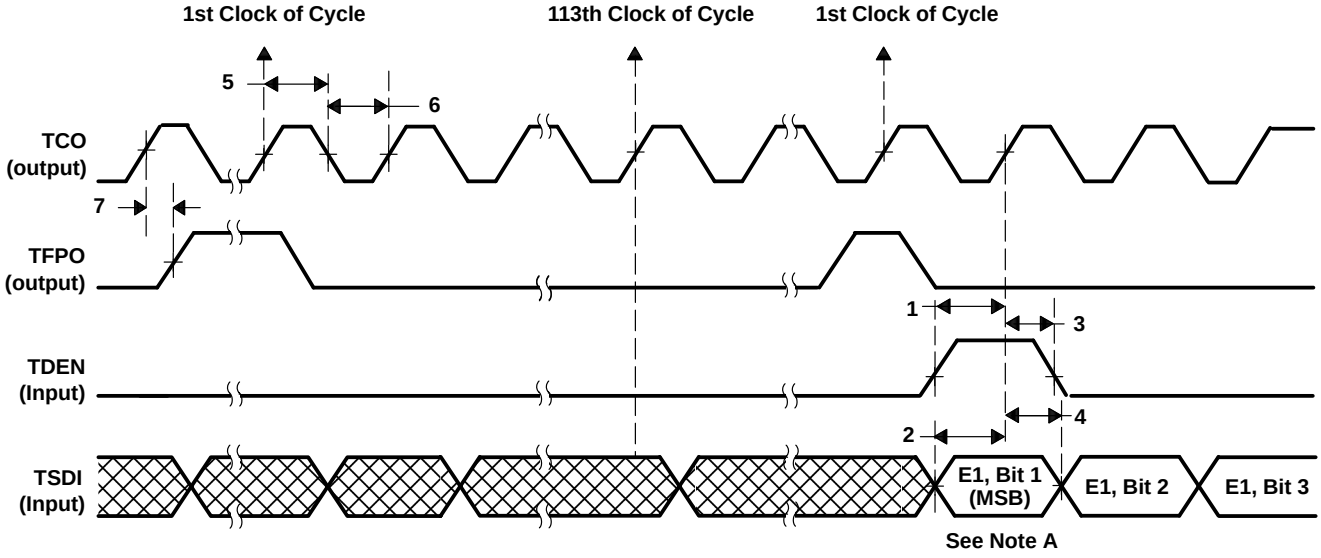
timing requirements (see Figure 6)

NO.			MIN	MAX	UNIT
1	$t_{su(TDEN)}$	Setup time, TDEN↑ before TCO↑			ns
2	$t_{su(TSDI)}$	Setup time, TSDI valid before TCO↑			ns
3	$t_{h(TDEN)}$	Hold time, TDEN↓ before TCO↑			ns
4	$t_{h(TSDI)}$	Hold time, TSDI valid after TCO↑			ns

operating characteristics (see Figure 6)

NO.	PARAMETER		MIN	MAX	UNIT
5	$t_{w(TCOH)}$	Pulse duration, TCO high			ns
6	$t_{w(TCOL)}$	Pulse duration, TCO low			ns
7	$t_{d(TFPO)}$	Delay time, TCO↑ to TFPO↑			ns



NOTE A: The state of TDEN is examined by TNETA1600 on the rising edge of TCO associated with the first bit (MSB) of each orderwire and data-communications byte. When TDEN is high on the first bit of the particular byte, that entire byte is read on TSDI. When TDEN is low on the first bit, TSDI is ignored for the eight clock cycles associated with that byte and that byte retains the value existing in overhead RAM. TDEN is reexamined on the first bit of the next byte.

Figure 6. Transmit Data-Communications Interface

timing requirements (see Note 2 and Figure 7)

NO.			MIN	MAX	UNIT
1	$t_{w(TPCKL)}$	Pulse duration, TPCK low			ns
2	$t_{w(TPCKH)}$	Pulse duration, TPCK high			ns

operating characteristics (see Note 2 and Figure 7)

NO.	PARAMETER		MIN	MAX	UNIT
3	$t_{d(RTNCK)}$	Delay time, TPCK↑ to RTNCK↑			ns
4	$t_{d(TPD0–TPD7)}$	Delay time, TPCK↑ to TPD0–TPD7 valid			ns
5	$t_{csp(TPD0–TPD7)}$	Deviation of clock-sampling point, transmit high-speed data			ns

NOTE 2: Data for this interface is valid only for capacitive loads not exceeding 15 pF.

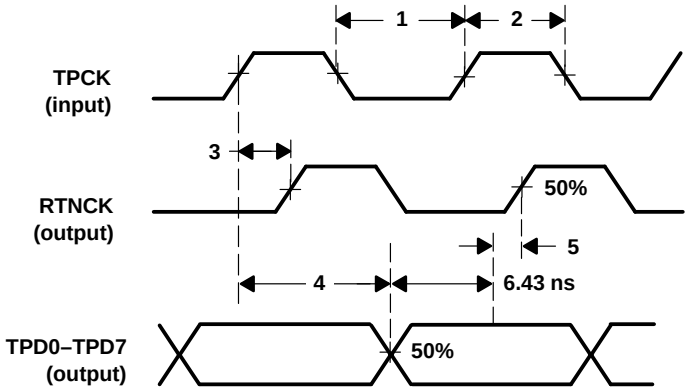


Figure 7. Transmit High-Speed Interface

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timing requirements (see Figure 8)

NO.			MIN	MAX	UNIT
1	$t_{w(RPCKH)}$	Pulse duration, RPCK high			ns
2	$t_{w(RPCKL)}$	Pulse duration, RPCK low			ns
3	$t_{su(RPD0–RPD7)}$	Setup time, RPD0–RPD7 valid before RPCK↑			ns
4	$t_{h(RPD0–RPD7)}$	Hold time, RPD0–RPD7 valid after RPCK↑			ns

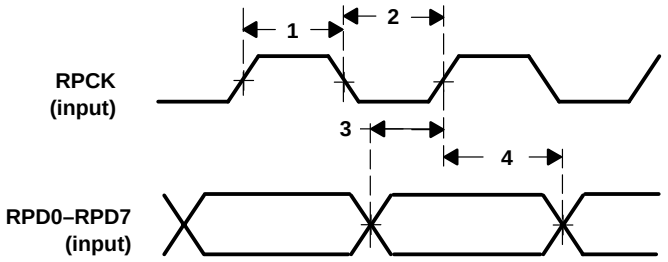

Figure 8. Receive High-Speed Interface

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operating characteristics (see Figure 9)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(RCOL)}$	Pulse duration, RCO low			ns
2	$t_{w(RCOH)}$	Pulse duration, RCO high			ns
3	$t_{d(RFPO)}$	Delay time, RCO↑ to RFPO↑			ns
4	$t_{d(RSDO)}$	Delay time, RCO↑ to RSDO valid			ns

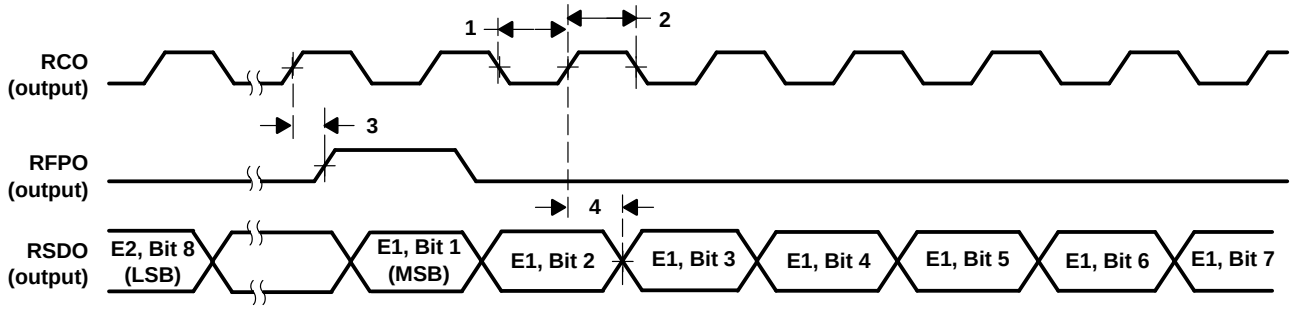

Figure 9. Receive Data-Communications Interface

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timing requirements (see Figure 10)

NO.			MIN	MAX	UNIT
1	$t_{w(RCKIH)}$	Pulse duration, RCKI high			ns
2	$t_{w(RCKIL)}$	Pulse duration, RCKI low			ns
3	$t_{su(RRE)}$	Setup time, $\overline{RRE}$ high before RCKI↑			ns
4	$t_{h(RRE)}$	Hold time, $\overline{RRE}$ high after RCKI↑			ns

operating characteristics (see Figure 10)

NO.	PARAMETER		MIN	MAX	UNIT
5	$t_{d(RXSOC)}$	Delay time, RCKI↑ to RXSOC↑			ns
6	$t_{d(RD0–RD15)}$	Delay time, RCKI↑ to RD0–RD15 valid			ns
7	$t_{d(RXCLAV)}$	Delay time, RCKI↑ to RXCLAV↓			ns
8	$t_{d(RXCLAV)}$	Delay time, RCKI↑ to RXCLAV↑			ns

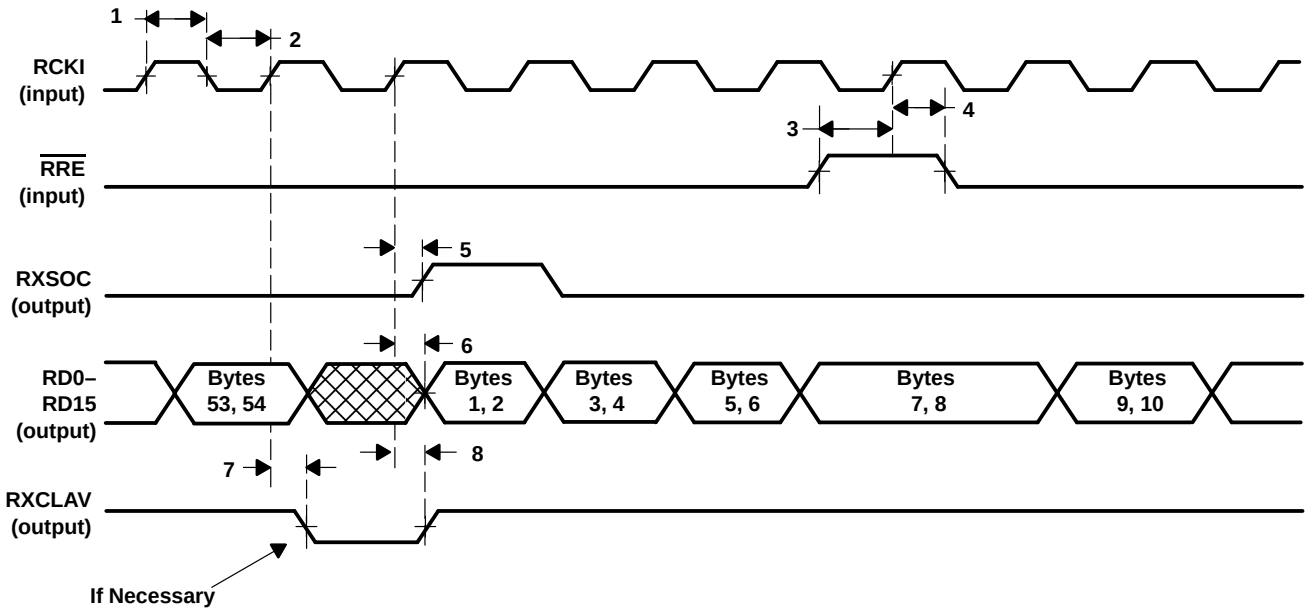

Figure 10. Receive-Cell Interface

timing requirements (see Figure 11)

NO.			MIN	MAX	UNIT
1	$t_{su(RD/WR)}$	Setup time, RD/$\overline{WR}$ high before $\overline{SEL}\downarrow$			ns
2	$t_{su(A0–A10)}$	Setup time, A0–A10 valid before $\overline{SEL}\downarrow$			ns
3	$t_{h(A0–A10)}$	Hold time, A0–A10 valid after $\overline{SEL}\downarrow$			ns
4	$t_{h(SEL)}$	Hold time, $\overline{SEL}$ low after $\overline{READY}\downarrow$			ns
5	$t_{h(RD/WR)}$	Hold time, RD/$\overline{WR}$ high after $\overline{SEL}\uparrow$			ns

operating characteristics (see Figure 11)

NO.	PARAMETER		MIN	MAX	UNIT
6	$t_{d(READY)1}$†	Delay time, $\overline{SEL}\downarrow$ to $\overline{READY}\downarrow$			ns
7	$t_{d(READY)2}$	Delay time, $\overline{SEL}\uparrow$ to $\overline{READY}\uparrow$			ns
8	$t_{d(D0–D7)1}$	Delay time, D0–D7 valid to $\overline{READY}\downarrow$			ns
9	$t_{d(D0–D7)2}$	Delay time, $\overline{SEL}\uparrow$ to D0–D7 invalid			ns

† When accessing status registers, interrupt-mask registers, control registers, counters, etc. (addresses 000–1FF), the maximum delay ($\overline{SEL}\downarrow$ to $\overline{READY}\downarrow$) is to be determined (TBD) in nanoseconds. However, when accessing overhead RAM (addresses 200–5FF), the negative transition of $\overline{READY}$ in response to $\overline{SEL}$ may be delayed by internal usage of the overhead RAM. In this case, the maximum possible delay is TBD in microseconds.

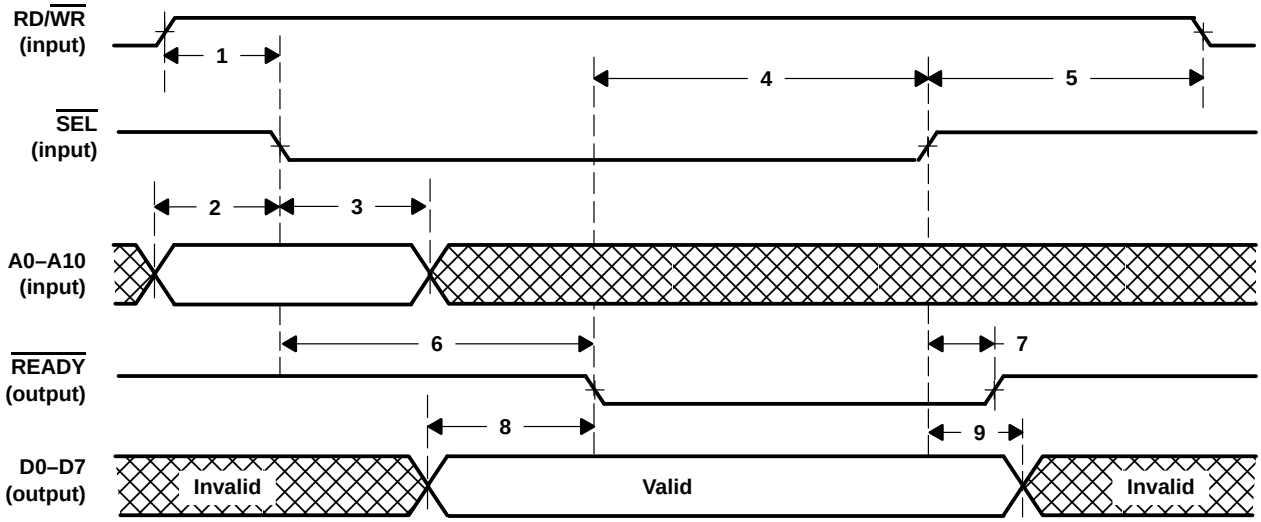

Figure 11. Controller-Interface Read Cycle

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timing requirements (see Figure 12)

NO.			MIN	MAX	UNIT
1	$t_{su(RD/WR)}$	Setup time, RD/$\overline{WR}$ low before $\overline{SEL}\downarrow$			ns
2	$t_{su(A0–A10)}$	Setup time, A0–A10 valid before $\overline{SEL}\downarrow$			ns
3	$t_{su(D0–D7)}$	Setup time, D0–D7 valid before $\overline{SEL}\downarrow$			ns
4	$t_{h(D0–D7)}$	Hold time, D0–D7 valid after $\overline{SEL}\downarrow$			ns
5	$t_{h(A0–A10)}$	Hold time, A0–A10 valid after $\overline{SEL}\downarrow$			ns
6	$t_{h(SEL)}$	Hold time, $\overline{SEL}$ low after $\overline{READY}\downarrow$			ns
7	$t_{h(RD/WR)}$	Hold time, RD/$\overline{WR}$ low after $\overline{SEL}\uparrow$			ns

operating characteristics (see Figure 12)

NO.	PARAMETER		MIN	MAX	UNIT
8	$t_{d(READY)1}$†	Delay time, $\overline{SEL}\downarrow$ to $\overline{READY}\downarrow$			ns
9	$t_{d(READY)2}$	Delay time, $\overline{SEL}\uparrow$ to $\overline{READY}\uparrow$			ns

† When accessing status registers, interrupt-mask registers, control registers, counters, etc. (addresses 000–1FF), the maximum delay ($\overline{SEL}\downarrow$ to $\overline{READY}\downarrow$) is to be determined (TBD) in nanoseconds. However, when accessing overhead RAM (addresses 200–5FF), the negative transition of $\overline{READY}$ in response to $\overline{SEL}$ may be delayed by internal usage of the overhead RAM. In this case, the maximum possible delay is TBD in microseconds.

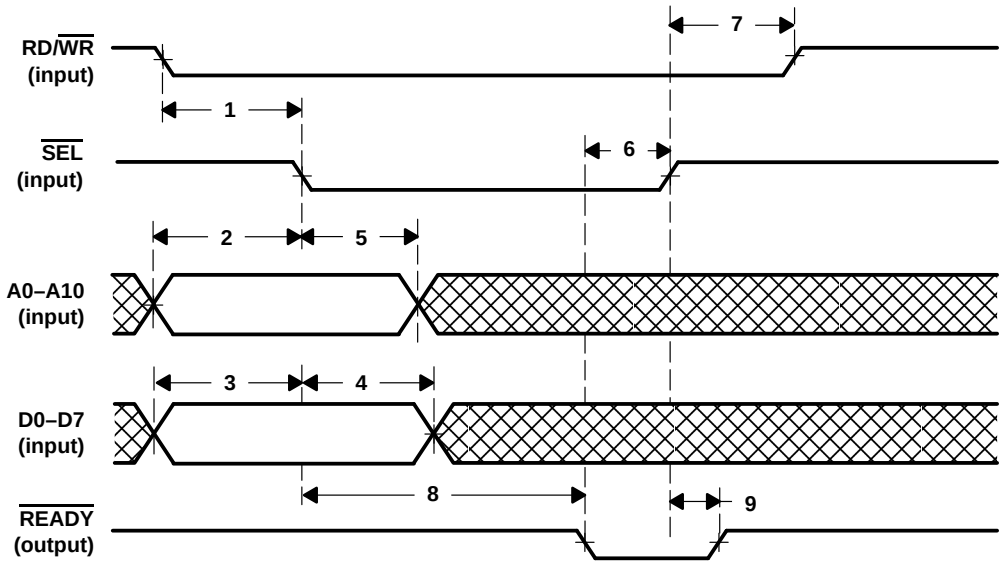

Figure 12. Controller-Interface Write Cycle

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timing requirements (see Figure 13)

NO.			MIN	MAX	UNIT
	$f_{clock(TCK)}$	Clock frequency, TCK		10	MHz
1	$t_{w(TCKL)}$	Pulse duration, TCK low			ns
2	$t_{w(TCKH)}$	Pulse duration, TCK high			ns
3	$t_{su(TDI)}$	Setup time, TDI valid before TCK↑			ns
3	$t_{su(TMS)}$	Setup time, TMS valid before TCK↑			ns
4	$t_{h(TDI)}$	Hold time, TDI valid after TCK↑			ns
4	$t_{h(TMS)}$	Hold time, TMS valid after TCK↑			ns

operating characteristics (see Figure 13)

NO.	PARAMETER		MIN	MAX	UNIT
5	$t_{d(TDO)}$	Delay time, TCK↓ to TDO valid			ns

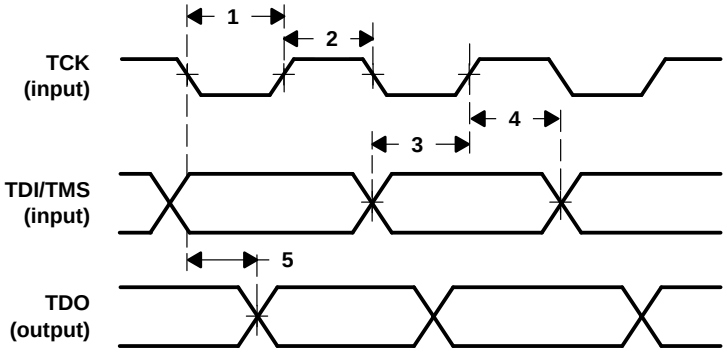

Figure 13. JTAG TAP Controller

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