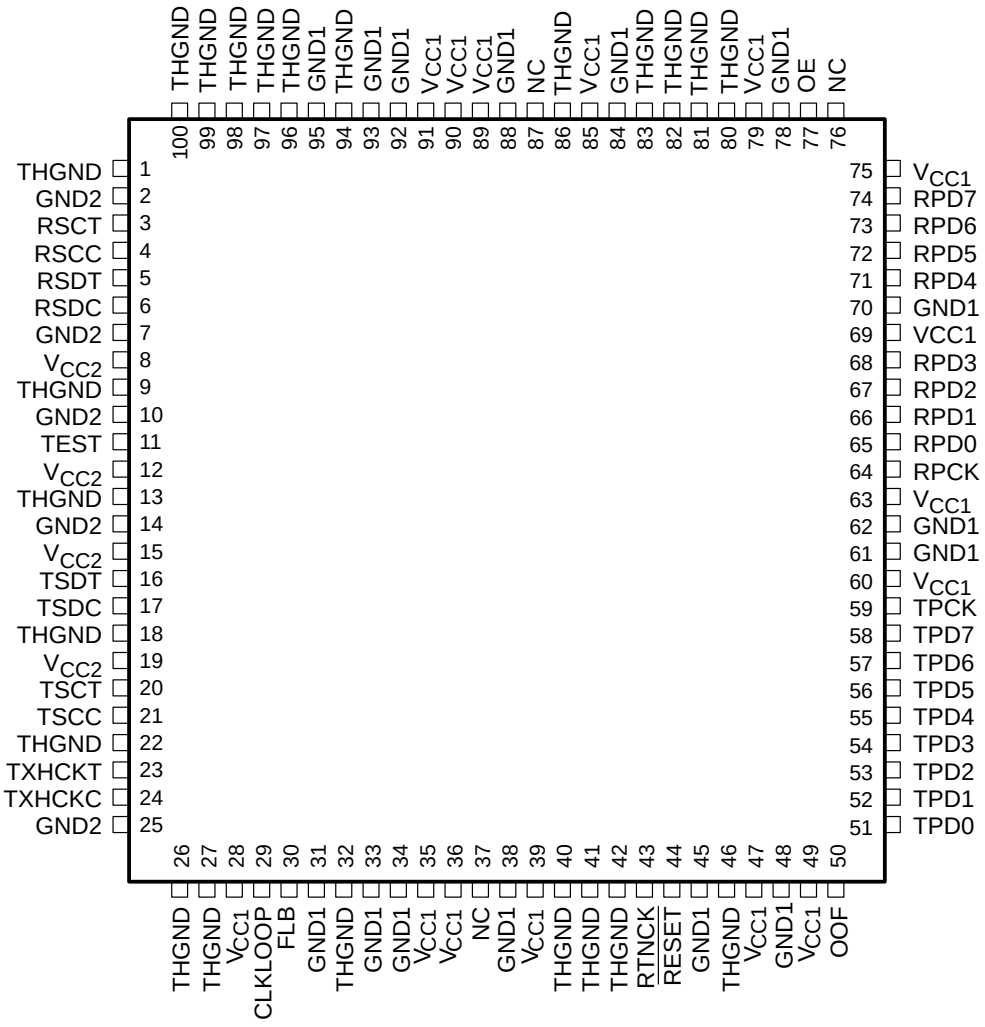
SDNS035E – AUGUST 1995 – REVISED JUNE 1996

- **Serial-to-Parallel/Parallel-to-Serial Conversion for 622.08-Mbit/s Data Streams**
- **Transmit Clock Is Selectable From an External 622.08-MHz Clock or the Receive-Clock Input**
- **Performs Bit-Alignment Function for SONET/SDH Frames**
- **Loopback Capability Increases Product Versatility**
- **Conforms to SONET/SDH Standards**

description

The TNETA1611 is an STS-12c/STM-4 receiver/transmitter that performs data serialization and deserialization for 622.08-Mbit/s data streams used in STS-12c/STM-4 systems. On the receive side, bit alignment is performed on the serial input data such that parallel data is output on SONET/SDH byte boundaries. The TNETA1611 conforms to applicable SONET/SDH standards and can simultaneously convert the serial data to byte-wide data and the byte-wide data to serial data. Clock and data loopback features increase versatility. The TNETA1611 is designed for operation with a heat sink over a temperature range of –40°C to 85°C.

PCA PACKAGE
(TOP VIEW)



NC – No internal connection
THGND – Thermal ground (no internal electrical connection)

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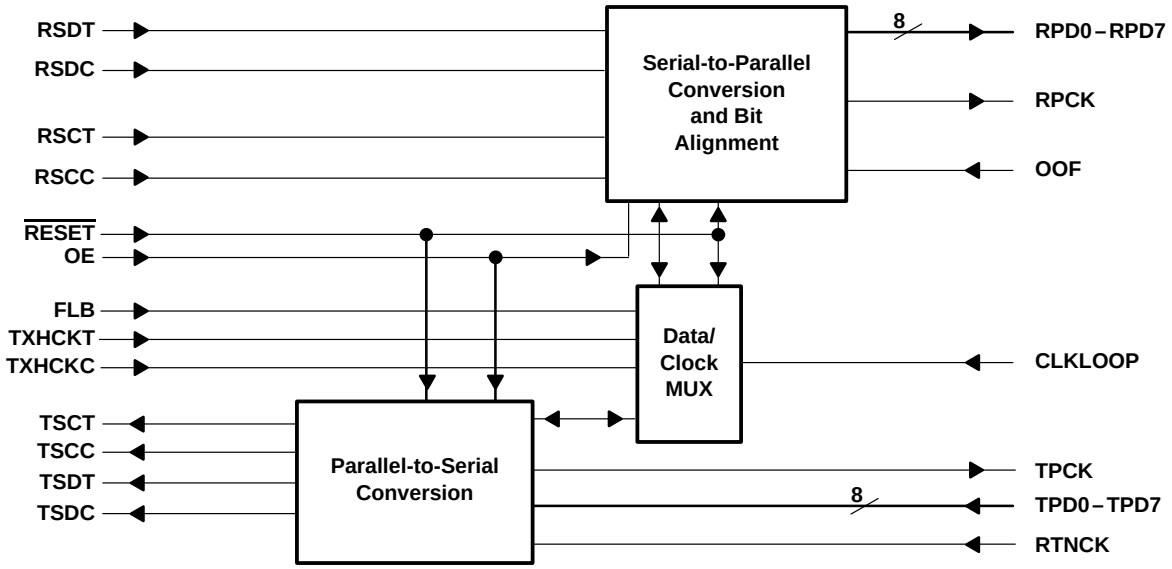
functional block diagram



detailed description

transmit operation

The transmit parallel interface consists of TTL-compatible byte-wide input data (TPD0–TPD7), a TTL-compatible transmit output clock (TPCK), and a TTL-compatible return clock input (RTNCK). TPCK is an output to associated processing elements (i.e., a framer) that controls the output of byte-wide transmit data from such devices. The return clock and data are input to the TNETA1611 such that byte-wide transmit data (TPD0–TPD7) is clocked into the TNETA1611 on low-to-high transitions of RTNCK. If a return clock is not available, RTNCK can be tied to TPCK provided the timing requirements between TPCK and TPD0–TPD7 can be met.

The byte-wide data is converted to a 622.08-Mbit/s serial-data stream that is sent out differentially on transmit serial-data true (TSDT) and transmit serial-data complement (TSDC). In addition, a phase-aligned 622.08-MHz clock is sent out differentially on transmit serial-clock true (TSCT) and transmit serial-clock complement (TSCC). The serial output data is valid on the rising edge of TSCT. TSDT, TSDC, TSCT, and TSCC are pseudo-ECL-compatible outputs.

The transmit clock source can come from either of two inputs. If transmit clock loop (CLKLOOP) is low, an external 622.08-MHz clock source is used. This differential transmit high-speed clock input enters on pseudo-ECL-compatible terminals TXHCKT and TXHCKC. If CLKLOOP is high, the receive serial clock (RSCT and RSCC) input with the receive data stream is used for transmit operations.

A facility-loopback (FLB) option is also available. When FLB is high, data input into the receiver and the corresponding clock are looped back and provided at the transmitter outputs. This allows a method for loopback testing in a system.

Transmit functions are reset by taking $\overline{\text{RESET}}$ low. This action can result in the loss of any data being processed.

receive operation

Serial data is provided to the TNETA1611 on true and complement pseudo-ECL-compatible inputs (RSDT and RSDC). A 622.08-MHz pseudo-ECL-compatible clock (RSCT and RSDC) must accompany the data such that the data is valid on the rising edge of the true clock (RSCT) signal. The serial data is converted to byte-wide data and directed out on RPD0–RPD7. This output data is accompanied by a clock (RPCK). RPD0–RPD7 and RPCK are TTL-compatible outputs.

The TNETA1611 utilizes the out-of-frame (OOF) signal generated by subsequent processing elements for bit alignment. When OOF goes high, the TNETA1611 begins searching the received data for a string of 12 consecutive A1 bytes (12 hex F6s). Once this sequence is found, the TNETA1611 aligns the byte-wide data output with the A1-byte boundaries so that subsequent data (i.e., the A2 bytes) is properly aligned. The subsequent processing element (i.e., a framer) must detect and monitor the byte-aligned data for complete SONET/SDH framing patterns (12 A1s followed by 12 A2s) to ensure standards compliance for functions like loss of frame, etc. The TNETA1611 does not realign the output when OOF is low.

An output-enable (OE) terminal is provided to enable/disable all TTL outputs. When OE is low, RPCK, RPD0–RPD7, and TPCK are held in the high-impedance state. When OE is high, these terminals function as previously described.

Receive functions are reset by taking $\overline{\text{RESET}}$ low. This action can result in the loss of any data being processed.

data/clock source control

There are three control inputs to the TNETA1611 that change the source of data (and/or clock) for a given output. The effects of these inputs (OE, CLKLOOP, and FLB) are indicated in the following table.

STATE OF CONTROL INPUTS			SOURCE OF DATA/CLOCK FOR OUTPUTS				
OE	CLKLOOP	FLB	TSDT/TSDC	TSCT/TSCC	TPCK	RPDO–RPD7	RPCK
0	0	0	N/A†	TXHCKT/TXHCKC	High impedance	High impedance	High impedance
0	0	1	RSDT/RSDC	RSCT/RSCC	High impedance	High impedance	High impedance
0	1	0	N/A†	RSCT/RSCC	High impedance	High impedance	High impedance
0	1	1	RSDT/RSDC	RSCT/RSCC	High impedance	High impedance	High impedance
1	0	0	TPD0–TPD7	TXHCKT/TXHCKC	TXHCKT/TXHCKC	RSDT/RSDC	RSCT/RSCC
1	0	1	RSDT/RSDC	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	1	0	TPD0–TPD7	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC
1	1	1	RSDT/RSDC	RSCT/RSCC	RSCT/RSCC	RSDT/RSDC	RSCT/RSCC

† This is not a normal operating condition. As no clock is output on TPCK, valid data cannot be properly input on TPD0–TPD7; thus, the data output on TSDT/TSDC may be invalid.

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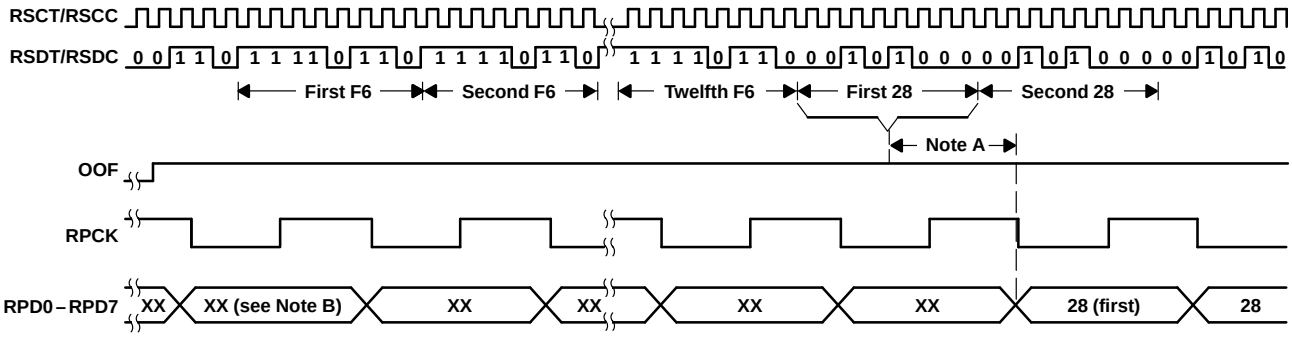
bit alignment

The bit-alignment function of the TNETA1611 is shown in Figure 1.



NOTES: A. After the 12th contiguous F6 is detected, the bit alignment is adjusted so that the next eight bits (the first A2 byte) are grouped together and sent out on RPD0 – RPD7 after some delay time through the device.
B. Even when OOF is high, the TNETA1611 continues to convert the serial input data to parallel output data. While data is present at the output, XX indicates that the alignment of the serial data into bytes on RPD0 – RPD7 may not be known.

Figure 1. Bit Alignment

Terminal Functions

high-speed serial interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RSCT, RSCC	3, 4	I (PECL)	Receive serial clock (true and complement). RSCT and RSCC are a differential 622.08-MHz clock that accompanies the incoming serial data on RSDT and RSDC.
RSDT, RSDC	5, 6	I (PECL)	Receive serial data (true and complement). RSDT and RSDC are differential data that is accompanied by RSCT/RSCC. RSDT and RSDC are valid on the rising edge of RSCT.
TSCT, TSCC	20, 21	O (PECL)	Transmit serial clock (true and complement). TSCT and TSCC are a differential 622.08-MHz clock that accompanies outgoing serial data on TSDT and TSDC.
TSDT, TSDC	16, 17	O (PECL)	Transmit serial data (true and complement). TSDT and TSDC are differential data that is valid on the rising edge of TSCT.
TXHCKT, TXHCKC	23, 24	I (PECL)	Transmit high-speed clock (true and complement). TXHCKT and TXHCKC are a differential 622.08-MHz clock source used when CLKLOOP is low.

control signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKLOOP	29	I (TTL)	Transmit clock-source loop. When CLKLOOP is low, TXHCKT and TXHCKC are used for transmit operations. When CLKLOOP is high, the clock input with the receive data stream is used for transmit operations. This clock is input differentially on RSCT and RSCC.
FLB	30	I (TTL)	Facility loopback. When FLB is high, the receive serial data and clock are looped back to the transmit serial clock and data output.
OE	77	I (TTL)	Output enable. OE enables or disables all TTL outputs. When OE is low, RPCK, RPD0 – RPD7, and TPCK are in the high-impedance state. When OE is high, these terminals function normally.
$\overline{\text{RESET}}$	44	I (TTL)	Reset. The device is reset by taking $\overline{\text{RESET}}$ low. This action can result in the loss of transmit or receive data that is being processed.

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Terminal Functions (Continued)

receive parallel interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
OOF	50	I (TTL)	Out of frame. OOF is generated by subsequent processing elements to control bit alignment in the TNETA1611. When OOF goes high, the TNETA1611 begins a search of the received data for a string of 12 consecutive A1 bytes (i.e., 12 F6s). Once this sequence is found, the TNETA1611 aligns the byte-wide output data with the A1-byte boundaries. The TNETA1611 does not realign the output when the OOF is low.
RPCK	64	O (TTL)	Receive parallel clock. RPCK accompanies the data on RPD0–RPD7 for timing purposes.
RPD0–RPD7	65 – 68, 71 – 74	O (TTL)	Receive parallel (byte-wide) data. RPD0–RPD7 are valid on the rising edge of RPCK.

transmit parallel interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RTNCK	43	I (TTL)	Return clock. RTNCK accompanies data on TPDO–TPD7 such that the data is read into the TNETA1611 on low-to-high transitions of RTNCK. RTNCK can be tied to TPCK if timing requirements between TPCK and TPD0–TPD7 can be met.
TPCK	59	O (TTL)	Transmit clock. TPCK is an output to subsequent processing elements that coordinates data transfers on TPD0–TPD7.
TPD0–TPD7	51 – 58	I (TTL)	Transmit parallel (byte-wide) data. TPD0–TPD7 is read into the TNETA1611 on low-to-high transitions of RTNCK.

miscellaneous signals

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND1	31, 33, 34, 38, 45, 48, 61, 62, 70, 78, 84, 88, 92, 93, 95		Ground. GND1 is the 0-V reference for TTL circuits.
GND2	2, 7, 10, 14, 25		Ground. GND2 is the 0-V reference for PECL circuits.
NC	37, 76, 87		No connection. Leave open.
TEST	11		Manufacturing test. Leave open.
THGND	1, 9, 13, 18, 22, 26, 27, 32, 40, 41, 42, 46, 80, 81, 82, 83, 86, 94, 96, 97, 98, 99, 100		Thermal ground. THGND terminals are used as thermal connections to the board ground plane. There is no electrical connection in the TNETA1611.
V_{CC1}	28, 35, 36 39, 47, 49, 60, 63, 69 75, 79, 85 89, 90, 91		Supply voltage. V_{CC1} is the 5 V ± 5 % supply for TTL circuits.
V_{CC2}	8, 12, 15, 19		Supply voltage. V_{CC2} is the 5 V ± 5 % supply for PECL circuits.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC1}, TTL (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range, V_{CC2}, PECL (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I: TTL . . . . . –1.2 V to 7 V
PECL . . . . . 0 V to V_{CC2}
Operating free-air temperature range, T_A (see Note 2) . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. An external heat sink is required (Wakefield Engineering D10650-40 or equivalent).

recommended operating conditions

			MIN	MAX	UNIT
V_{CC1}	Supply voltage, TTL		4.75	5.25	V
V_{CC2}	Supply voltage, PECL		4.75	5.25	V
V_{IH}	High-level input voltage	TTL	2		V
		PECL (see Note 3)	V_{CC} –1.15	V_{CC} –0.80	
V_{IL}	Low-level input voltage	TTL		0.8	V
		PECL (see Note 3)	V_{CC} –1.90	V_{CC} –1.50	
T_A	Operating free-air temperature (see Note 2)		–40	85	°C

NOTES: 2. An external heat sink is required (Wakefield Engineering D10650-40 or equivalent).
3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_{IK} = – 18 mA			–1.2	V
V_{OH}	High-level output voltage‡	TTL	V_{CC} = 4.75 V, I_{OH} = – 4 mA	4.25			V
		PECL–TSDT, TSDC	V_{CC} = 4.75 V to 5.25 V	V_{CC} –1.03		V_{CC} –0.85	
		PECL–TSCT, TSCC	V_{CC} = 5 V		V_{CC} –1.0		
V_{OL}	Low-level output voltage‡	TTL	V_{CC} = 4.75 V, I_{OL} = 4 mA			0.5	V
		PECL–TSDT, TSDC	V_{CC} = 4.75 V to 5.25 V	V_{CC} –1.85		V_{CC} –1.62	
		PECL–TSCT, TSCC	V_{CC} = 5 V		V_{CC} –1.6		
$V_{O(PP)}$	Output voltage swing, PECL‡	PECL–TSCT, TSCC	V_{CC} = 4.75 V to 5.25 V	400			mV
I_I	Input current	TTL	V_{CC} = 5.25 V, V_I = V_{CC} or GND			±300	µA
I_{IH}	High-level input current	PECL	V_{CC} = 5.25 V, V_I = 4.45 V			25	µA
I_{IL}	Low-level input current	PECL	V_{CC} = 5.25 V, V_I = 3.35 V			±25	µA
I_{CC}	Supply current§		V_{CC} = 5.25 V, I_O = 0				mA
I_{CC}	Supply current‡		V_{CC} = 5.25 V				mA
C_i	Input capacitance	TTL					pF

‡ PECL outputs are terminated with a 50-Ω resistor to V_{CC2} – 2 V.
§ PECL outputs are not terminated.

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timing requirements (see Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{su(RSDT/RSDC)}$	Setup time, RSDT/RSDC valid before RSCT/RSCC↑	500		ps
2	$t_{h(RSDT/RSDC)}$	Hold time, RSDT/RSDC valid after RSCT/RSCC↑	500		ps

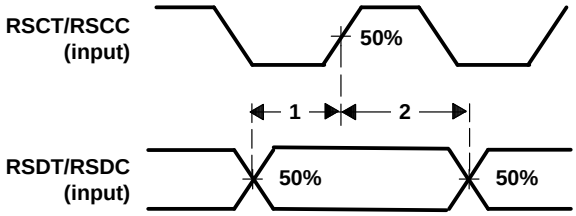

Figure 2. Receive Serial Interface

operating characteristics (see Figure 3)

NO.			MIN	MAX	UNIT
1	t_{csp}	Deviation of clock-sampling point, receive parallel data	– 3.6	3.6	ns

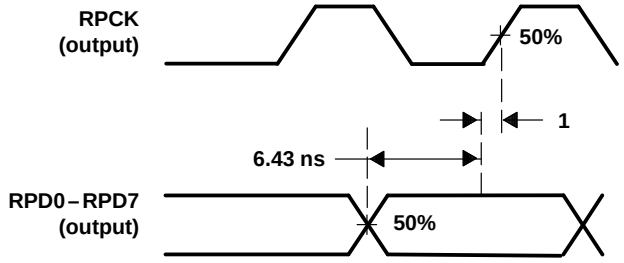

Figure 3. Receive Parallel Interface

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operating characteristics (see Figure 4)

NO.			MIN	MAX	UNIT
1	t_{csp}	Deviation of clock-sampling point, transmit serial data	– 200	200	ps

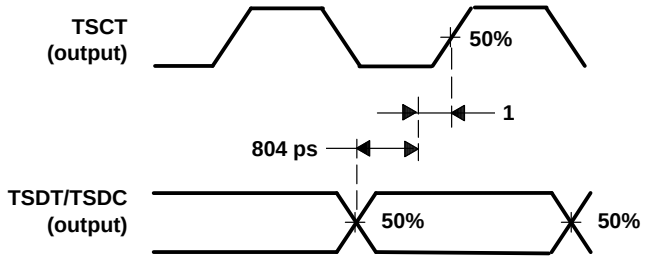

Figure 4. Transmit Serial Interface

timing requirements (see Figure 5)

NO.			MIN	MAX	UNIT
1	t_{csp}	Delay time, TPCK↑ to TPD0–TPD7 valid (RTNCK tied to TPCK)	2	10	ns

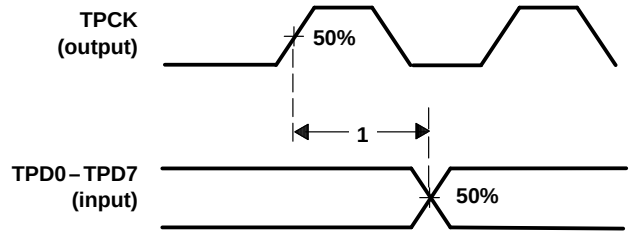

Figure 5. Transmit Parallel Interface

timing requirements (see Figure 6)

NO.			MIN	MAX	UNIT
1	$t_{su(TPD0-TPD7)}$	Setup time, TPD0–TPD7 valid before RTNCK↑	3.6		ns
2	$t_{h(TPD0-TPD7)}$	Hold time, TPD0–TPD7 valid after RTNCK↑	3.6		ns

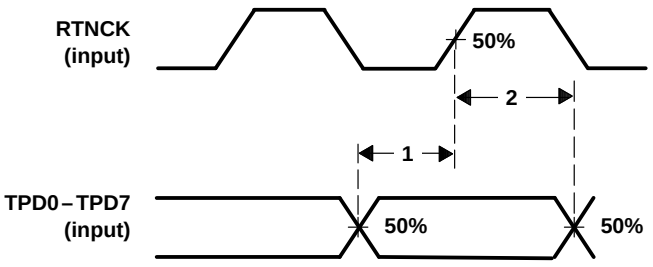

Figure 6. Transmit Parallel Interface Using Return Clock

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