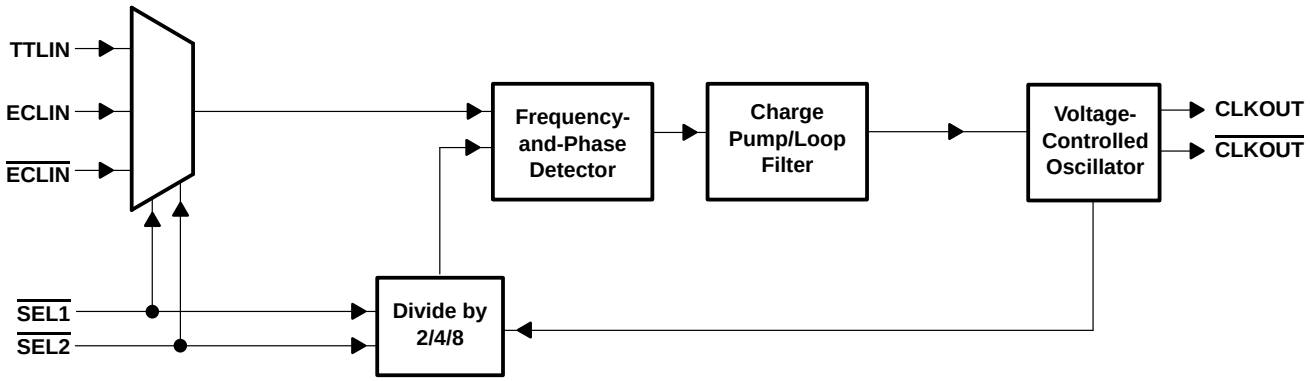
SDNS022B – MARCH 1994 – REVISED JUNE 1995

- **Generates a 155.52-MHz Clock From a TTL Clock of 19.44 MHz**
- **Generates a 155.52-MHz Clock From ECL Clock Signals at 38.88 MHz and 77.76 MHz**
- **Provides Differential ECL Outputs**
- **Clock Frequency Is Selected Via Two Select Inputs**
- **Uses an Internal Third-Order Low-Pass Filter**

description

The TNETA1531 device is a 155.52-MHz clock-generation circuit with the capability of receiving a TTL clock of 19.44 MHz and ECL clock signals at 38.88 MHz and 77.76 MHz. It has differential ECL outputs. The clock frequency can be programmed by using the two select inputs. The TNETA1531 uses an internal third-order low-pass filter to reduce jitter.

functional block diagram†



† TTLIN receives a 19.44-MHz signal. ECLIN and ECLIN receive 38.88-MHz and 77.76-MHz signals.

Terminal Functions

NAME	I/O	DESCRIPTION
TTLIN	I	19.44-MHz TTL input clock
ECLIN	I	38.88/77.76-MHz ECL input clock true
ECLIN	I	38.88/77.76-MHz ECL input clock complement
SEL1	I	Select input for clock frequency
SEL2	I	Select input for clock frequency
CLKOUT	O	155.52-MHz ECL output clock true
CLKOUT	O	155.52-MHz ECL output clock complement

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, TTL . . . . . –1.2 V to 7 V
ECL . . . . . –2.5 V to 0 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under"recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	TTL	2			V
		ECL (see Note 2)	–1.1		–0.8	
V_{IL}	Low-level input voltage	TTL			0.8	V
		ECL (see Note 2)	–1.9		–1.5	
I_{IK}	Input clamp current, TTL				–18	mA
T_A	Operating free-air temperature		–40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage, ECL	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	–1.03	–0.88	V
V_{OL}	Low-level output voltage, ECL	V_{CC} = 4.75 V to 5.25 V,	See Notes 2 and 3	–1.85	–1.62	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_L = –18 mA		–1.2	V
I_I	Input current, TTL	V_{CC} = 5.25 V,	V_I = V_{CC} or GND		–1	µA
I_{IH}	High-level input current, ECL	V_{CC} = 5.25 V,	V_I = –0.88 V		–1.5	mA
I_{IL}	Low-level input current, ECL	V_{CC} = 5.25 V,	V_I = –1.81 V		–2.5	mA
I_{CC}	Supply current	V_{CC} = 5.25 V, Outputs open	f = 155.52 MHz,			mA
		V_{CC} = 5.25 V, See Note 4	f = 155.52 MHz,			

NOTES: 2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.
3. These outputs are terminated to –2 V.
4. These outputs are terminated with a 50-Ω resistor to –2 V.

PRODUCT PREVIEW

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