- **SBus Device That Provides Asynchronous Transfer-Mode Interface**
- **Single-Chip Segmentation and Reassembly (SAR) for Full-Duplex ATM Adaptation-Layer (AAL) Processing**
- **On-Chip SBus Host Interface Allows Use of Host Memory for Packet SAR**
- **53-Byte ATM Cells Are Transparent to the User**
- **Provides Complete Encapsulation and Termination of AAL5 and Limited AAL3/4**
- **Features a Null AAL That Provides Functions for Constant-Bit-Rate Services**
- **Supports 1023 Unique Virtual Circuits (VCs) on Receive Side**
- **Explicit Cell-Level Interleaving Between Groups of VCs**
- **Packet Interface Is Managed by Efficient Descriptor Rings**
- **Physical (PHY)-Layer Interface Is Full Duplex**
- **Supports PHY-Layer Data Rates in the Range of 25.6 Mbit/s to 155.52 Mbit/s**
- **Interfaces Directly to the TNETA1500 SONET ATM BiCMOS Receiver/Transmitter (SABRE)**
- **Recognizes ATM-Layer Operation and Maintenance (OAM) Cells**
- **No External Logic Required for Host Bus to Ensure Simple Design**

description

The TNETA1560 is an asynchronous transfer mode (ATM) segmentation and reassembly (SAR) device with an SBus interface. This device incorporates ATM adaptation-layer (AAL) processing, ATM SAR processing for full-duplex operation up to the STS-3c rate of 155.52 Mbit/s, and the controls for the register interface on the physical (PHY) layer. The device provides a packet interface that is managed by descriptor rings, making the 53-byte ATM-framing format transparent to the user. The device passes the payload of 48 bytes, constituting the payload of each cell, across the SBus-host interface. All packets are segmented and reassembled in host memory and accessed by the chip via the descriptor-ring mechanism. This operation reduces the memory requirements for network-interface cards (NICs). The TNETA1560 requires no local processor on the card, which enables very compact solutions.

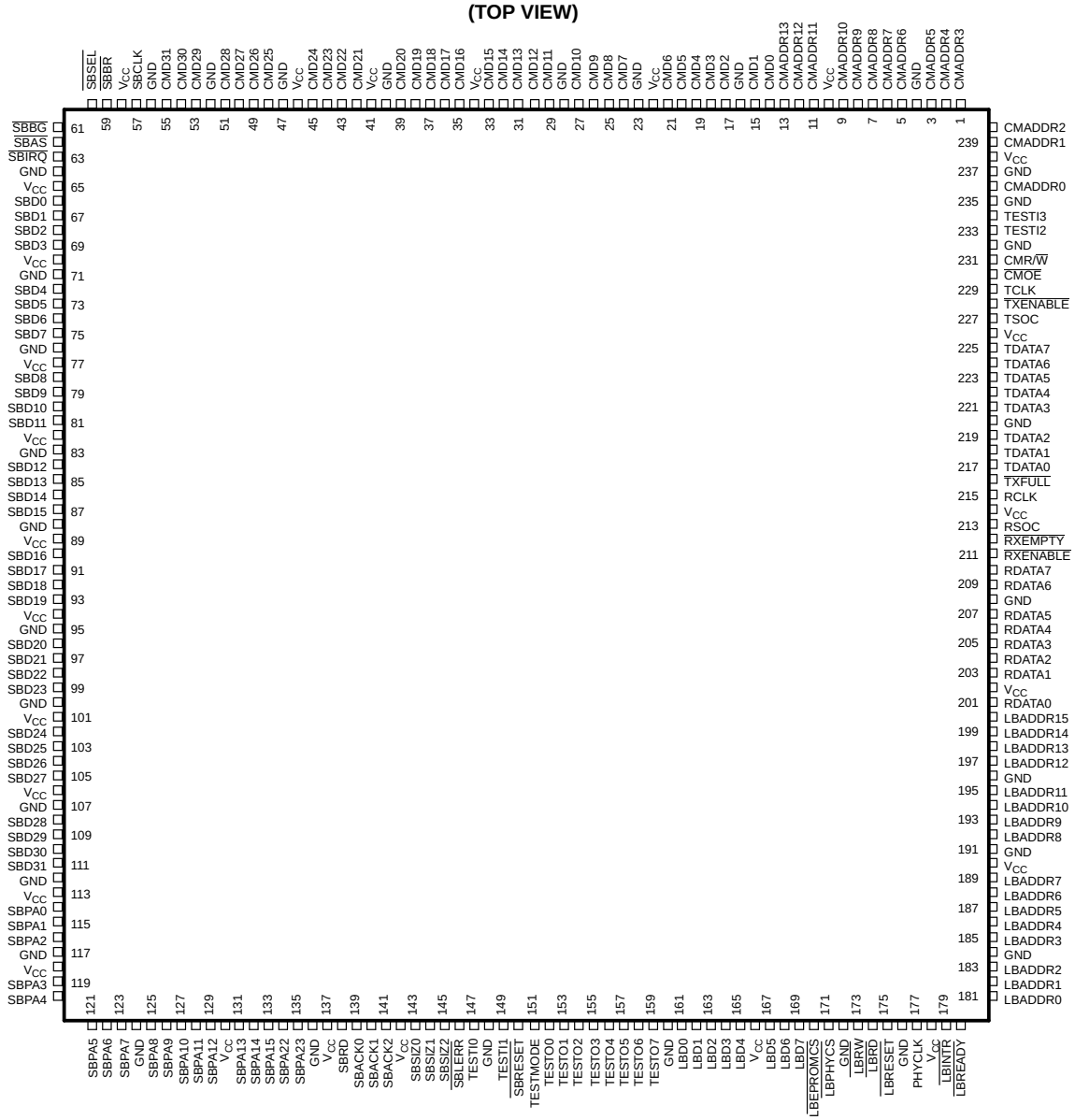
The applications for the TNETA1560 include NICs for client workstations and servers, embedded applications like LAN emulation, and multiprotocol systems like video servers. The TNETA1560 provides complete AAL5 encapsulation and termination in hardware. In addition, limited support is provided for AAL3/4 and a null AAL is provided to facilitate real-time data transfer. The TNETA1560 recognizes ATM-layer operation and maintenance (OAM) cells.

In the transmit direction, the TNETA1560 generates data via a special bit-rate control table that provides explicit cell-level interleaving between groups of virtual circuits (VCs). This mechanism brings a higher degree of flexibility when specifying peak rates for each group (up to 155.52 Mbit/s at a resolution greater than 32 kbit/s). The VCs within a group are serviced via a first-in, first-out (FIFO) discipline on a per-packet basis.

In the receive direction, the TNETA1560 allows multiple virtual paths (VPs) with the condition that each VC is unique. The device is primarily intended for AAL5 encapsulation and termination that is supported in hardware.

The TNETA1560 has four interfaces that include: the SBus interface with a 32-bit-wide data bus, the cell interface, a control-memory interface to access the local SRAM, and the local-bus interface to access the PHY-layer register and an EPROM. The cell interface to the PHY layer consists of an 8-bit-wide data path and associated control signals in both the transmit and receive directions. The 53-byte ATM cells pass between the ATM and PHY layers.

PGC PACKAGE
(TOP VIEW)



description (continued)

The native clock for the TNETA1560 is the SBus clock, which can range between 16.67 MHz and 25 MHz. The native-word size for the device is 32 bits, corresponding to the data width for the SBus. The control-memory interface is 32 bits wide. This interface allows the device to access the local memory to obtain the control information on the packets being segmented and reassembled and to obtain their locations in host memory. Each packet queued for transmission can be distributed across multiple buffers in host memory with each starting at any byte boundary. This is supported in hardware by the device. Every received package is placed in a single buffer in the host memory and is aligned to a 16-byte boundary. The TNETA1560 operation is explained in detail in the Principles of Operation section.

Terminal Functions

SBus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SBACK2–SBACK0	139–141	I/O	SBus acknowledge. SBACK2–SBACK0 are used to indicate SBus word acknowledgement for word operations on the TNETA1560 registers and control memory if set to 011. If set to 101, the SBus byte acknowledgement is for local bus operations. An error acknowledgement is indicated if set to 110. SBACK2–SBACK0 can be driven by the system or by the TNETA1560 in slave mode.
$\overline{\text{SBAS}}$	62	I	SBus address strobe. When $\overline{\text{SBAS}}$ is low, an address is loaded in the TNETA1560.
$\overline{\text{SBBG}}$	61	I	SBus bus grant. $\overline{\text{SBBG}}$ is asserted by the SBus controller to make the TNETA1560 the master.
$\overline{\text{SBBR}}$	59	O	SBus request. $\overline{\text{SBBR}}$ is asserted by the TNETA1560 to request operation as the SBus master.
SBCLK	57	I	SBus clock
SBD31–SBD0	66–69, 72–75, 78–81, 84–87, 90–93, 96–99, 102–105, 108–111	I/O	SBus data bus. SBD31–SBD0 provide access from the host to the contents of the TNETA1560 internal registers.
$\overline{\text{SBIRQ}}$	63	O	SBus interrupt request. $\overline{\text{SBIRQ}}$ is asserted by the TNETA1560 to send an interrupt request to the host.
$\overline{\text{SBLERR}}$	146	I	SBus late error. $\overline{\text{SBLERR}}$ is considered a fatal error. $\overline{\text{SBLERR}}$ causes the TNETA1560 to terminate the ongoing master-bus cycle. If $\overline{\text{SBLERR}}$ is a burst transfer, it completes the burst.
SBPA15–SBPA0	114–116, 119–123, 125–129, 131–133	I	SBus physical address. SBPA15–SBPA0 and SBPA22–SBPA23 provide the address for the host to access the peripheral devices and the TNETA1560 internal registers via SBus slave-mode transactions.
SBPA22–SBPA23	134–135		
$\overline{\text{SBRESET}}$	150	I	SBus reset. $\overline{\text{SBRESET}}$ is active low.
SBRD	138	I/O	SBus read. SBRD can be driven by the system or by the TNETA1560 when SBRD is operating as the master. SBRD indicates a read when high and a write when low.
$\overline{\text{SBSEL}}$	60	I	SBus select. $\overline{\text{SBSEL}}$ is active low and enables the host to access the TNETA1560 device.
SBSIZ2–SBSIZ0	143–145	I/O	SBus data-transfer size signals. SBSIZ2–SBSIZ0 are used to indicate the size of data transfers between the TNETA1560 and the host.

Terminal Functions (Continued)

PHY-layer receive interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
RCLK	215	O	Receive clock. RCLK is equivalent to the internal clock at 19.44 MHz. RCLK is sent to the PHY layer.
RDATA7–RDATA0	201. 203–207, 209–210	I	Receive data. RDATA7–RDATA0 are connected to the PHY-layer receive interface.
RSOC	213	I	Receive start of cell. The PHY layer sends RSOC with the output data.
$\overline{\text{RXEMPTY}}$	212	I	Receive buffer empty in PHY layer. $\overline{\text{RXEMPTY}}$ acts as an inverted enable signal on the PHY-layer receive.
$\overline{\text{RXENABLE}}$	211	O	Receive enable. $\overline{\text{RXENABLE}}$ is always high. For proper operation with a PHY-layer device, leave it open or invert it before going to the PHY layer.

PHY-layer transmit interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TCLK	229	O	Transmit clock. The TNETA1560 generates TCLK at the SBus frequency and sends it to the PHY layer.
TDATA7–TDATA0	217–219, 221–225	O	Transmit data. TDATA7–TDATA0 are sent at the rate of the SBus clock and are driven by the TNETA1560.
TSOC	227	O	Transmit start of cell. TSOC is sent to the PHY layer with the transmit output data and indicates that the first byte of an ATM cell was transmitted to the PHY layer.
$\overline{\text{TXENABLE}}$	228	O	Transmit enable. The TNETA1560 turns off $\overline{\text{TXENABLE}}$ when the PHY layer sends the $\overline{\text{TXFULL}}$ signal.
$\overline{\text{TXFULL}}$	216	I	Transmit buffer full in the PHY layer. The PHY layer asserts $\overline{\text{TXFULL}}$ at least four cycles before any internal buffers are full. This makes the TNETA1560 stop the data transmission to the PHY layer.

control-memory interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CMADDR13–CMADDR0	236 239–240, 1–3, 5–9, 11–13	O	Control-memory address. CMADDR13–CMADDR0 are used to access the data structures in control memory.
CMD31–CMD0	14–15 17–21, 24–27, 29–33, 35–39, 42–45, 48–51, 53–55	I/O	Control-memory data bus. CMD31–CMD0 is a 32-bit data bus. This control-memory interface is designed for 20-ns asynchronous SRAMs. The TNETA1560 uses CMD31–CMD0 to write and read data from its data structures in the control memory.
$\overline{\text{CMOE}}$	230	O	Control-memory output enable. $\overline{\text{CMOE}}$ is an active-low signal.
CMR/$\overline{\text{W}}$	231	O	Control-memory read/write. CMR/$\overline{\text{W}}$ determines a read or write operation. If CMR/$\overline{\text{W}}$ is low, it is a write operation. If CMR/$\overline{\text{W}}$ is high, it is a read operation.

Terminal Functions (Continued)

local-bus interface

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
LBADDR15–LBADDR0	181–183, 185–189, 192–195, 197–200	O	Local-bus address. LBADDR15–LBADDR0 are the lower 16 bits of the SBus address bus and are routed directly to the local-bus-address lines.
LBD7 – LBD0	161–165, 167–169	I/O	Local-bus data. LBD7–LBD0 are used to transfer data to/from local slave devices.
$\overline{\text{LBEPROMCS}}$	170	O	Local-bus EPROM chip-select. $\overline{\text{LBEPROMCS}}$ is an active-low signal.
$\overline{\text{LBINTR}}$	179	I	Local-bus interrupt. $\overline{\text{LBINTR}}$ is generated by a local-bus device.
$\overline{\text{LBPHYCS}}$	171	O	Local-bus PHY-layer chip select. $\overline{\text{LBPHYCS}}$ is used to select PHY-layer devices.
$\overline{\text{LBRD}}$	174	O	Local-bus read. $\overline{\text{LBRD}}$ is an active-low signal that indicates a read operation.
$\overline{\text{LBREADY}}$	180	I	Local-bus-ready. $\overline{\text{LBREADY}}$ is driven by local slave devices. The bus transaction must be completed after eight SBus cycles regardless of $\overline{\text{LBREADY}}$. $\overline{\text{LBREADY}}$ is accepted by the TNETA1560 as a handshake from the devices on the bus.
$\overline{\text{LBRESET}}$	175	O	Local-bus reset output. $\overline{\text{LBRESET}}$ is an active-low signal.
$\overline{\text{LBRW}}$	173	O	Local-bus write. $\overline{\text{LBRW}}$ is an active-low signal that indicates a write operation.

control and configuration

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PHYCLOCK	177	I	PHY-layer clock. PHYCLOCK is a 19.44-MHz clock signal driven by a PHY-layer clock crystal.
TESTI3–TESTI0	147, 149, 233–234	I/O	Test signals. TEST13–TESTI0 are for manufacturer use only. These signals are tied low for normal operation.
TESTMODE	151	I	Test-mode configuration. TESTMODE is tied low for normal operation. TESTMODE is for manufacturer use only.
TESTO7–TESTO0	152–159	I/O	Test signals. TESTO7–TESTO0 are left open for normal operation. TESTO7–TESTO0 are for manufacturer use only.

power and ground

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	4, 16, 23, 28, 40, 47, 52, 56, 64, 71, 76, 83, 88, 95, 100, 107, 112, 117, 124, 136, 148, 160, 172, 176, 184, 191, 196, 208, 220, 232, 235, 237	Ground
V_{CC}	10, 22, 34, 41, 46, 58, 65, 70, 77, 82, 89, 94, 101, 106, 113, 118, 130, 137, 142, 166, 178, 190, 202, 214, 226, 238	Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 6 V
Input voltage range, V_I . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 2) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 3) . . . . . ±20 mA
Operating free air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. Applies for external input and bidirectional buffers
3. Applies for external output and bidirectional buffers

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage	CMOS	V_{CC} = 4.75 V	3.325			V
			V_{CC} = 5.25 V	3.675			
		TTL		2			
V_{IL}	Low-level input voltage	CMOS	V_{CC} = 4.75 V			0.95	V
			V_{CC} = 5.25 V			1.05	
		TTL				0.8	
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 8 mA	V_{CC}–0.8			V
		I_{OL} = 4 mA	V_{CC}–0.8			
V_{OL}	Low-level output voltage	I_{OH} = 8 mA			0.5	V
		I_{OL} = 4 mA			0.5	
I_{OZ}	High-impedance-state output current	V_I = V_{CC} or GND			±10	µA
I_{IL}	Low-level input current	V_I = GND			–1	µA
I_{IH}	High-level input current	V_I = V_{CC}			1	µA
I_{CC}	Supply current	V_{CC} = 5.25 V, f_{clock} (SBCLK) = 25 MHz, Full-duplex operation		250		mA

timing requirements (see Note 4 and Figure 1)

NO.			MIN	MAX	UNIT
1	$t_{w(RCLKH)}$	Pulse duration, RCLK high	12		ns
2	$t_{w(RCLKL)}$	Pulse duration, RCLK low	12		ns
3	$t_{su(RSOC)}$	Setup time, RSOC high before RCLK↑	10		ns
4	$t_{su(RDATA)}$	Setup time, RDATA7–RDATA0 valid before RCLK↑	10		ns
5	$t_{h(RSOC)}$	Hold time, RSOC high after RCLK↑	1		ns

NOTE 4: All output signals are generated on the rising edge of RCLK.

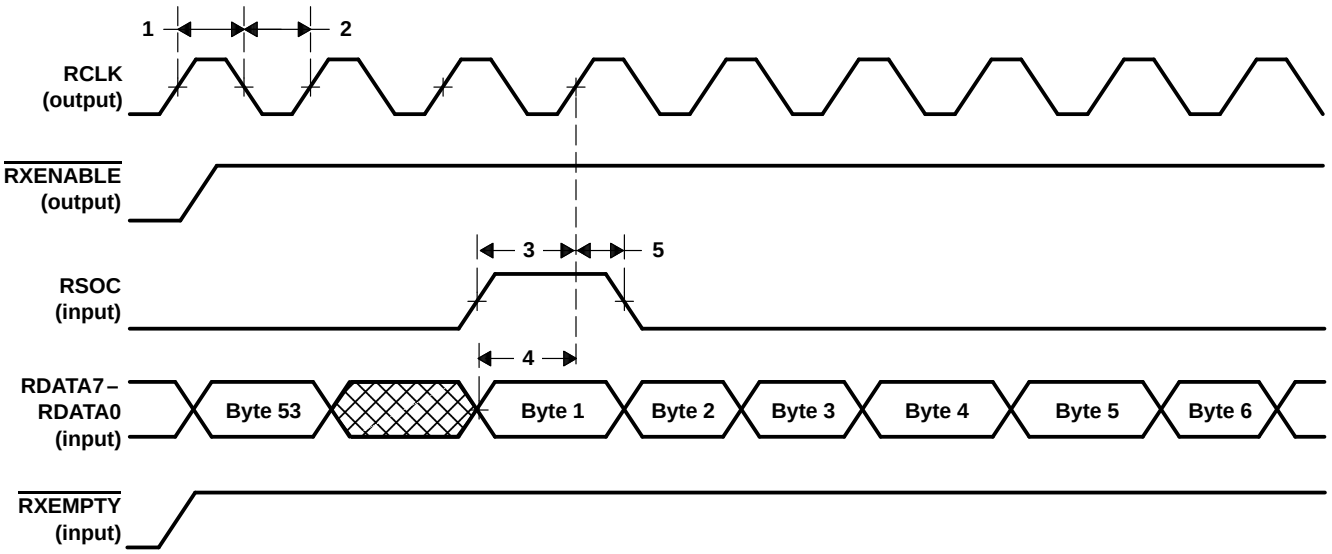


Figure 1. Receive-Cell Interface

timing requirements (see Note 5 and Figure 2)

NO.			MIN	MAX	UNIT
1	$t_{w(TCLKH)}$	Pulse duration, TCLK high	12		ns
2	$t_{w(TCLKL)}$	Pulse duration, TCLK low	12		ns

NOTE 5: All output signals are generated on the rising edge of RCLK. All inputs are sampled on the rising edge of TCLK.

operating characteristics (see Note 5 and Figure 2)

NO.			MIN	MAX	UNIT
3	$t_{d(TXENABLE)}$	Delay time, TCLK↑ to $\overline{\text{TXENABLE}}$↓	1	24	ns
4	$t_{d(TSOC)}$	Delay time, TCLK↑ to TSOC↑	1	24	ns
5	$t_{d(TDATA)}$	Delay time, TCLK↑ to TDATA7 – TDATA0 valid	1	24	ns

NOTE 5: All output signals are generated on the rising edge of RCLK. All inputs are sampled on the rising edge of TCLK.

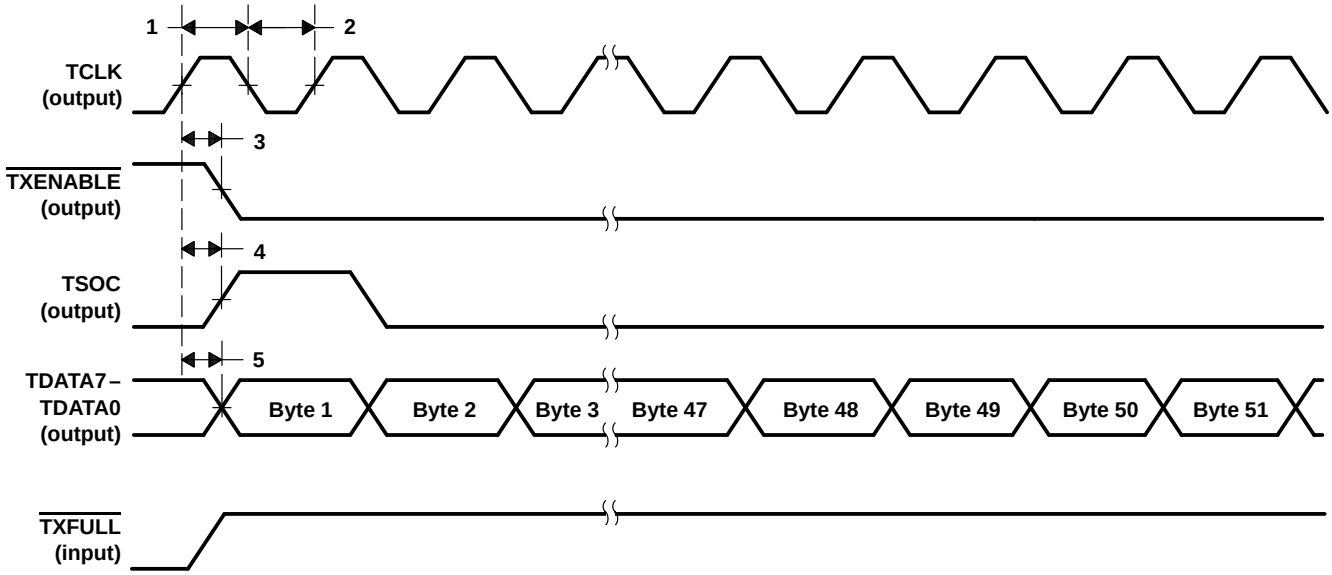


Figure 2. Transmit-Cell Interface

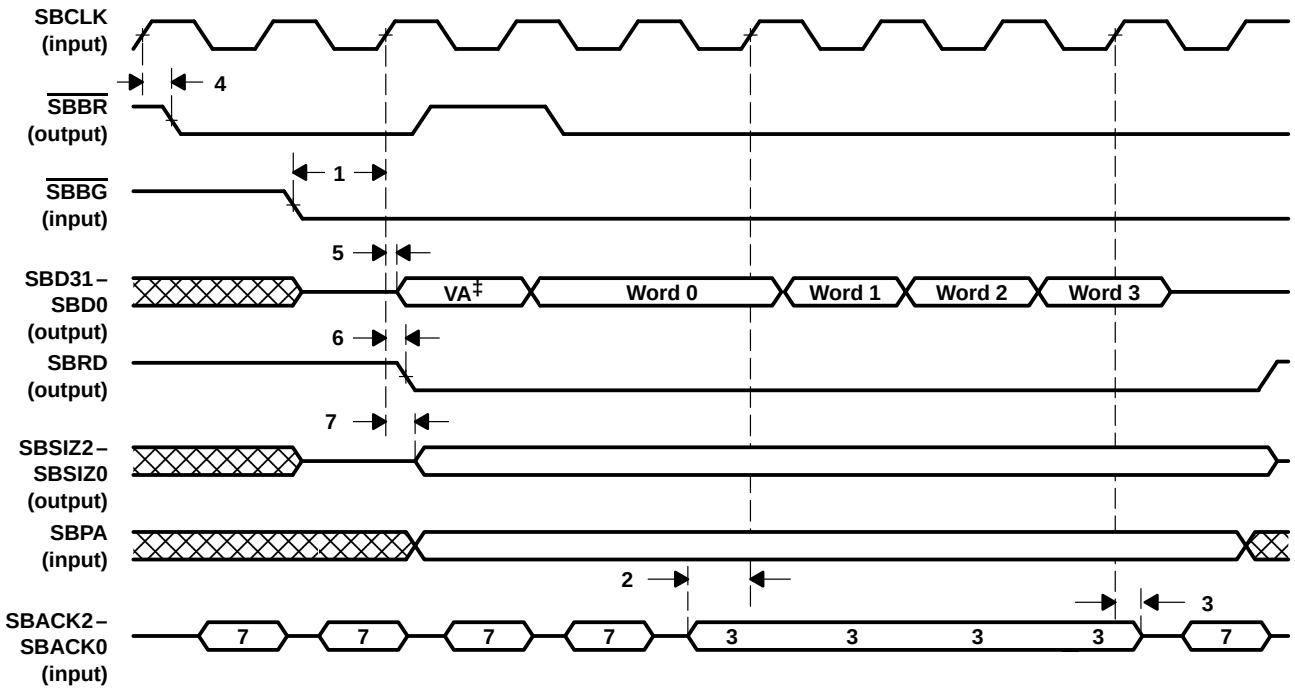
timing requirements (see Figure 3)

NO.			MIN	MAX	UNIT
1	$t_{su(SBBG)}$	Setup time, $\overline{SBBG}$ low before SBCLK↑	15		ns
2	$t_{su(SBACK)}$	Setup time, SBACK2–SBACK0 valid before SBCLK↑	15		ns
3	$t_{h(SBACK)}$	Hold time, SBACK2–SBACK0 valid after SBCLK↑	0		ns

operating characteristics (see Figure 3)

NO.			MIN	MAX	UNIT
4†	$t_{d(SBBR)}$	Delay time, SBCLK↑ to $\overline{SBBR}$↓	2.5	22	ns
5†	$t_{d(SBD)}$	Delay time, SBCLK↑ to SBD31–SBD0 valid	2.5	22	ns
6†	$t_{d(SBRD)}$	Delay time, SBCLK↑ to SBRD↓	2.5	22	ns
7†	$t_{d(SBSIZ)}$	Delay time, SBCLK↑ to SBSIZ2–SBSIZ0 valid	2.5	22	ns

† The values are given for operation with a 25-MHz SBus clock.



‡ VA = Virtual address

Figure 3. TNETA1560 Write Operation (TNETA1560 as Master in This Burst Operation)

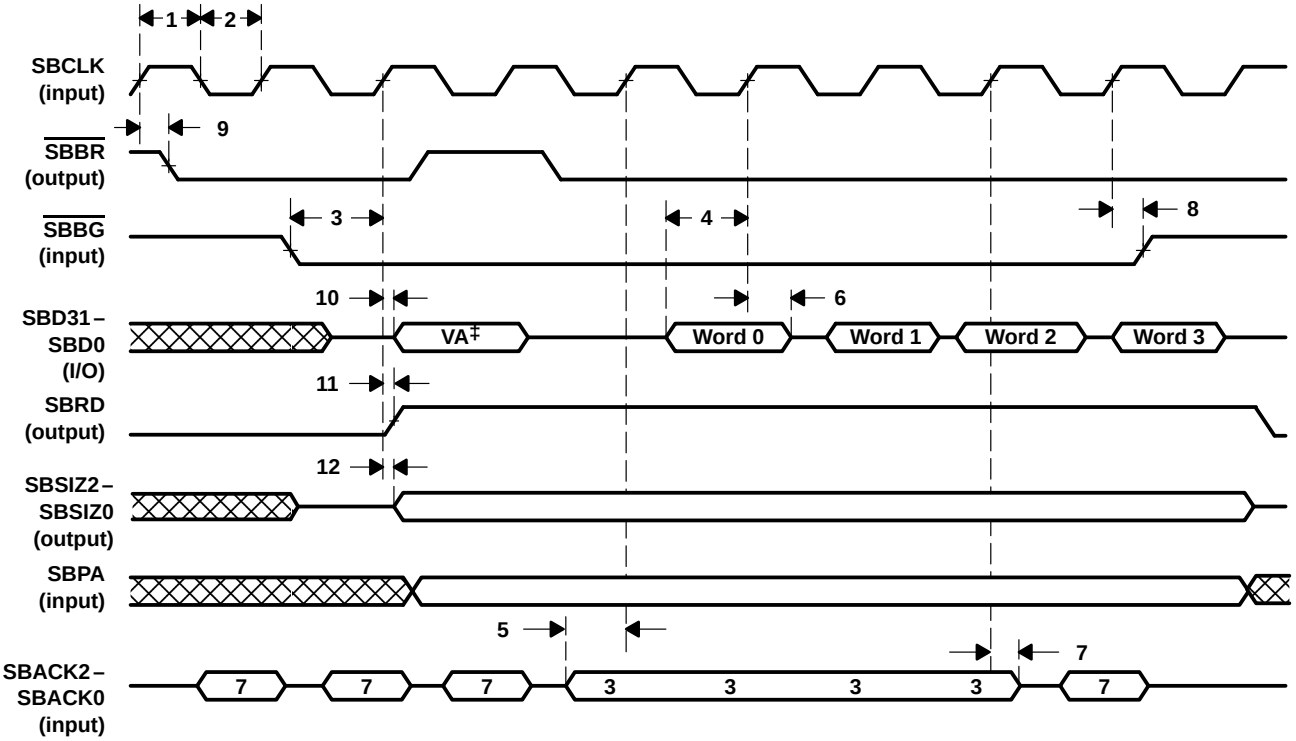
timing requirements (see Figure 4)

NO.			MIN	MAX	UNIT
1	$t_{w(SBCLKH)}$	Pulse duration, SBCLK high	17		ns
2	$t_{w(SBCLKL)}$	Pulse duration, SBCLK low	17		ns
3	$t_{su(SBBG)}$	Setup time, $\overline{SBBG}$ low before SBCLK↑	15		ns
4	$t_{su(SBD)}$	Setup time, SBD31–SBD0 valid before SBCLK↑	15		ns
5	$t_{su(SBACK)}$	Setup time, SBACK2–SBACK0 valid before SBCLK↑	15		ns
6	$t_{h(SBD)}$	Hold time, SBD31–SBD0 valid after SBCLK↑	4		ns
7	$t_{h(SBACK)}$	Hold time, SBACK2–SBACK0 valid after SBCLK↑	1		ns
8	$t_{h(SBBG)}$	Hold time, $\overline{SBBG}$ low after SBCLK↑	2		ns

operating characteristics (see Figure 4)

NO.			MIN	MAX	UNIT
9†	$t_{d(SBBR)}$	Delay time, SBCLK↑ to $\overline{SBBR}$↓	2.5	22	ns
10†	$t_{d(SBD)}$	Delay time, SBCLK↑ to SBD31–SBD0 valid	2.5	22	ns
11†	$t_{d(SBRD)}$	Delay time, SBCLK↑ to SBRD↑	2.5	22	ns
12†	$t_{d(SBSIZ)}$	Delay time, SBCLK↑ to SBSIZ2–SBSIZ0 valid	2.5	22	ns

† The values are given for operation with a 25-MHz SBus clock.



‡ VA = Virtual address

Figure 4. TNETA1560 Read Operation (TNETA1560 as Master in This Burst Transfer)

timing requirements (see Figure 5)

NO.			MIN	MAX	UNIT
1	$t_{su(SBRD)}$	Setup time, SBRD high before SBCLK↑	15		ns
2	$t_{su(SBSIZ)}$	Setup time, SBSIZ2–SBSIZ0 valid before SBCLK↑	15		ns
3	$t_{su(SBPA)}$	Setup time, SBPA valid before SBCLK↑	15		ns
4	$t_{su(SBSEL)}$	Setup time, $\overline{\text{SBSEL}}$ low before SBCLK↑	15		ns
5	$t_{su(SBAS)}$	Setup time, $\overline{\text{SBAS}}$ low before SBCLK↑	15		ns
6	$t_{h(SBPA)}$	Hold time, SBPA valid after SBCLK↑	0		ns
7	$t_{h(SBSEL)}$	Hold time, $\overline{\text{SBSEL}}$ low after SBCLK↑	0		ns

operating characteristics (see Figure 5)

NO.			MIN	MAX	UNIT
8†	$t_{d(SBACK)}$	Delay time, SBCLK↑ to SBACK2–SBACK0 valid	2.5	22	ns
9†	$t_{d(SBD)}$	Delay time, SBCLK↑ to SBD31–SBD0 valid	2.5	22	ns

† The values are given for operation with a 25-MHz SBus clock.

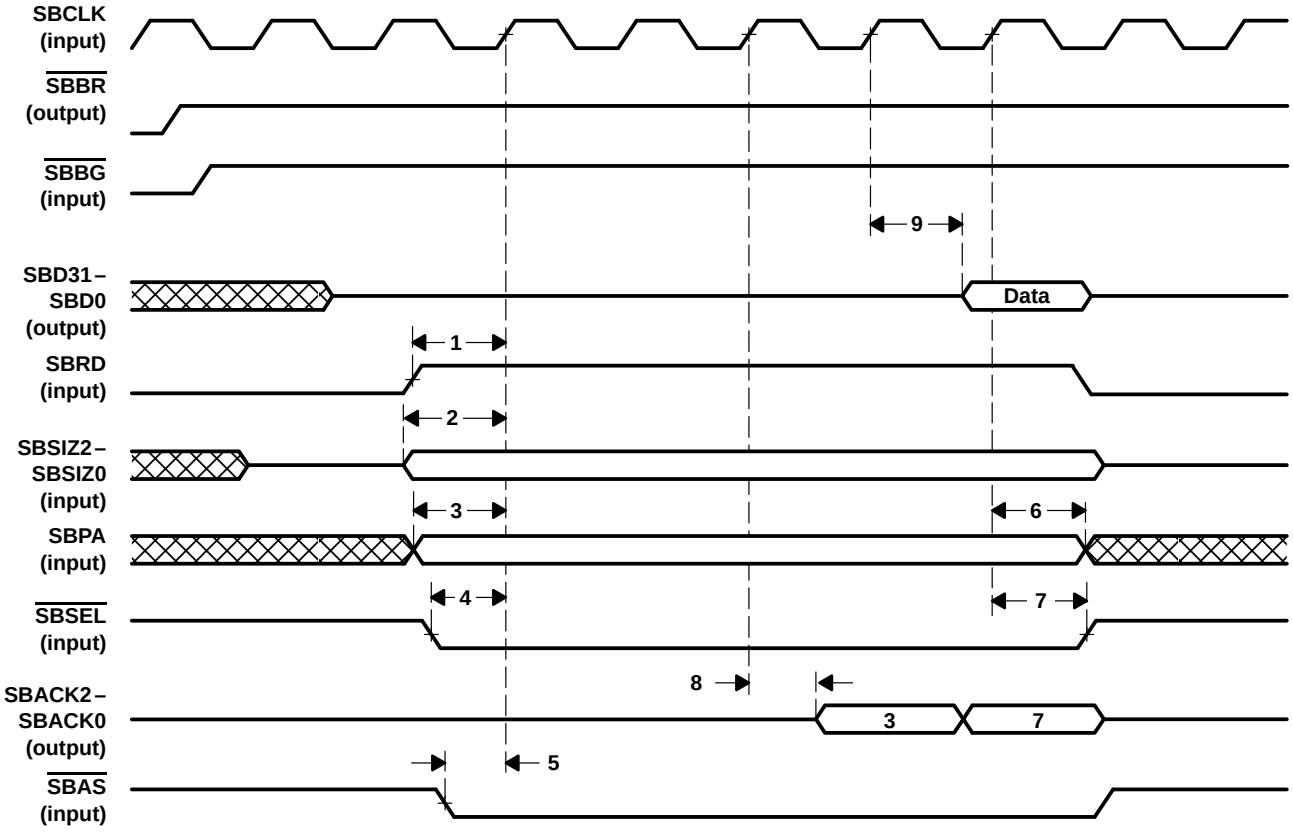


Figure 5. TNETA1560 Read Operation (TNETA1560 as Slave)

timing requirements (see Figure 6)

NO.			MIN	MAX	UNIT
1	$t_{su(SBRD)}$	Setup time, SBRD low before SBCLK↑	15		ns
2	$t_{su(SBSIZ)}$	Setup time, SBSIZ2–SBSIZ0 valid before SBCLK↑	15		ns
3	$t_{su(SBPA)}$	Setup time, SBPA valid before SBCLK↑	15		ns
4	$t_{su(SBSEL)}$	Setup time, $\overline{\text{SBSEL}}$ low before SBCLK↑	15		ns
5	$t_{su(SBAS)}$	Setup time, $\overline{\text{SBAS}}$ low before SBCLK↑	15		ns
6	$t_{su(SBD)}$	Setup time, SBD31–SBD0 valid before SBCLK↑	15		ns
7	$t_{h(SBSEL)}$	Hold time, $\overline{\text{SBSEL}}$ low after SBCLK↑	0		ns
8	$t_{h(SBAS)}$	Hold time, $\overline{\text{SBAS}}$ low after SBCLK↑	1		ns
9	$t_{h(SBPA)}$	Hold time, SBPA valid after SBCLK↑	0		ns
10	$t_{h(SBD)}$	Hold time, SBD31–SBD0 valid after SBCLK↑	4		ns

operating characteristics (see Figure 6)

NO.			MIN	MAX	UNIT
11	$t_{d(SBACK)}$	Delay time, SBCLK↑ to SBACK2–SBACK0 valid	2.5	22	ns

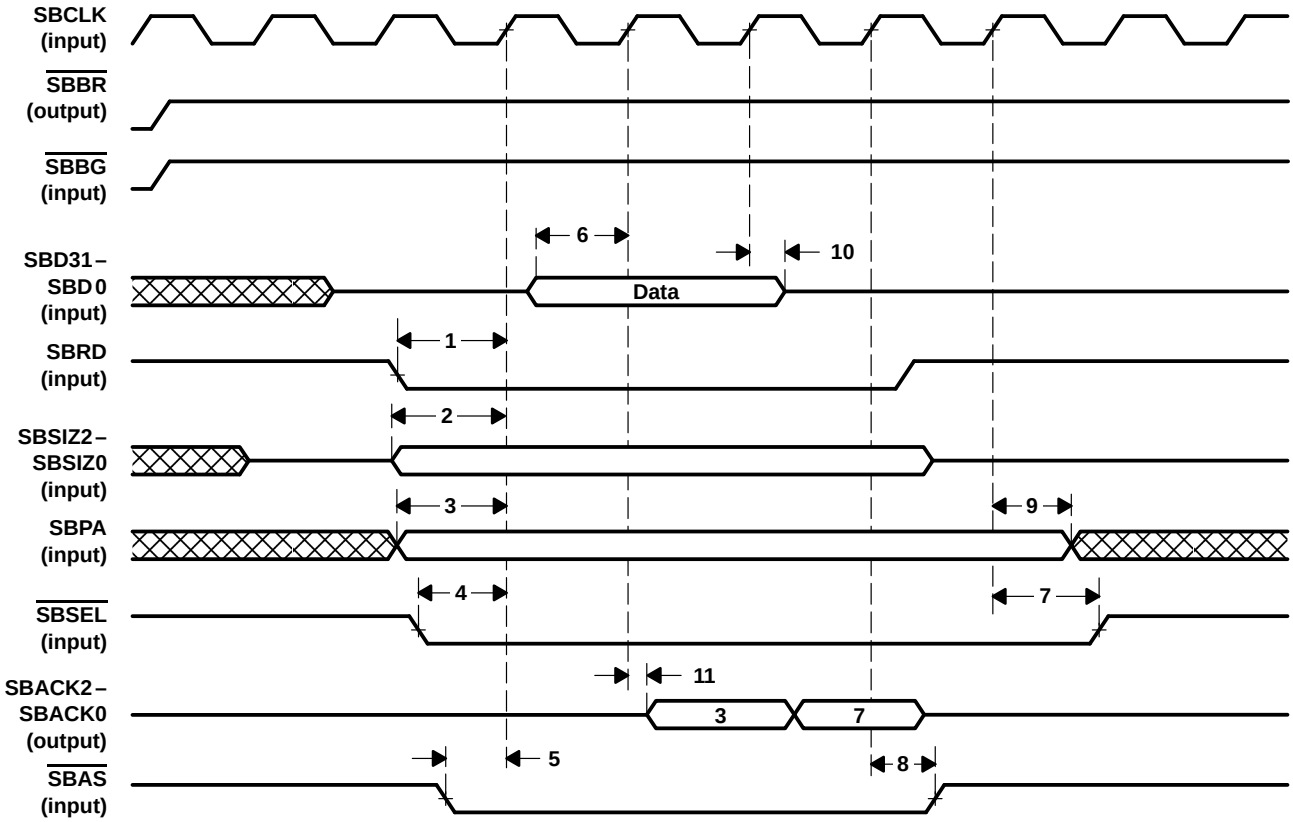


Figure 6. TNETA1560 Write Operation (TNETA1560 as Slave)

operating characteristics (see Note 6 and Figure 7)

NO.			MIN	TYP†	MAX	UNIT
1	$t_{d(LBPHYCS)1}$	Delay time, $\overline{\text{LBRD}}\downarrow$ to $\overline{\text{LBPHYCS}}\downarrow$		40		ns
2	$t_{d(LBPHYCS)2}$	Delay time, $\overline{\text{LBREADY}}\downarrow$ to $\overline{\text{LBPHYCS}}\uparrow$		120		ns

† The typical values are given for operation with a 25-MHz SBus clock.

NOTE 6: If $\overline{\text{LBREADY}}$ does not go active low within eight SBus clocks after $\overline{\text{LBPHYCS}}$ goes active low, TNETA1560 latches in the data on the LBD7–LBD0 bus and terminates the read operation.

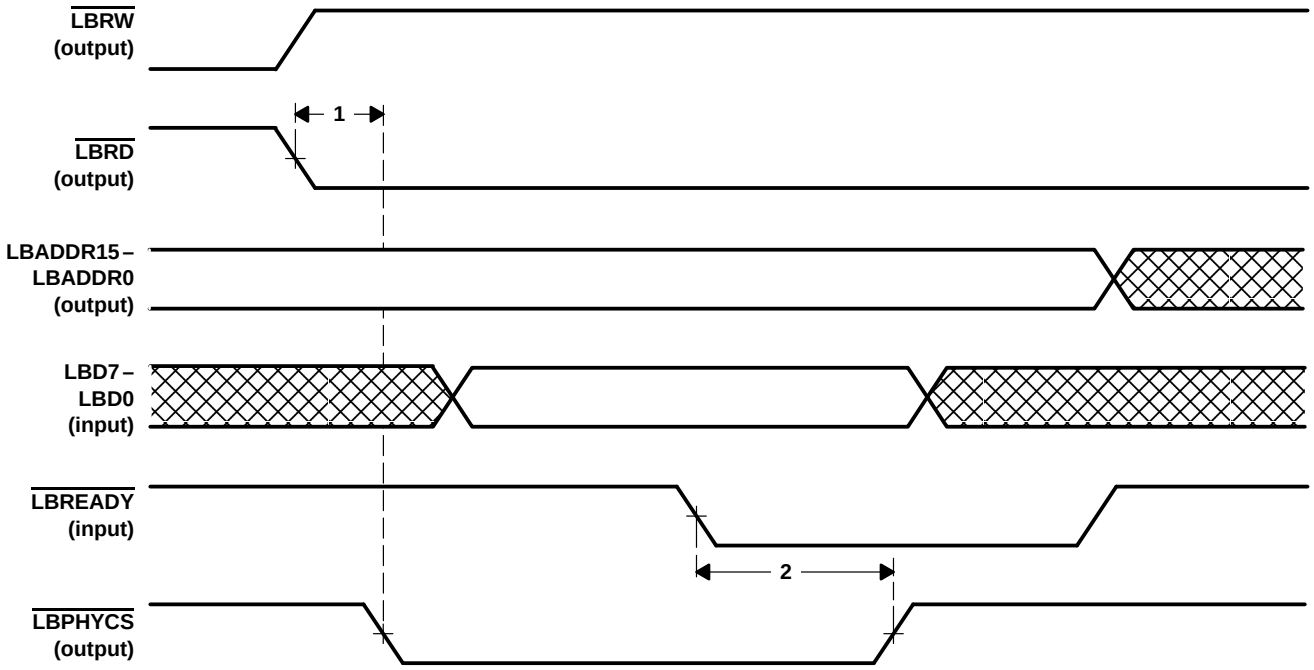


Figure 7. Local-Bus-Interface Read Operation (TNETA1560 as Slave)

operating characteristics (see Figure 8)

NO.			MIN	TYP†	MAX	UNIT
1	$t_{d(LBPHYCS)1}$	Delay time, $\overline{LBRW}\downarrow$ to $\overline{LBPHYCS}\downarrow$		40		ns
2	$t_{d(LBPHYCS)2}$	Delay time, LBADDR15–LBADDR0 valid to $\overline{LBPHYCS}\downarrow$		160		ns
3	$t_{d(LBPHYCS)3}$	Delay time, LBD7–LBD0 valid to $\overline{LBPHYCS}\downarrow$		40		ns
4	$t_{d(LBADDR)}$	Delay time, $\overline{LBPHYCS}\uparrow$ to LBADDR15–LBADDR0 invalid		126		ns

† The typical values are given for operation with a 25-MHz SBus clock.

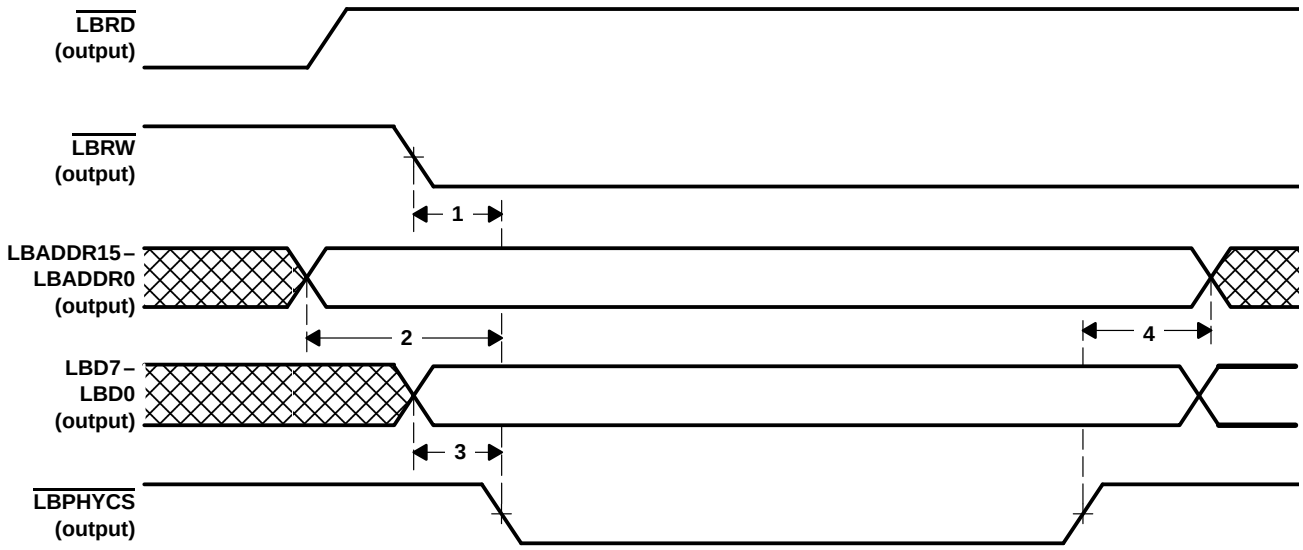


Figure 8. Local-Bus-Interface Write Operation (TNETA1560 as Slave)

operating characteristics (see Figure 9)

NO.			MIN	TYP†	MAX	UNIT
1	$t_{w(CMR/WL)}$	Pulse duration, CMR/$\overline{W}$ low		40		ns
2	$t_{d(CMR/W)1}$	Delay time, CMADDR13–CMADDR0 valid to CMR/$\overline{W}\downarrow$		20		ns
3	$t_{d(CMR/W)2}$	Delay time, CMD31–CMD0 valid to CMR/$\overline{W}\uparrow$		60		ns
4	$t_{d(CMD)}$	Delay time, CMR/$\overline{W}\uparrow$ to CMD31–CMD0 invalid		20		ns

† The typical values are given for operation with a 25-MHz SBus clock.

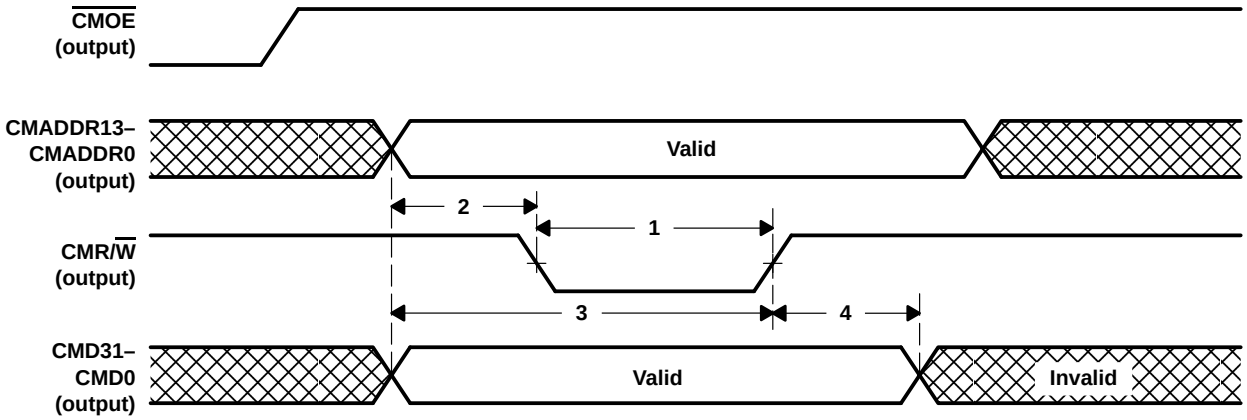


Figure 9. Control-Memory-Interface Write Operation

timing requirements (see Figure 10)

NO.			MIN‡	MAX	UNIT
1	$t_{su(CMD)}$	Setup time, CMD31–CMD0 valid before $\overline{CMOE}\uparrow$	9		ns
2	$t_{h(CMD)}$	Hold time, CMD31–CMD0 valid after $\overline{CMOE}\uparrow$	2		ns

‡ These values are given for operation with a 25-MHz SBus clock.

operating characteristics (see Figure 10)

NO.			MIN	TYP†	MAX	UNIT
3	$t_{d(CMOE)}$	Delay time, CMADDR13–CMADDR0 valid to $\overline{CMOE}\downarrow$		1		ns

† The typical values are given for operation with a 25-MHz SBus clock.

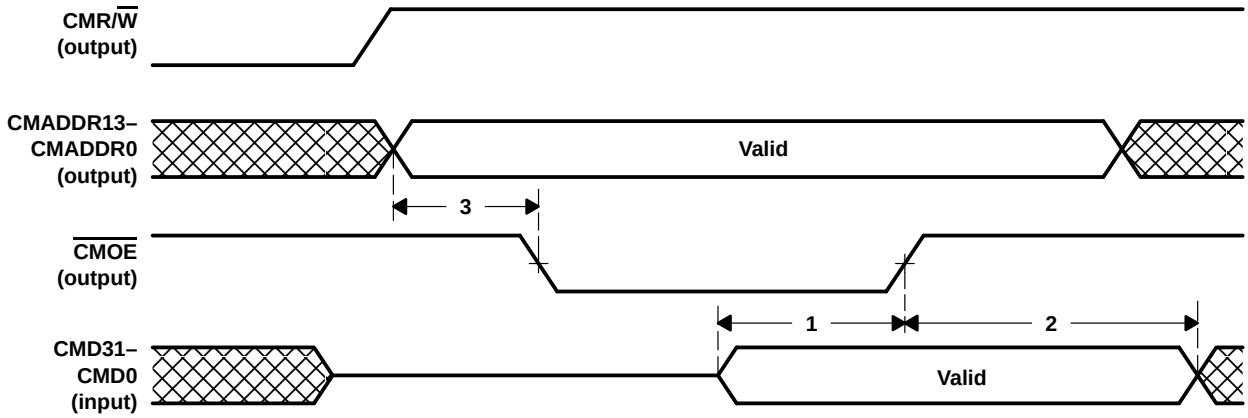


Figure 10. Control-Memory-Interface Read Operation

PRINCIPLES OF OPERATION

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functional overview

The SBus SAR refers to an SBus device (TNETA1560) that provides an ATM interface. The device provides an interface to SBus, ATM adaptation-layer processing, ATM SAR processing for full-duplex ATM at the STS-3c rate of 155.52 Mbit/s, and the controls for the register interface on the physical (PHY) layer. Figure 11 shows a typical connection to the SBus SAR in an adaptor-card application.

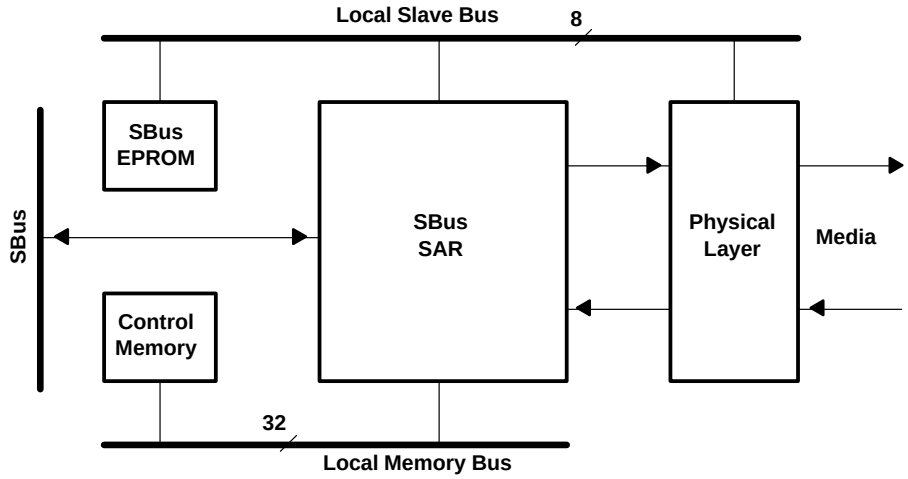

Figure 11. SBus SAR External Connections

The SBus SAR provides a packet interface managed by descriptor rings, making the 53-byte ATM framing format transparent to the user. The device passes the 48-byte payload of each cell across the SBus. All packets are stored in host memory and accessed by the chip via the descriptor-ring mechanism.

The SBus SAR generates data in the transmit direction via a special bit-rate control table that provides explicit cell-level interleaving between groups of VCs. This mechanism provides a high degree of flexibility in specifying peak rates for each group, up to 155.52 Mbit/s at a resolution greater than 32 kbit/s. The VCs within a group are serviced via a FIFO discipline on a per-packet basis.

The SBus SAR supports 1023 unique VCs, typically all associated with virtual path identifier (VPI) 0. The SBus SAR allows multiple VPs with the caveat that each VC is unique. Limited support is provided to recognize ATM-layer OAM cells.

The device is primarily intended for ATM adaptation-layer type 5 (AAL5) encapsulation and termination, which is fully supported in hardware. Limited support is provided for ATM adaptation-layer type 3/4 (AAL3/4) with 48-byte transfers across the SBus interface and hardware recognition of the EOM indicator on the receive side. Finally, a null AAL is also supported to facilitate real-time data transfer.

The interface to the PHY layer consists of an 8-bit-wide data path and associated control signals in both the transmit and receive directions. The 53-byte ATM cells pass between the ATM and PHY layers.

functional overview (continued)

The native clock for the SBus SAR is the SBus clock, which can range between 16.67 MHz and 25 MHz. The 8-bit-wide data path on the PHY-layer receive interface requires a clock rate of at least 19.44 MHz when interacting with a 155.52 Mbit/s PHY-layer. The PHY-layer receive interface uses the the PHY-layer clock. The native-word size for the device is 32 bits, corresponding to the data-bus width for SBus.

glossary and conventions

This section presents several special terms and conventions used throughout this document. It is not a complete list of abbreviations.

transmit direction

The direction of data flow from SBus to the ATM PHY layer

receive direction

The direction of data flow from ATM PHY-layer to SBus

two's-complement value

A number in two's complement is given by (0 – actual positive value) modulo (2^n), where n is the number of bits in the field.

GFC

Generic flow control field. Appears in the upper four bits of the ATM cell header at the UNI.

EOM

End of message

EOP

End of packet

NCE

Network control engine

functional description

packet interface

The SBus SAR uses host memory to store the 48-byte payload units that constitute a packet in both the transmit and receive directions. The device initiates the 48-byte data transfers containing packet data over the SBus for both transmit and receive operations. The packet does not include AAL5 encapsulation while in host memory. This is provided by the SBus SAR. The buffering within the device is limited to that required to match the ATM-PHY transfer protocol to the transaction-oriented SBus transfer protocol. The chip contains an 8-cell transmit FIFO and a 32-cell receive FIFO.

Each packet queued for transmission may be distributed across multiple buffers in host memory with each starting at any byte boundary. This is supported in hardware by the device. Each received packet is placed in a single buffer in host memory (either small or big) aligned to a 16-byte boundary.

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bandwidth group (BWG) table mechanism

The SAR generates data via a special bit-rate control table known as the BWG table (see Figure 12). The BWG table consists of up to 4800 entries and each entry consists of an 8-bit BWG index. The table is organized with 1200 words in control memory. The size is programmable via the BWG-size register. Since each BWG index corresponds to a transmit direct-memory access (DMA) channel, the TNETA1560 can support 255 (8-bit Index) transmit DMA channels simultaneously. The SAR cycles through the table and sends an ATM cell for the transmit DMA channel for each entry in the table. If a zero value is entered for a BWG index, an idle cell is transmitted. The BWG table is used to assign the transmit-side bandwidth. The total available bandwidth for an OC3c SONET link is 135.63 Mbit/s (155.52 Mbit/s less SONET and ATM overhead). The granularity is obtained by dividing the SONET-link bit rate (135.63 Mbit/s) by the entries in the BWG table (4800). Thus, an application requiring 500 kbit/s requires 19 entries in the table.

500 kbit/s/28250 bit/s per entry = 19 required entries in the table.

If the application uses the transmit descriptor ring 5, there will be 19 entries, with 5 as the BWG index in the BWG table shown in Figure 12.

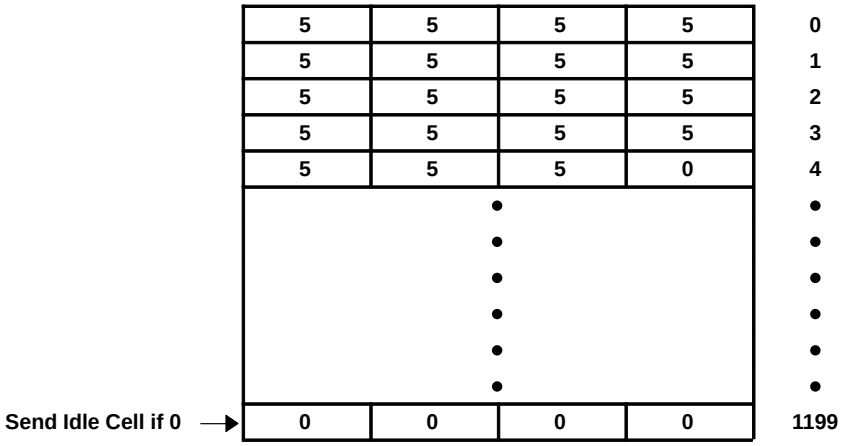

Figure 12. BWG Table

AAL-type processing

The SBus SAR supports various types of AAL processing. AAL3/4, AAL5, null-AAL, GFC, and OAM processing are described in this section.

AAL3/4 processing

Since 48 bytes are provided across the SBus interface, all AAL3/4 packet data processing is performed by the host in software. AAL5 processing is disabled on VCIs using AAL3/4. The AAL3/4 EOM indicator, which is located in the first byte of the ATM payload (see Figure 13), is recognized in hardware, initiating an interrupt to the host.

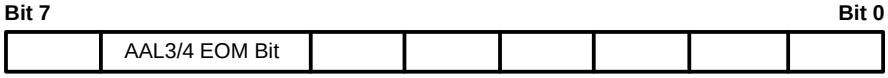

Figure 13. AAL3/4 Processing

PRINCIPLES OF OPERATION

AAL5 processing

The primary support is for AAL5 with encapsulation in the transmit direction and termination in the receive direction. The AAL5 packets are converted to cells by the SBus SAR before delivery to the PHY layer. Similarly, the device recovers 53-byte ATM cells from the PHY layer before it performs AAL5 termination.

The SBus SAR adds the pad, the control/length field, and the cyclic redundancy check (CRC) for transmit packets. The SBus SAR does not interpret the field length in the AAL5 frame in the receive direction; therefore, the entire AAL5 packet is forwarded to host memory allowing the driver to remove the correct payload. This also allows the host to examine the control field in software, necessary in a time of evolving standards in this area. The device performs CRC checks in the receive direction and indicates EOP processing to the host based on the EOP indication in AAL5.

null-AAL processing

Null-AAL processing uses the same mechanism as the AAL3/4 in the transmit direction to disable AAL5 processing. The control entry associated with each BWG (VCI) in the receive direction has an entry to indicate an interval defined in units of cells received. The SBus SAR then provides an interrupt to the host when the number of cells received on the VCI is equal to that indicated by the table entry. This counter is reset after each interrupt (at the end of each interval). This interval is also referred to as a packet, although it does not encapsulate a well-defined unit of information.

high-order VPI/VCI bits GFC processing

The lower ten bits of the VCI are used to encode the 1023 possible VCIs. VCI 0 is not used since it indicates unassigned cells. The upper-order bits of the VCI and the VPI field are programmable on a per-VC basis on transmit. The GFC field is always set to zero.

The upper-order bits of the VCI, the VPI field, and the GFC field are ignored on all cells that are received. These cells pass to the SBus SAR if the header-error-control (HEC) field is correct, the upper-order bits of the header are set intentionally, or the cell is misrouted. The probability of misrouting is small and such an event would be detected via the CRC check in AAL5. The advantage of this scheme is that any VPI/VCI combination is supported if the lower ten bits of the VCI are unique.

OAM processing

The ATM-layer OAM processing does not require any real-time intervention and is processed in software. OAM cells received on the link must be identified by the device. Table 1 summarizes ATM-layer OAM encoding as described by various standards bodies.

Table 1. ATM-Layer OAM Encoding

NO.	ITEM	VCI	PTI
1	VP level: link-associated OAM cell	3	—
2	VP level: end-to-end OAM cell	4	—
3	VC level: link-associated OAM cell	Any	4
4	VC level: end-to-end OAM cell	Any	5

Each OAM cell forms a fully encapsulated packet. The ATM-layer OAM cells transcend AAL protocols and are recognized differently. The end system recognizes all four ATM-layer OAM flows. OAM cells received in VCI 3 and 4 do not interfere with the normal data stream. The only special processing necessary is to initiate EOP processing for each cell. The software drivers must configure VCI 3 and 4 as null-AAL channels with a packet length equal to one cell in the receive direction. OAM cells are transmitted as null-AAL packets with length equal to one cell. VC-level OAM cells are specially interpreted. They are diverted to receive direct-memory access (DMA) channel 0 and the 4-byte ATM header is passed on to a receive completion ring in host memory during normal EOP processing.

PRINCIPLES OF OPERATION

transmit descriptor rings and DMA

Each transmit BWG is supported by a corresponding DMA channel and its own descriptor ring. The SBus SAR supports 255 BWGs, 255 descriptor rings, and 255 DMA channels in the transmit direction. BWG 0 represents null, indicating that an idle cell should be transmitted. This limits the number of packets and VCs active simultaneously in the transmit direction to 255.

Each descriptor ring holds up to 256 entries corresponding to 256 buffers that may be queued for transmission in the ring. The total number of buffers that can be queued for transmission by the device is 64K. The buffers within a descriptor ring (each BWG) are serviced in FIFO order on a per-buffer basis. Each packet consists of one or more byte-aligned buffers in host memory.

Each descriptor-ring entry contains a control bit that indicates whether a buffer is queued for transmission. The DMA entry for each BWG contains a pointer to the first item in the queue in the corresponding descriptor ring. An idle cell is transmitted if the control bit in the next entry of the descriptor ring indicates an inactive entry.

A field in each DMA entry allows the BWG to be disabled by the host. This may be used by the host to respond to back-pressure mechanisms in software.

receive free-buffer rings and DMA

The SBus SAR uses buffer pointers from two free-buffer rings to place incoming packets in the host memory. These are called small free-buffer ring and the big free-buffer ring. Each receive BWG has a control bit indicating the type of buffer it uses: small or big. BWGs are unable to preallocate buffers for the next packet, which prevents user processes from managing their own buffer space.

The SBus SAR supports 1023 receive DMA channels and 1023 VCs. The incoming VCI indexes the receive DMA channels directly. BWG 0 is reserved to process special information for OAM cells. The drivers must configure VCI 0 as a null-AAL VCI with a packet length equal to one cell.

completion rings

The SBus SAR indicates completion of packet processing in either direction to the host via an interrupt and by posting entries to receive- and transmit-completion rings. Each completion ring accepts up to 256 entries. A control bit in each entry of the completion ring prevents the device from overwriting an entry that has not been processed by the host.

packet-size restrictions

The SBus SAR supports a maximum packet size of 64K bytes in either direction. The maximum buffer size for transmit is also 64K bytes.

SBus interaction and burst-transfer size requirements

The SBus SAR behaves both as an SBus direct virtual memory access (DVMA) master and as a slave. Table 2 classifies the interaction between the device and SBus into seven groups. This also quantifies the support required from the DMA controller on the host machine.

PRINCIPLES OF OPERATION

Table 2. SBus Transactions

NO.	TRANSACTION TYPE	SAR ROLE	TRANSFER SIZE	ACK. SIZE
1	Host accesses SAR registers or control memory	Slave	Word	Word
2	Host accesses PHY-layer registers	Slave	Word	Word
3	Host accesses EPROM	Slave	Byte/Word	Byte
4	SAR transmits control-information transactions and receives free-buffer ring transactions	Master	Word	Word
5	SAR receive completion-ring entries posted to the host	Master	4 Word	4 Word
6	SAR cell-payload transfers (default)	Master	8, 4, and 1 Word	8, 4, and 1 Word
7	SAR cell-payload transfers (NCE)	Master	4 Word	4 Word

It is efficient to transfer the 48-byte payload via successive transfers of 32 and 16 bytes if the data is on even burst boundaries. This is the algorithm followed by the SAR in the default mode for all transfers on receive and for all transfers on transmit except those on buffer boundaries.

The NCE is based on a SPARC station 1+ platform that does not support 32-byte bursts. A configuration register bit on the SBus SAR programmed by the host is set to indicate that the platform is the NCE or any system that does not support 32-byte bursts. The device then uses 16-byte bursts exclusively to transfer cell-payload data in each direction.

Since there is at least a 4-cycle overhead associated with each transfer for a DVMA master, the number of cycles required to transfer a cell in the default mode in either direction with no overhead for packet processing is at least 20 SBus cycles. The time to transfer the 48-byte cell payload on the NCE in either direction is at least 24 SBus cycles.

SBus interaction and burst-transfer size requirements (continued)

Burst transfers in the transmit direction are optimized to yield the fewest SBus cycles based on buffer, packet, cell boundaries, and their location in host memory.

commands, registers, and interrupts

The SBus SAR has several internal registers for configuration and storage of operational-state information. The information contained in the registers is described in a later section.

The SAR generates an interrupt, connected on the adapter to $\overline{\text{SBIRQ}}$, on packet completion and on a variety of error conditions.

PHY data interface

The ATM-cell-transfer rate is full-duplex 149.76 Mbit/s, but data may arrive in bursts at 155.52 Mbit/s due to the framing scheme described by the PHY layer. A clock rate of at least 19.44 MHz is essential in the receive direction to prevent cell loss due to buffer overflow in the PHY layer. The SBus SAR decouples the SBus clock from the ATM clock in the receive direction via an asynchronous FIFO memory, which holds up to 32 cells. The SAR transmits data to the PHY layer at the SBus clock rate.

PHY-layer control interface

Figure 11 shows that the local bus is used to connect the SBus EPROM to the register interface on the PHY-layer device.

PRINCIPLES OF OPERATION

interfaces

The terminal layout and the terminal functions table fully describe the terminal assignments and functions of the Sbus SAR (TNETA1560).

SBus interface

The SBus SAR behaves both as an SBus DVMA master and slave. The SBus SAR is selected as the slave if the $\overline{\text{SBSEL}}$ signal is asserted. The system accesses the control-memory block, the local bus, and the user registers with SBus slave accesses to the SAR. The transfer size is determined by SBSIZ2–SBSIZ0, which must be set to 000 to represent a 1-word transfer. The physical address is given by the SBPA signals and must fall within the ranges specified in Tables 4 and 13. The SBus SAR generates an error acknowledgment given by SBACK2–SBACK0 set to 110 if either of these two conditions is violated. The $\overline{\text{SBAS}}$ signal is used as described in the SBus specification, and the SBRD signal indicates a read or write operation. Finally, SBACK2–SBACK0 are set to 011 to indicate SBus word acknowledgment for operations on the SAR registers and control memory; SBACK2–SBACK0 are set to 101 to indicate SBus byte acknowledgment on host accesses to the EPROM via the local bus.

The SBus SAR can initiate transactions as master only when no slave transactions are active. The SAR asserts the dedicated $\overline{\text{SBBR}}$ signal to request an operation as the SBus master. The SBus controller asserts the SAR dedicated $\overline{\text{SBBG}}$ signal making the SAR the master. The SAR sets the SBSIZ2–SBSIZ0 signals to indicate a 1-word, 16-byte, or 32-byte transfer, the SBRD signal indicates a read or write operation, and the DVMA address is placed on the SBD31–SBD0 lines. The TNETA1560 monitors the SBACK2–SBACK0 lines anticipating the appropriate acknowledgment value. The SBus SAR considers either an error acknowledgment on the SBACK2–SBACK0 lines or a late error on the $\overline{\text{SBLERR}}$ line as a fatal error, disables all data-transfer processing, and generates a SBus interrupt via the $\overline{\text{SBIRQ}}$ signal.

control-memory interface

The control memory is set up in a 16K $\times$ 32 configuration with the cycle time given by the SBus clock. The interface is designed for an asynchronous SRAM with a 32-bit data bus, a 14-bit address bus, a CMR/$\overline{\text{W}}$ signal determine read or write, and an output-enable signal ($\overline{\text{CMOE}}$).

PHY-layer interface

The SBus SAR generates a transmit clock at the SBus frequency and a 19.44-MHz receive clock. This ensures that all setup- and hold-time restrictions are met.

The SBus SAR generates output data along with a start-of-cell indicator in the transmit direction. This data is sent at the rate of the SBus clock. The PHY layer can respond with a full signal, which is asserted at least four cycles before any internal buffers are full. The SAR then turns off $\overline{\text{TXENABLE}}$ until the full signal is deasserted. The PHY layer sends a start-of-cell indicator with output data. The empty signal acts as an inverted enable signal on this interface.

The PHY-layer interrupt signal is directly connected to the SBus interrupt signal; therefore, the SBus interrupt is asserted when the PHY-layer interrupt signal is asserted.

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local-bus interface

Since there could be several devices on the local bus, the SBus SAR accepts a ready signal from devices on the bus as a handshake. The bus transaction is assumed to be complete eight SBus cycles (at least 320 ns) after the transaction is initiated, regardless of the ready signal. This accommodates slow devices such as EPROMs and also can be used to relax timing constraints on the register interface for the PHY-layer devices.

The local bus is accessed exclusively via SBus transactions with the SAR as the slave with the exception of the local-bus interrupt signal. The lower 16 bits of the SBus address bus are directly routed to the local-bus (LBus) address bus. The SBus address must remain stable while the local bus is active. This is achieved by not returning an acknowledgment signal on SBus until the LBus transaction is complete.

architecture

Figure 14 depicts a data-flow representation of the SBus SAR architecture.

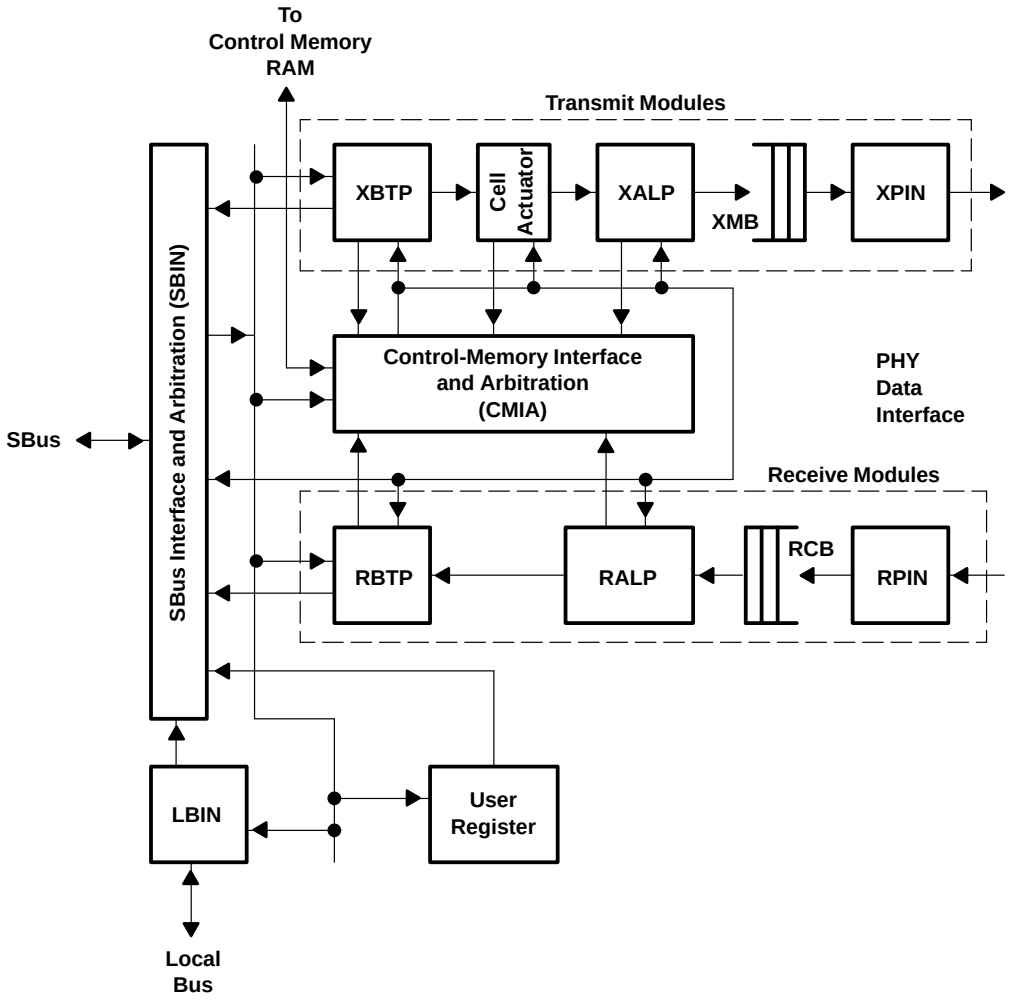

Figure 14. SBus SAR Architecture

PRINCIPLES OF OPERATION

transmit modules

The transmit-host and buffer-transaction processor (XBTP) is responsible for all host-related functions on the transmit side and requests 16- and 32-byte transfers from the SBus-interface block. The cell actuator accesses the BWG table and determines the next VC to be serviced. The transmit adaptation-layer processor (XALP) processes all AAL-related functions and adds the four bytes of the ATM header to each cell. The XALP identifies the AAL5 CRC and determines if it should be appended to the packet. The transmit buffer (XMB) is an 8-cell buffer that receives 13 words per cell. Idle cells are also placed in this buffer. The transmit PHY interface (XPIN) does word-to-byte unpacking and interacts with the PHY layer using the SBus clock.

receive modules

The receive PHY interface (RPIN) performs byte-to-word packing, filters idle cells, and interacts with the PHY layer using the system's PHY-layer clock crystal. The receive buffer (RCB) performs rate synchronization from the PHY-layer clock to the SBus clock and buffers up to 32 cells. The receive ATM processor (RAT) and the receive ATM adaptation-layer processor (RALP) operate in parallel and are part of the same module. The RALP terminates the AAL5 CRC and processes various EOP indicators. The RAT block is responsible for deleting the ATM header and accessing the correct receive DMA entry. Finally, the receive host and buffer-transaction processor (RBTP) performs all host-specific functions on the receive side.

SBus interface module

The SBus interface module (SBIN) is responsible for implementing the details of the SBus protocol. The XBTP and the RBTP are the only two modules that require SBus transactions involving the SAR as a master; therefore, SBIN arbitrates between requests from the two blocks. The SAR is the SBus slave when the host accesses control memory, the local bus, or the user registers internal to the SAR.

control-memory interface and arbitration

The control-memory interface and arbitration (CMIA) block performs memory arbitration for all the blocks that access control memory. Since each access is a 1-word access, no module can hold up the memory for a long time. CMIA imposes a strict priority mechanism and services various blocks in the following order: RALP, XALP, cell actuator, RBTP, SBTP, SBIN.

local bus-interface module

The local bus-interface (LBIN) module is used to access the EPROM and the registers on the PHY-layer device.

user register

The user-register block stores a number of configuration and operational registers. The user registers also generate SBus interrupts on packet completion or when an error condition is detected.

data management

The SAR architecture uses two memory subsystems: host memory and on-board control memory. The control memory provides fast multichannel memory-based DMA channels and a temporary storage area used as virtual auxiliary registers. Some transmit and receive data-management components reside in control memory for immediate access to critical real-time events isolated from host memory, which is tied to SBus latency. The AAL5 CRC is also encapsulated in the control memory. The control memory is accessible by the host for initialization and monitoring the hardware and network status. Figure 15 shows the organization of the SAR data structures across control and host memory.

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data management (continued)

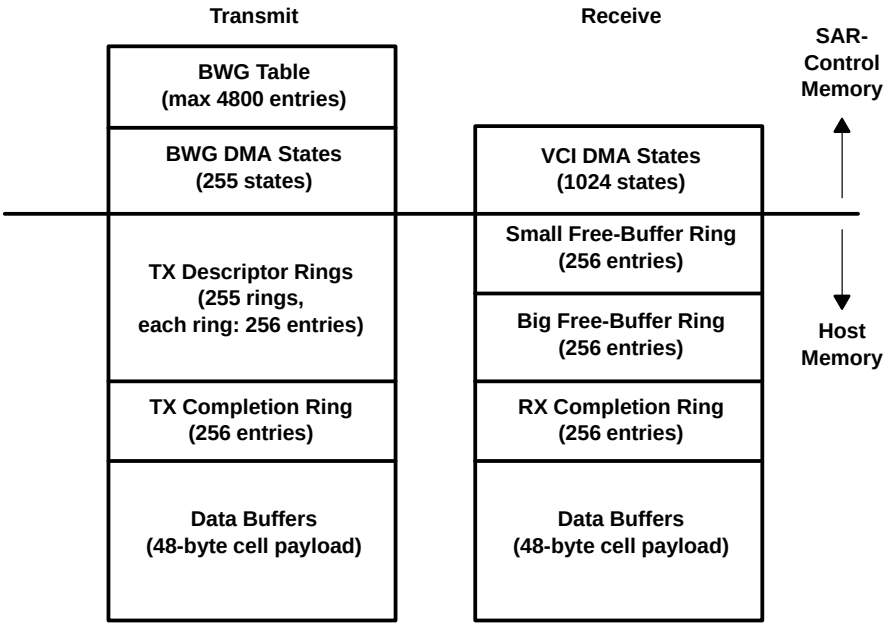

Figure 15. SBus SAR Data Organization

Several registers stored in the control memory indicate the address of the next entry in the two free-buffer rings and the two completion rings. The descriptor rings apply to packet- or buffer-level processing, whereas the DMA channels apply to per-cell processing. The transmit DMA state for each BWG indicates the location of each transmit descriptor ring.

programmer's reference

This section presents the SBus SAR data structures in detail. The contents of various physical locations are summarized in Table 3. A large part of this information is presented in Figure 15 but is duplicated here for convenience.

Table 3. Location of SBus SAR Data Structures

CONTROL MEMORY	HOST MEMORY	SAR REGISTERS	EPROM
BWG table	TX descriptor rings (255)	Configuration registers	Boot code
TX DMA states	TX completion ring	Operation registers	48-bit address
RX DMA states	Small free-buffer ring		Diagnostics
Initialization block	Big free-buffer ring		SBus ID
	RX completion ring		
	Data buffers		

The system has a bus width of four bytes and all transactions are conducted on 4-byte boundaries. The SBus SAR uses big-endian addressing by definition as an SBus device. All addresses are in hexadecimal notation unless otherwise specified.

programmer's reference (continued)

Each descriptor ring has 256 entries as shown in Figure 15. Each descriptor-ring entry consists of four words. Each descriptor ring is aligned to a 4K-byte boundary in host memory with each entry aligned to a 16-byte boundary. The SAR has two receive free-buffer rings, one transmit completion ring, and one receive completion ring. The current pointer to each of these rings is stored in the initialization block in SAR control memory. An entry in each transmit DMA channel points to one of the 255 transmit-descriptor rings in host memory.

Each DMA-channel entry consists of eight words and is located in control memory. The DMA entries on both transmit and receive have an OWN bit that is set when the DMA channel is active. The descriptor-ring entries, the completion-ring entries, and the free-buffer-ring entries have an OWN bit that is set when the entry belongs to the SAR.

control-memory map and access

Table 4 shows a control-memory map. The address bus to memory is 14 bits wide. The physical SBus offset address on the SAR for control memory is C00000 hex. All SBus accesses to control are 1-word accesses at word boundaries.

Table 4. Control-Memory Map

MEMORY REGIONS	CONTROL-MEMORY BASE POINTERS (hex)	SBus PHYSICAL ADDRESS (hex)
Initialization block	0000	C00000
Transmit BWG 0 – 255 – DMA block	0100	C00400
BWG table (1200 words, 4800 entries)	0900	C02400
Receive BWG / VCI 0 – 1023 – DMA block	1000	C04000

initialization block

The initialization block contains exactly four entries and resides in control memory. Table 5 shows the configuration of the initialization block.

Table 5. Initialization Block

SBus PHYSICAL ADDRESS (hex)	CONTROL-MEMORY ADDRESS (hex)	BITS 27 – 8	BITS 7 – 0
C00000	0000	TX completion-ring offset pointer	Index 0 – 255
C00004	0001	RX completion-ring offset pointer	Index 0 – 255
C00008	0002	Small free-buffer-ring offset pointer	Index 0 – 255
C0000C	0003	Big free-buffer-ring offset pointer	Index 0 – 255

The pointers are mapped to SBus DVMA addresses by appending the lower-order four bits representing the offset within each 16-byte descriptor-ring entry. Since accesses are only permitted on a word basis, the lower-order two bits are always set to zero.

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transmit data-descriptor rings

Each of the 255 transmit data-descriptor rings holds 256 entries and each ring represents one transmit packet queued for transmission. A packet is composed of one or more transmit buffers. The host posts entries to the rings and the SAR processes each entry within the given ring. Table 6 shows the composition of the four-word entry.

Table 6. Transmit-Data Descriptor-Ring Summary

ENTRY	DESCRIPTION
Word 0	Control field, packet length, buffer length
Word 1	Start-of-buffer pointer – 32 bits
Word 2	4-byte ATM header
Word 3	AAL5 tail – control and length fields

TX descriptor-ring word 0 – configuration

Control (bits 31 – 27)	Packet length (bits 26 – 16)	Buffer length (bits 15 – 0)

OWN (bit 31)

The descriptor is owned by the SBus SAR when the OWN bit is set. The descriptor is owned by the host when the OWN bit is zero. The OWN bit is set by the host when a buffer/packet is queued for transmission. When the next BWG index from the BWG table does not have an active buffer location in the transmit DMA entry, the SBus SAR attempts to recover a new buffer-descriptor entry from the transmit data-descriptor ring. This entry is loaded into the DMA entry if the OWN bit is set. If the OWN bit for the first descriptor in the transmit data-descriptor ring is zero, no data is queued for transmission and an idle cell is transmitted.

The host places all the buffers for a packet in the descriptor ring before setting the OWN bits on the entries representing each buffer in sequence from the last buffer to the first buffer (in reverse order). The SBus SAR clears the OWN bit after if finishes transmitting/processing the bytes associated with the buffer pointed to by the DMA entry. When the OWN bit is cleared by the host, word 0 is not meaningful and is overwritten by the host.

start of chain (SOC) (bit 30)

The SOC bit indicates that this is the first buffer of a packet, which consists of one or more buffers. This bit is also set in packets with single buffers.

end of chain (EOC) (bit 29)

The EOC bit indicates that this is the last buffer of a packet. Single buffer packets have both the SOC and EOC bits set. Packets with multiple buffers have the SOC bit set on the first buffer and the EOC bit set on the last buffer.

AAL type – AAL5 indicator (bit 27)

The AAL-type bit indicates the packet/buffer described in this descriptor-ring entry is an AAL5 packet. When zero, this bit indicates to the SAR that AAL5 processing should be performed in the transmit direction. This includes addition of the pad, the control- and packet-length fields, and the 32-bit CRC. The total size of the AAL5 packet is a multiple of 48 bytes.

The SBus SAR does not perform any packet-level encapsulation similar to that used in AAL5 for either AAL3/4 or the null AAL. The host provides packets correctly formatted into 48-byte cells to the SAR.

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packet length (bits 26 – 16)

The packet-length field is expressed in units of cells in the packet. The host computes the correct number of cells in the packet including the additional cell sometimes needed for AAL5 to accommodate the 8-byte tail. This field represents the value used by the SBus SAR to determine the number of cells in a packet and enable EOP processing.

The field is programmed in two's complement. Incrementing the value by one each time a cell is sent results in zero when the entire packet is transmitted. The maximum size of a packet is 64K bytes; therefore, 11 bits are adequate to describe the largest packet.

Since this is a packet-level field as opposed to one that applies to individual buffers, it is only placed in the first buffer descriptor of a packet in the transmit data-descriptor rings. The DMA channel only updates the packet-length field on a per-packet basis. The packet-length field is general in that it is used for all three AAL modes supported. In each case, the SAR enables EOP processing to notify the host when the EOP is detected on transmit via the packet-length field.

buffer length (bits 15 – 0)

The buffer-length field specifies the number of bytes in the buffer represented by this descriptor-ring entry. The maximum buffer size is 64K bytes, which is the largest packet size and allows an entire packet in one buffer. This field is programmed in two's complement and is equal to zero when all the bytes in a buffer are retrieved by the SAR.

TX descriptor-ring word 1 – start-of-buffer pointer

Byte-aligned start-of-buffer pointer (bits 31 – 0)

The start-of-buffer pointer is 32 bits. Each buffer can be aligned on byte boundaries.

TX descriptor-ring word 2 – ATM header

PTI2 (bits 31 – 29)	CLP2 (bit 28)	VPI (bits 27 – 20)	VCI (bits 19 – 4)	PTI1 (bits 3 – 1)	CLP1 (bit 0)

Word 2 contains the 4-byte header for every cell of the packet. The upper-order four bits of the ATM header, representing the GFC at the user-to-network interface (UNI), are set to zero in every outgoing cell. Bits (3 – 0) in word 2 represent the payload-type indicator (PTI) and cell-loss priority (CLP) fields used in every cell of the packet except the last one (the cell that contains the EOP indication). Bits (31 – 28) in word 2 represent the PTI and CLP fields used in the last cell of the packet.

The PTI field in the last cell of an AAL5 packet is set either to 001 or 011. The CLP is programmable and the cell containing the EOP indication can have a different priority level from the other cells. This field is required only in the first descriptor for the packet. In AAL3/4 or null-AAL packets, the PTI and CLP fields in both the upper- and lower-order bits of word 2 are the same.

TX descriptor-ring word 3 – AAL5 control/length

AAL5 control field (bits 31 – 16)	AAL5 length field (bits 15 – 0)

The AAL5 control and length fields apply to packets, not to buffers, and this entry is required only in the first descriptor for the packet. The AAL5 length field is not used to determine the length of the packet during transmit processing. The software driver is responsible for entering these two fields. The control field is all zeros and the length field is the number of bytes in the packet. Both fields are placed in the descriptor ring in an AAL5 packet in the proper position (in the four bytes preceding the AAL5 32-bit CRC). These fields are not used if the packet is either an AAL3/4 or a null-AAL packet.

PRINCIPLES OF OPERATION

transmit BWG DMA block

The control memory contains 255 transmit BWG DMA entries, each containing eight words. Table 7 summarizes the contents of each entry.

Table 7. Transmit BWG DMA Entry

ENTRY	DESCRIPTION	STATIC/ DYNAMIC
Word 0	Control field, packet length, buffer length	Dynamic
Word 1	Current-buffer pointer – 32 bits	Dynamic
Word 2	4-byte ATM header	Dynamic
Word 3	Static bits – BWG ON/OFF (BWG_ON bit)	Static
Word 4	BWG data-ring pointer, descriptor pointer	Dynamic
Word 5	BWG cell-counter place holder – not implemented	Dynamic
Word 6	Partial 32-bit packet CRC	Dynamic
Word 7	AAL5 tail – control and length fields	Static

The SBus SAR initiates host transactions affecting the DMA table, except those required for one-time configuration of a channel for normal operation based on cell-transmission opportunities from the BWG table. Each DMA entry represents a buffer under segmentation.

During initialization, the host has to configure word 0, word 3, and word 4 in the transmit DMA states table for each BWG selected for transmission in the BWG table, including the BWG0. These words allow the TNETA1560 to start a transmission of a new packet. After configuration, the TNETA1560 reads word 3 to check if the BWG_ON bit is set. If it is set, the device reads word 0 to determine if the OWN bit is set. When the OWN bit is not set, it indicates that this is the first buffer of a new packet. The TNETA1560 then reads word 4 to obtain a transmit descriptor-ring pointer that indicates the memory address in host memory for the transmit descriptor-ring pointer. The following sections explain each TX DMA table word in detail.

TX DMA word 0 – state/configuration

Control (bits 31 – 27)	Current-packet length (bits 26 – 16)	Current-buffer length (bits 15 – 0)

The contents of word 0 are copied directly from the corresponding transmit data-descriptor-ring entry at the start of each new buffer. This applies to all the fields in this status word and the host must ensure consistency across the fields.

OWN (bit 31)

The OWN bit is set when the DMA channel for the BWG is active and all related state information in the DMA entry is current. The OWN bit indicates a packet is currently being segmented and transmitted for this BWG. This OWN bit is cleared by the SAR after the entire packet is transmitted, a completion-ring entry is posted, and an interrupt generated to the host.

The host sets the OWN bits for individual buffers in a packet in the transmit data-descriptor rings in order from last to first. This ensures that the DMA block is not held up while waiting to acquire the next buffer from a partially transmitted packet.

start of chain (SOC) (bit 30)

The SOC bit indicates that this is the first buffer of a packet which may consist of one or more buffers. This bit is also set in packets with single buffers. The SOC bit is cleared by the SAR after all processing for the first buffer is complete.

PRINCIPLES OF OPERATION

end of chain (EOC) (bit 29)

The EOC bit indicates that this is the last buffer of a packet. Every packet has at least one buffer with the EOC bit set.

AAL type – AAL5 indicator (bit 27)

The AAL-type bit is set to zero to indicate that the packet described in this descriptor-ring entry is an AAL5 packet. This bit is a configuration item rather than a bit carrying state information. This bit is set in every buffer of a packet, and the software driver ensures that all buffers within a packet use the same AAL type.

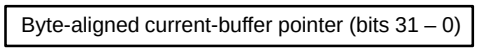
current-packet length (bits 26 – 16)

The SBus SAR increments this two's-complement value with every cell transmitted until the counter is equal to zero, which indicates to the SAR that the entire packet has been transmitted.

current-buffer length (bits 15 – 0)

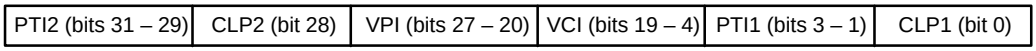
The buffer-length field specifies the number of remaining bytes in the buffer currently being processed in this BWG. The SAR adds to the value of this two's-complement field with every transfer of payload data to the XMB until it is equal to zero, which indicates to the SAR that all the bytes in this buffer are processed and queued for transmission.

TX DMA word 1 – current-buffer pointer



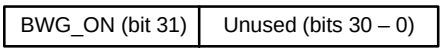
The current-buffer pointer is copied directly from the start-of-buffer pointer in the corresponding transmit data-descriptor-ring entry at the start of each new buffer. The field is 32 bits, which implies that the buffer is aligned to a byte boundary. The pointer is adjusted to point to the current location after each transfer of payload data from the host to the XMB.

TX DMA word 2 – ATM header



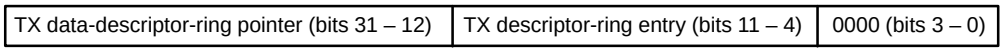
The 4-byte ATM header field is copied directly from the corresponding transmit data-descriptor entry at the start of each new packet. Bits (28 – 0) are concatenated to the 4-bit GFC field that is set to zero for every cell in the packet except the last one. Bits (31 – 28) provide the PTI and CLP fields in the last cell of each packet.

TX DMA word 3 – configuration



This bit allows the host to enable data transmission on a per-BWG basis. The BWG_ON bit from the current BWG index is examined by the SAR on each cell opportunity. BWG_ON (31) is directly set by the host to indicate that the BWG is enabled and that normal data processing is followed. If the bit is zero, no processing of transmit data on the BWG is performed and an idle cell is transmitted on the link. This idle cell is used by the host to respond to congestion indicators.

TX DMA word 4 – descriptor-ring address



This pointer is a direct DVMA address to the location of the current entry (there are 256 entries in each ring) in the corresponding transmit data-descriptor ring (one of 255 rings) for this BWG. Each descriptor ring is aligned to a 4K-byte boundary in host memory with each entry aligned to a 16-byte boundary.

PRINCIPLES OF OPERATION

TX DMA word 4 – descriptor-ring address (continued)

The address of the 4K-byte boundary in host memory is provided by bits (31 – 12). The entry number between 0 and 255 is provided by bits (11 – 4). The low-order four bits are set to zero and each entry is 16 byte aligned. Bits (11 – 0) are initialized by the host to zero to correspond with the first entry used by the host in the transmit data-descriptor ring.

TX DMA word 5 – place holder

Place holder (bits 31 – 0)

TX DMA word 6 – transmit CRC

Partial AAL5 transmit CRC (bits 31 – 0)

This field stores the 32-bit CRC calculated over the entire payload of each AAL5 packet. The CRC is placed in the last four bytes of the last cell of the corresponding packet.

TX DMA word 7 – AAL5 tail

AAL5 control field (bits 31 – 16)	AAL5 length field (bits 15 – 0)

The AAL5 control and length fields are copied directly from the corresponding transmit data-descriptor entry at the start of each new packet. The length field is not used for any control functions within the SAR. Both fields are used exclusively for placement in the tail of an AAL5-protocol data unit (PDU).

transmit completion ring

Table 8 shows the composition of the 4-word entry. The transmit completion ring is a free ring with 256 entries. The SAR posts an item to the next entry in the completion ring when it completes the transmission of each packet. The transmit-completion-ring pointer maintains the value of the current entry within the SAR. The host can recalibrate to this by reading the value from the initialization section in control memory.

Table 8. Transmit-Completion-Ring Summary

ENTRY	DESCRIPTION		
Word 0	OWN (bit 31)	Unused (bits 30 – 8)	BWG index (bits 7 – 0)
Word 1	Reserved		
Word 2	Reserved		
Word 3	Reserved		

TX completion-ring word 0

OWN (bit 31)

This completion-ring entry is owned by the SBus SAR when the OWN bit is set. The completion-ring entry is owned by the host when the OWN bit is zero. The SAR uses the next completion-ring entry in the ring if the OWN bit is set. The TNETA1560 clears the OWN bit after updating the entry. The host then receives an interrupt and retrieves the next entry in the completion ring to post the completion of packet transmission for a BWG and the release of the buffer space occupied by the buffers constituting the packet. The host clears the OWN bit to allow the SAR to use the completion-ring entry. If the OWN bit is not set when the SAR is ready to post a completed packet, a status bit is set in the hardware-status register and an interrupt is generated if the error condition is unmasked.

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BWG index (bits 7 – 0)

The only item that is posted to the transmit completion ring when the SAR completes transmission of a packet is the BWG index. This is adequate for the host to locate the transmit-buffer pointers to the buffer locations where data for the packet was stored and reclaim the buffer space.

receive free-buffer-ring format

Table 9 shows the composition of each free-buffer-ring entry. Each of the two rings has 256 entries. The host places free-buffer pointers in each ring. The SAR removes a pointer when it starts processing each new packet from the link.

Table 9. Receive Free-Buffer-Ring Summary

ENTRY	DESCRIPTION		
Word 0	OWN (bit 31)	Unused (bits 30 – 28)	Start-of-buffer pointer (bits 27 – 0)
Word 1	Reserved		
Word 2	Reserved		
Word 3	Reserved		

RX free-buffer-ring word 0

OWN (bit 31)

Each free-buffer-ring entry is owned by the SAR when the OWN bit is set and it is owned by the host when the OWN bit is zero. The host sets the OWN bit for new entries placed in the free-buffer rings. The SBus SAR uses the next free-buffer-ring entry in the respective ring if the OWN bit is set. The SBus SAR clears the OWN bit after acquiring the buffer and releasing the ring location to the host. The buffer is not freed until a packet is posted to the receive completion ring. If the OWN bit is not set when the SAR polls a free-buffer ring for a new entry, a status bit is set in the hardware-status register and an interrupt is generated if the error condition is unmasked.

start-of-buffer pointer (bits 27 – 0)

A pointer to a buffer, aligned to a 16-byte boundary, is the only information placed in each free-buffer ring.

receive DMA block

The SAR supports 1024 receive DMA-channel entries with each containing eight words. Each DMA channel represents a VCI on which data is received, and DMA entries in the control memory are indexed by incoming VCIs. The SAR initiates all transactions affecting the DMA table, except those required for one-time configuration of a channel in word 3, during normal operation based on the header of cells received from the link. Table 10 summarizes a receive DMA-channel entry.

Table 10. Receive DMA-Virtual-Channel Entry

ENTRY	DESCRIPTION	STATIC/DYNAMIC
Word 0	Control, status, EFCN cell count, current packet length	Dynamic
Word 1	Current buffer pointer – 28 bits	Dynamic
Word 2	Start-of-buffer pointer – 28 bits	Static
Word 3	Control, packet length	Static
Word 4	Reserved	
Word 5	AAL5 partial CRC – 32 bits	Dynamic
Word 6	Reserved	
Word 7	Reserved	

PRINCIPLES OF OPERATION

receive DMA block (continued)

Data with the PTI field equal to 10X, representing VC-level OAM cells, is diverted to DMA channel 0 that operates in the null-AAL mode with a packet length of one cell. Word 0 in each receive DMA-channel entry is copied from word 3 at the start of each new packet. A number of the fields in word 0 represent the dynamic state of the reassembly process for a cell. The fields in word 3 represent one-time configuration values for the VC entered by the host. SAR accesses word 0 during normal cell-level processing to retrieve configuration items.

RX DMA word 0 – VC status/configuration

Control (bits 31 – 23)	Unused (bit 22)	Current-congestion number (bits 21 – 11)	Current-packet length (bits 10 – 0)

OWN (31)

The OWN bit is set when the DMA channel for this BWG is active and all DMA parameters such as the receive-data pointer, buffer length, and packet length are current. The OWN bit is set by the SAR when word 3 is copied to word 0 at the start of each new packet. The bit is cleared by the SAR when the entire packet has been posted to a buffer in host memory. The BWG is inactive when the OWN bit is zero. The free-buffer ring indicated in word 3 is used to poll a new buffer on the arrival of the first cell of a new packet on the VCI used to index this BWG.

static-configuration bits from word 3

Table 11 summarizes six static-configuration bits copied from word 3 at the start of each packet. Each is described in detail in the section on word 3 of this DMA block.

Table 11. RX DMA Word 0 Static-Configuration Bit Summary

LOCATION	FIELD
Bit 30	VC_ON
Bit 29	Buffer type: small or big
Bit 28	Null-AAL5 indication
Bit 25	AAL3/4 indication
Bit 24	End-of-packet wait
Bit 23	Enable-end-of-packet wait

explicit-forward congestion-notification (EFCN) cell counter (bits 21 – 11)

The number of cells received with the EFCN indicator set in each packet is counted and the value stored in this field. The EFCN indication is given a logic value of 01x in the PTI field of the ATM header. This value is passed to the receive completion ring at the end of each packet. Since this field is copied from word 3 at the start of each new packet, it is reset to zero at this time.

packet length (bits 10 – 0)

The packet-length field in word 0 is set up with the two's-complement value for the buffer size used by this BWG at the start of each new packet. The counter is incremented with each new cell until the EOP signal or until the value is zero. Null-AAL packets are terminated when the value of this counter reaches zero. If either the AAL5 or AAL3/4 packet fills the buffer to capacity, the counter reaches zero and the packet is terminated with the buffer-overflow indicator set in the receive completion-ring entry.

PRINCIPLES OF OPERATION

RX DMA word 1 – current-buffer pointer

Unused (bits 31 – 28)	Current-buffer pointer – 16 byte aligned (bits 27 – 0)

The current-buffer pointer is 28 bits, which implies that the buffer is aligned to 16-byte boundaries. This is a dynamic field that is updated with every RCB-to-SBus transaction.

RX DMA word 2 – start-of-buffer pointer

Unused (bits 31 – 28)	Start-of-buffer pointer – 16 byte aligned (bits 27 – 0)

The start-of-buffer pointer is 28 bits because the buffer is aligned to 16-byte boundaries. This field is copied from the corresponding 28-bit field in word 0 of a free-buffer-ring entry.

RX DMA word 3 – configuration

Configuration (bits 31 – 23)	Unused (bits 22 – 11)	Null-AAL packet length (bits 10 – 0)

OWN bit position (bit 31)

The OWN bit is set high for each valid receive channel. It is copied into the corresponding OWN bit location in word 0 at the start of each new packet to indicate that the DMA channel is active.

VC_ON (bit 30)

The VC_ON bit enables packet-reassembly processing. The bit is set in the default mode to indicate that the VC is enabled. The SAR discards cells received on the corresponding VC when the VC_ON bit is deasserted on a per-cell basis.

buffer type – small or big (bit 29)

The SAR supports only two buffer sizes on receive: small and big. The host determines the sizes of the small and big buffers. The buffer-type bit is used to select between a buffer pointer from the small free-buffer ring or the big free-buffer ring for each new packet, which allows the host to target small or big buffers for all packets on a given VC. The small free-buffer ring is used when the bit is set and the big free-buffer ring is used in the default (zero) state.

null-AAL indication (bit 28)

This field is set to indicate that null-AAL packets are received on this BWG (VC). The null-AAL packet-length field in bits (10 – 0) is used to determine the end of a packet. CRC errors are ignored for null-AAL packets. The CRC-error indicator in the receive completion ring is not used.

AAL3/4 indication (bit 25)

This field is set to indicate that AAL3/4 packets are received on this BWG (VC). This indicates the EOM field in byte 6 (bit 6 of an ATM cell is used as the EOP indicator). CRC errors are ignored for AAL3/4 packets. The CRC-error indicator in the receive completion ring is not used.

end-of-packet wait (bit 24)

This bit must be set to zero by the device driver during initialization. This gives the SAR the responsibility of setting the bit to one in DMA word 0 (when this feature is enabled). This bit is a status bit used by the TNETA1560 during operation.

PRINCIPLES OF OPERATION

enable end-of-packet wait (bit 23)

When a start of a packet is detected by the TNETA1560, the TNETA1560 requests a buffer from the host memory. If the buffer is not available, the first cell of this packet is dropped. The rest of the packet is dropped after it is received. The host can set bit 23 to 1 enabling the TNETA1560 to drop the cells of a packet that had the first cell dropped. Once the TNETA1560 detects the end packet, it begins to receive packets in this VCI. This feature only works for AAL5 and AAL3/4. For null-AAL and OAM cells, bit 23 must be set to zero.

EFCN cell counter place holder (bits 21 – 11)

This field is set to zero since it is a place holder for the EFCN cell counter in word 0 of this DMA block.

AAL-packet length (bits 10 – 0)

The AAL-packet-length field in word 3 indicates the length of the buffer in cells for each packet in this BWG. This is used in different ways based on whether the BWG supports AAL5 or AAL3/4 packets or null-AAL packets. This field indicates the length of the buffer size allocated by entries in the free-buffer ring used by this BWG for AAL5 or AAL3/4 packets. This is used to detect buffer overflow.

When the null-AAL indicator is set, this field programmed in two's-complement notation represents the number of cells in each null-AAL packet. Since receive DMA channel 0 operates off the null-AAL mode with each packet of size equal to one cell, this field is programmed with the value 1 in two's-complement notation (7FFhex).

RX DMA word 5 – AAL5 partial CRC

Partial AAL5 receive CRC (bits 31 – 0)

This field stores the 32-bit CRC that is calculated over the entire payload of each received AAL5 packet. The CRC is stored in the last four bytes of the last cell in the AAL5 frame. The CRC check results in a unique polynomial, if the frame is error free.

receive completion ring

Table 12 shows the composition of a 4-word receive completion-ring entry. The receive completion ring is a free ring with 256 entries. The SAR posts an item to the next entry in the completion ring when it completes reassembly on a packet. The receive-completion-ring pointer maintains the value of the current entry within the SAR. The host can recalibrate to this by reading the value from the initialization section in control memory.

Table 12. Receive-Completion-Ring Summary

ENTRY	DESCRIPTION
Word 0	Control field, EFCN cells received, packet length
Word 1	Start-of-buffer pointer – 28 bits
Word 2	4-byte ATM header
Word 3	Reserved

RX completion-ring word 0 – control

Control (bits 31 – 29)	Unused (bits 28 – 22)	Congestion cells received (bits 21 – 11)	Packet length (bits 10 – 0)

PRINCIPLES OF OPERATION

OWN (bit 31)

This completion-ring entry is owned by the SAR when the OWN bit is set and it is owned by the host when the OWN bit is zero. If the OWN bit of the next entry in the respective receive completion ring is zero when the SAR polls it to post the completion-of-packet processing, an error indicator in the status register is set and an interrupt generated. This causes the buffer that the SAR attempted to post to be lost. The SAR clears the OWN bit in the receive completion ring after it posts the packet. The host then owns the entry and may retrieve various pointers to the packet.

packet overflow (bit 30)

The packet-overflow bit is set if the receive buffer overflowed while processing the current packet. Every packet that ends in a buffer overflow is immediately terminated and a completion-ring entry is posted to the host.

CRC condition (bit 29)

The SAR forwards AAL5 packets with a CRC error to the host. This bit is set when a packet is received with an AAL CRC error.

congestion cells received (bits 21 – 11)

The number of cells received in the packet with the EFCN indication set is forwarded to the host to implement associated feedback mechanisms to squelch the source.

packet length (bits 10 – 0)

All received data is passed to the host in units of 48 bytes. The packet length in 48-byte payload units from word 0 of the receive DMA block is passed to the host in two's-complement notation. This value is always zero for null-AAL packets. The length of AAL5 or AAL3/4 packets in integer units is obtained by subtracting this value from the reassembly-buffer length reserved for the packet.

RX completion-ring word 1 – start-of-buffer pointer

Unused (bits 31 – 28)	Start-of-buffer pointer – 16 byte aligned (bits 27 – 0)

The 28-bit start-of-buffer pointer is provided to the host in the RX completion ring to enable it to locate the reassembled packet.

RX completion-ring word 2 – ATM header

ATM header byte 1	ATM header byte 2	ATM header byte 3	ATM header byte 4

The 4-byte header from the last cell in the reassembled packet is passed to the host.

user registers

This section describes several host-accessible internal SAR registers. Host-write accesses to nonexistent registers are ignored. A null word (32 zeroes) is returned to the host on a read access from a nonexistent register.

configuration register

The configuration register holds various values pertaining to overall SAR configuration. The host may read the register and is allowed to program the EN_RX and the EN_TX bits.

Unused (bits 31 – 5)	NCE_M (bit 4)	0 (bit 3)	EN_RX (bit 2)	EN_TX (bit 1)	0 (bit 0)

PRINCIPLES OF OPERATION

EN_TX – enable transmit operation

The EN_TX bit allows the host to disable packet-to-cell segmentation and any payload data transfer from the host to the link. It is set high to enable normal transmit processing and set to zero to disable such processing. It is set to zero on reset, disabling transmit operation until various configuration register, the BWG table, and the DMA blocks are configured by the host. The transfer of the new cells from SBus to the SAR is inhibited when the enable-transmit bit is disabled; however, cells already in the output buffer are forwarded to the PHY layer.

EN_RX – enable receive operation

The EN_RX bit allows the host to disable packet reassembly. All cells from the PHY layer are dropped when the EN_RX bit is zero. The EN_RX bit is set high to enable normal processing. It is set to zero on reset, disabling receive operation until various configuration and the DMA blocks are reconfigured by the host. The transfer of new cells from the ATM link to the receive buffer is inhibited when the enable receive bit is disabled.

NCE mode indicator

The NCE bit is set to indicate to the SAR that cell payloads must be transferred exclusively via 16-byte SBus bursts. The value at the input of the NCE-mode terminal is shifted into this indicator bit on every clock cycle. Internal operation of the SBus SAR is based on the value of this register.

status register

The SAR status register is read only for the host. All the bits except the TX_freeze bit and the SBus error flags are cleared when the register is read. The SAR generates an SBus interrupt to the host if one of the bits in the register is set and if the condition represented by the bit is enabled by the interrupt-enable-mask register. The SBus interrupt is an asynchronous signal that is held until the system clears the condition that caused the interrupt.

Unused (bits 31 – 11)	LB_intr (bit 10)	SB_lerr (bit 9)	SB_err_ack (bit 8)
RX_freeze (bit 7)	TX_freeze (bit 6)	TX_comp_notav (bit 5)	RX_comp_notav (bit 4)
RX_bfree_notav (bit 3)	RX_sfree_notav (bit 2)	TX_comp_update (bit 1)	RX_comp_update (bit 0)

TX_comp_update, RX_comp_update (bits 1 – 0)

The transmit or receive completion update bit is set when the hardware releases a transmit or receive descriptor, respectively, to the completion ring. This is initiated when the OWN bits in the respective DMA blocks are cleared by the SAR.

RX_bfree_notav, RX_sfree_notav (bits 3 – 2)

The appropriate receive free-buffer not-available bit is set when the first entry in the corresponding receive free-buffer ring is not available. This is indicated when the OWN bit in the first entry of the free ring is zero.

The incoming cell is deleted since there is no buffer available in which to place it. This eventually causes the loss of the entire packet due to the resultant CRC error. The buffer-allocation-error bit in the DMA block is set, indicated by a zero in the first free-buffer-ring entry.

RX_comp_notav (bit 4)

The receive completion-ring not-available bit is set when the next descriptor in the receive completion ring has not been released by the host. This is indicated when the OWN bit in the entry is zero. This packet and buffer are both lost to host memory.

PRINCIPLES OF OPERATION

TX_comp_notav (bit 5)

The transmit completion-ring not-available bit is set when the next descriptor in the receive completion ring has not been released by the host. This is indicated when the OWN bit in the entry is zero. The transmit-freeze bit is set when this bit is set, disabling all transmit operation until the transmit-freeze bit is cleared via an active command from the host.

TX_freeze (bit 6)

The transmit-freeze bit is set when the TX_comp_notav bit is set, disabling all transmit operation until the transmit-freeze bit is cleared via an active command from the host. This has the same effect on the transmit circuitry as disabling the enable-transmit bit.

RX_freeze (bit 7)

The receive-freeze bit is set when the RX_comp_notav bit is set, disabling all receive operation until the receive freeze bit is cleared via an active command by the host. The buffer that could not be posted is effectively lost, and the host must find some way to recover it while the freeze is in operation. The receive-freeze indicator has the same effect on the receive path as disabling the enable-receive bit.

SB_err_ack (bit 8)

The SBus-error-acknowledgment bit is set to indicate that the SAR detected the SBus-error-acknowledgment signal; i.e., SBACK2 – SBACK0 set to 110 during the SBus DMA cycle. The SAR then terminates the ongoing master-bus cycle, even if it is a burst transfer, and freezes all DMA-channel operation until a hardware or software reset. This is a fatal error.

SB_lerr (bit 9)

The SBus-late-error bit is set to indicate that the SAR detected the SBus-late-error ($\overline{\text{SBLERR}}$) signal during the SBus DMA cycle. The SBus SAR then terminates the ongoing master-bus cycle unless it is a burst transfer, in which case, it completes the burst. It then freezes all DMA-channel operation until a hardware or software reset. This is a fatal error.

LB_intr (bit 10)

The LBus-interrupt bit is set if an interrupt is generated on the local bus.

interrupt-enable-mask register

Unused (bits 31 – 11)	Mask (bits 10 – 0)

The interrupt-enable-mask-register bit has a bit to correspond to every entry in the status register. When a bit in the mask register is set, an interrupt is generated if a corresponding bit in the status register is also set.

BWG-table-configuration register

Unused (bits 31 – 11)	BWG Table Size (bits 10 – 0)

The 11-bit BWG-table-size register allows the user to configure the size of the BWG table in 4-byte words. Each word in the table consists of four 8-bit entries. The maximum table size is 1200 decimal, allowing for 4800 entries. A resolution greater than 32 kb/s is achieved with 4800 entries. The number of entries in the table is one more than the number programmed in this register; therefore, there is one entry in the table when the register is set to zero.

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FIFO-maximum-depth registers

Unused (bits 31 – 20)	Max_RX_FIFO_Depth (bits 19 – 10)	Max_TX_FIFO_Depth (bits 9 – 0)

This is the only set of statistics collected by the SAR, which is useful information for queuing analysis in different platforms with varying SBus-clock speeds and latencies. These registers are not of the read-and-reset variety and must be explicitly set to zero to restart the measurement.

SBus physical-address mapping (in SBus-slave mode)

The SAR allows the host to access various peripheral devices and internal registers via an SBus-slave mode. The device connects to the SBus physical-address bits (15–0) and (24–23). To access the PHY-layer register, the software driver uses the SBus address offset given in Table 13. The SBus interface on the TNETA1560 uses byte addressing to access the PHY-layer registers. During read operations, the data byte received from the PHY-layer device is copied four times to make a 32-bit data word that is transferred across the bus. In a write operation to a PHY-layer register, the software writes a valid data byte on SBD31–SBD24 because the SBus uses the big-endian convention.

The accesses to the EPROM are similar to the read operations to the PHY-layer registers with the difference being that the SBACK signals are set to 101 to indicate byte accesses.

peripheral devices

Table 13 specifies the SAR-slave mode SBus physical-address ranges for the SAR peripheral devices.

Table 13. SBus Physical Addresses for SAR Peripheral Devices

ADDRESS – 24 BITS (hex)	DESCRIPTION	ADDRESS BITS	READ/WRITE
000000-00FFFF	EPROM addresses	16	Read only
400000-40FFFF	PHY-layer register addresses	16	Read/write
C00000-C0FFFF	Control-memory addresses	14	Read/write

SBus SAR registers

The SBus SAR internal registers have an SBus physical-address base value of hex 800000. Table 14 specifies the offset from this address for various SAR registers.

Table 14. SBus Physical Addresses for SAR Registers

OFFSET – 8 BIT (hex)	DESCRIPTION	READ/WRITE
00	Software reset	Write only
04	Status register	Read only
08	Interrupt-mask register	Read/write
0C	Configuration register	Read/write
10	Reserved	
14	BWG-table-size register	Read/write
18	TX/RX FIFO-maximum-depth register	Read/write
1C	Reserved	
20	Clear-transmit-freeze command	Write only
24	Clear-receive-freeze command	Write only

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