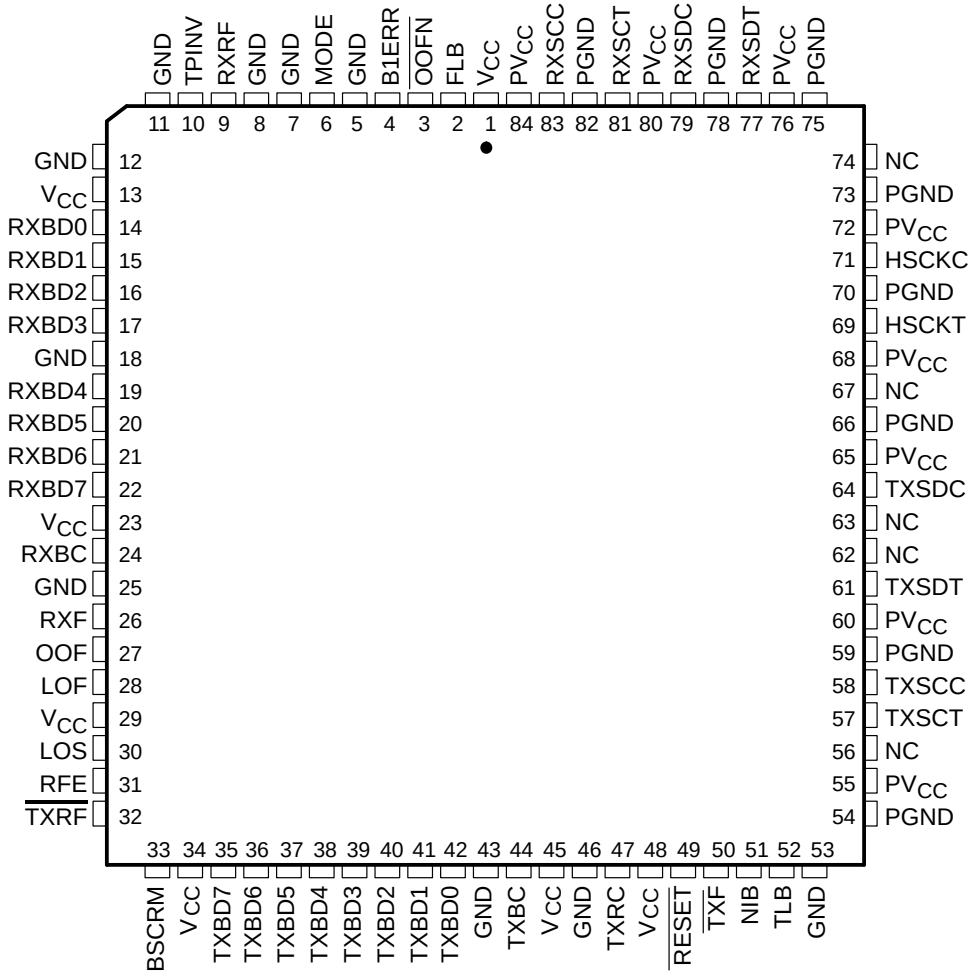
SDNS002 – SEPTEMBER 1992 – REVISED JUNE 1993

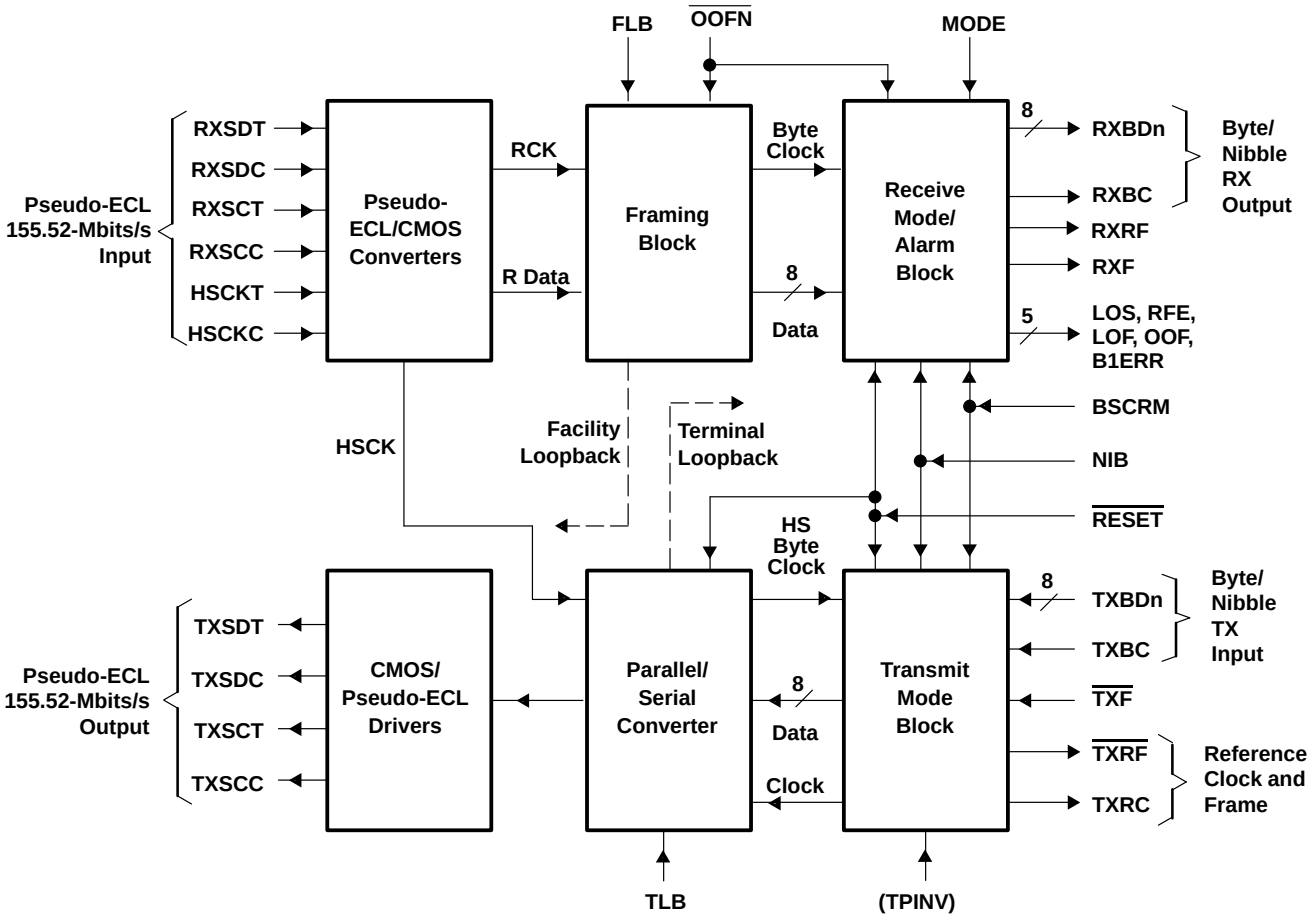
- **Member of the Texas Instruments Digital Communication Series of Standard DS-3 and SONET Devices**
- **Transmits and Receives at the STS-3/STM-1 Rate of 155.52 Mbits/s**
- **Converts 155.52 Mbits/s Data and Clock to Byte/Nibble Data and Clock and Vice Versa**
- **Provides Psuedo-ECL Levels for 155.52-Mbits/s Data and Clock**
- **Detects the Frame of the Incoming Signal and Transmits a Frame-Indication Signal**
- **Provides User-Selectable Options for:**
  - **Signal Scrambling/Descrambling**
  - **B1 Parity Calculation**
- **Provides Loss-of-Signal (LOS), Loss-of-Frame (LOF), and Receive Frame-Error (RFE) Flags for 155.52-Mbits/s Data**
- **Packaged in 84-Pin Plastic Leaded Chip Carrier (PLCC) Using 50-mil Center-to-Center Spacings**

FN PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



description

The TDC2302B provides a complete frame synchronization function for a STS-3/STM-1 signal interface. The device frame aligns the incoming 155.52-Mbits/s serial data stream and converts it to a byte or nibble data output. A byte or nibble clock output is also provided along with a frame indication signal. In the transmit direction, the TDC2302B accepts byte or nibble data and clock and outputs a 155.52-Mbits/s serial data stream. The device can be programmed to provide signal descrambling/scrambling and B1 byte parity checking/generation. The TDC2302B also monitors the incoming serial data and provides a loss of signal (LOS) indicator. In addition, loopback of both the facility serial line input and the terminal byte/nibble input is provided.

The TDC2302B provides two modes of frame synchronization: tracking or nontracking. When the tracking mode is activated, the device finds the frame of the incoming signal and monitors the signal continuously for frame alignment errors. In this operating mode, outputs are provided to indicate a receive frame error (RFE), out-of-frame error (OOF), or loss-of-frame error (LOF). If the nontracking mode is activated, the device finds the frame of the incoming signal, but no subsequent monitoring of the signal is provided. In this mode, the RFE, OOF, and LOF outputs are deactivated.

The serial data and clock inputs and outputs operate at pseudo-ECL levels (ECL levels referenced to 5 V instead of 0 V). Of the remaining I/O signals, the inputs are TTL compatible, and the outputs are CMOS. The TDC2302B is specified for operation over a temperature range of –40°C to 85°C.

description (continued)

serial data input to byte/nibble output

The serial inputs to the TDC2302B consist of a 155.52-Mbits/s data stream and a corresponding 155.52-MHz clock signal from an optical-to-electrical converter, clock recovery circuit, or similar function. Both the serial data and clock inputs operate at differential pseudo-ECL levels. The serial data is clocked into the device on a positive transition of the clock signal. A serial search for the framing bytes (A1, A2) is performed on the incoming data in accordance with the selected frame synchronization mode. If the tracking mode is selected (MODE = low), the device continues to monitor the incoming data stream after the frame has been established, and the LOF, OOF, and RFE indicators are enabled. If the nontracking mode is selected (MODE = high), the incoming data is not monitored after the frame has been found, and the LOF, OOF, and RFE indicators are disabled.

If the tracking mode is selected and an out-of-frame condition exists, the TDC2302B initiates a search for the framing pattern. The framing pattern is defined in ANSI standards and CCITT recommendations to be the six bytes (F6, F6, F6, 28, 28, 28) for an STS-3/STM-1 signal. These bytes occupy the A1 and A2 byte positions in the SONET/SDH frame. Once the frame has been found, the serial data is converted to parallel data and output in either nibble or byte format, depending on the state of the nibble (NIB) input. If NIB is high, the data is output in nibble format along with a 38.88-MHz clock. If NIB is low, the data is output in byte format along with a 19.44-MHz clock. The device also provides a framing pulse output (RXF) that goes high when the third A2 byte appears on the data output.

When tracking mode is selected, the RFE, LOF, and OOF indicators are enabled. The RFE output is synchronous with the third A2 byte and becomes active high when a framing bit error is detected. The signal is active for one clock cycle when byte format is selected and two clock cycles when nibble format is selected. If four consecutive frames have framing errors, the OOF output goes high. This output remains high for at least two frames. If the OOF output remains high for 24 frames, then the LOF output goes high. This output remains high until eight consecutive error-free frames are received. When an out-of-frame condition occurs (OOF goes high), the device begins a new search for the framing pattern. The device also begins a new search for the framing pattern if the $\overline{\text{OOFN}}$ input is taken low for two RXBC clock cycles.

The TDC2302B provides signal scrambling/descrambling and B1 parity checking/generation if the tracking mode is selected. When the BSCRM input is high, signal scrambling/descrambling and B1 parity checking/generation are both enabled, and all the bytes after the third C1 byte are scrambled. The B1 parity errors are indicated with the B1ERR output. A positive output pulse is sent out for each bit of the B1 byte in error. The pulses are clocked out with the RXBC receive clock, and each pulse is one byte clock period long. There can be up to eight pulses on the B1ERR lead in a given frame. The ordering of the bit error pulses is from bit 7 to bit 0. For example, if the pulses out of the B1ERR output form the sequence 01000100, then errors are detected in bit 6 and bit 2 of the B1 byte.

The data and clock outputs of the TDC2302B can be selected to follow either a nibble or byte format when the tracking mode is enabled. If the nibble mode is selected (NIB is high), the clock output frequency is 38.88 MHz, and the data byte is output as two nibbles on RXBD3–RXBD0. The most significant nibble is transmitted first, with the most significant bit of the data byte output on RXBD3. The least significant bit of the data byte is transmitted on the RXBD0 output of the second nibble. If the byte mode is selected (NIB is low), the clock output frequency is 19.44 MHz, and the most significant bit is output on RXBD7.

When the nontracking mode is selected, the TDC2302B begins a search for the framing pattern when the $\overline{\text{OOFN}}$ input is taken low for two RXBC clock periods. The RXBDn output data is set to zero on the rising edge of $\overline{\text{OOFN}}$. Valid data is transmitted after the framing pattern has been detected. The RFE, OOF, and LOF alarm indicators are disabled when the nontracking mode is selected. In addition, the scrambler/descrambler is disabled, and the data can be output only in byte format.

The serial input data can be looped to the serial data output (facility loopback) independent of whether tracking mode or nontracking mode is selected. To implement a facility loopback, the facility loopback (FLB) input is taken high. The received data is passed to the terminal side as well as looped back to the serial output. The terminal transmit data is blocked by the looped signal and ignored.

description (continued)

byte/nibble data input to serial data output

Nibble or byte data is clocked into the TDC2302B on negative transitions of the data input clock (TXBC). If nibble mode is selected, the data is input using the TXBD3–TXBD0 pins with TXBD3 being the most significant bit. If byte mode is selected, the data is input using the TXBD7–TXBD0 pins with TXBD7 being the most significant bit. For a given byte, the most significant bit is transmitted first on the serial data output. If the scrambling and B1 parity generation functions are to be performed by the SYNC155, then a framing pulse ($\overline{\text{TXF}}$) identifying the location of the third A2 byte in the incoming data is required. To facilitate the generation of TXBC and $\overline{\text{TXF}}$, the TDC2302B provides a reference byte or nibble clock (TXRC) and a reference frame ($\overline{\text{TXRF}}$) output that are generated from the 155.52-MHz clock inputs (HSCKT and HSCKC). $\overline{\text{TXRF}}$ is active low, has a nominal width of 51.44 ns, and occurs at the frame rate of 8 KHz. TXRC occurs at a rate of 19.44 MHz or 38.88 MHz depending upon the state of the NIB input.

The byte/nibble input data can be looped back to the byte/nibble output data if the terminal loopback (TLB) input is high. When terminal loopback is selected, the byte/nibble input data is passed to the line-side serial data output as well as looped back to the terminal-side output. The received line data is blocked by the looped signal and ignored.

The byte/nibble data is scrambled and the B1 parity byte is generated if the BSCRM input is high. If the BSCRM input is low, then these functions are bypassed. The byte/nibble data is converted to serial format and output via TXSC, the serial output clock.

Terminal Functions

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
BSCRM	33	I (TTL)	B1 scramble. A high on this input selects B1 parity generation/checking and scrambling/ descrambllng on both the received and transmitted signals.
B1ERR	4	O (CMOS)	B1 parity error. This output provides a positive pulse for each B1 bit in error clocked out with the RXBC receive clock. Each pulse is one byte-clock long.
FLB	2	I (TTL)	Facility loopback. When this input is high, the serial input data is looped backed to the serial output. The received serial data is also passed to the terminal output.
GND	5, 7, 8, 11, 12, 18, 25, 43, 46, 53		Digital ground (0-V reference)
HSCKC	71	I (PECL)	High-speed clock complement. Used with HSCKT to provide a differential input clock.
HSCKT	69	I (PECL)	High-speed clock true. Used in conjunction with the HSCKC to provide the 155.52-MHz reference and transmit clock.
LOF	28	O (CMOS)	Loss of frame. This output goes high whenever the OOF output is high for 24 frames. It remains high until eight consecutive error-free frames are received.
LOS	30	O (TTL)	Loss of signal. This output goes high whenever the receive pseudo-ECL clock or data remains high or low for 25 $\pm$ 5 ms.
MODE	6	I (TTL)	This input selects either the tracking (MODE = 0) or the nontracking (MODE = 1) mode of operation. In tracking mode, the RFE, OOF, and LOF indicators are active; in nontracking mode, they are not.
NC	56, 62, 63, 67, 74		No connection
NIB	51	I (TTL)	Nibble/byte control. If the NIB input is high, the terminal interface is nibble wide; if the NIB input is low, the terminal interface is byte wide.
OOF	27	O (CMOS)	Out of frame. This output goes high whenever four consecutive frames have framing errors and remains high for at least two frames to verify timing.
$\overline{\text{OOFN}}$	3	I (CMOS)	Out-of-frame negative. A low-level signal on this input for two RXBC clock periods starts a new frame search.

Terminal Functions (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
PGND	54, 59, 66, 70, 73, 75, 78, 82		Pseudo-ECL ground (0-V reference)
PV_{CC}	55, 60, 65, 68, 72, 76, 80, 84		Pseudo-ECL supply voltage, 5 V ± 5%
$\overline{\text{RESET}}$	49	I (CMOS)	Taking $\overline{\text{RESET}}$ low for 105 ns minimum resets the transmit side of the device. The device must be reset after power is applied.
RFE	31	O (CMOS)	Receive framing error. This output goes high whenever a framing error has been detected. The output is synchronous with the third A2 byte.
RXBC	24	O (CMOS)	Receive clock. This clock outputs the data from the TDC2302B on the falling edge of the signal. The clock frequency is either 19.44 MHz (byte clock) or 38.88 MHz (nibble clock).
RXBD(7–0)	22–19, 17–14	O (CMOS)	Receive data. Terminal-side output data, either byte-or-nibble wide, depending on the state of the NIB input.
RXF	26	O (CMOS)	Receive frame. This output provides a positive pulse in synchronization with the third A2 byte of the SONET/SDH frame.
RXRF	9	O (TTL)	Receive reference frame. An 8-KHz output derived from the input serial clock RXSC.
RXSCC	83	I (PECL)	Receive serial clock complement. Used with RXSCT to provide a differential clock input.
RXSCT	81	I (PECL)	Receive serial clock true. Used with RXSCC to provide a differential clock input that accompanies the serial data input.
RXSDC	79	I (PECL)	Receive serial data input complement. Used with RXSDT to provide a differential data input.
RXSDT	77	I (PECL)	Receive serial data input true. Used with RXSDC to provide a differential data input.
TLB	52	I (TTL)	Terminal loopback. When this input is high, the terminal input data is looped back to the terminal output. The terminal input data is also sent to the serial output.
TPINV	10	I (TTL)	Transmit path invert. When TPINV is low, the $\overline{\text{TXRF}}$ output is active low and clocked out on the rising edge of TXRC. In addition, the $\overline{\text{TXF}}$ input is active low and clocked into the TDC2302B, along with TXBDn, on the falling edge of TXBC. When TPINV is high, $\overline{\text{TXRF}}$ becomes an active-high output that is clocked out on the falling edge of TXRC. Also, $\overline{\text{TXF}}$ becomes an active-high input that is clocked into the TDC2302B, along with TXBDn, on the rising edge of TXBC.
TXBC	44	I (CMOS)	Transmit clock. Terminal-side input clock, either 19.44 MHz (byte data) or 38.88 MHz (nibble data). The data on TXBDn is clocked into the device on the falling edge of TXBC.
TXBD(7–0)	35–42	I (CMOS)	Transmit data. Terminal-side input data, either byte or nibble wide.
$\overline{\text{TXF}}$	50	I (CMOS)	Transmit frame. This active-low input is synchronous with the third A2 byte of the terminal input and is required to perform signal scrambling.
TXRC	47	O (CMOS)	Transmit reference clock. A clock output occurring at the rate of 19.44 MHz or 38.88 MHz, depending on the state of the NIB input.
$\overline{\text{TXRF}}$	32	O (CMOS)	Transmit reference frame. An active-low, one-byte-clock-wide pulse occurring at the frame rate of 8 kHz.
TXSCC	58	O (PECL)	Transmit serial clock output complement. Inverter pseudo-ECL clock output.
TXSCT	57	O (PECL)	Transmit serial clock output true. Noninverted pseudo-ECL clock output.
TXSDC	64	O (PECL)	Transmit serial data output complement. Inverted pseudo-ECL data output.

Terminal Functions (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
TXSDT	61	O (PECL)	Transmit serial data output true. Noninverted pseudo-ECL data output.
V_{CC}	1, 13, 23, 29, 34, 45 48		Digital supply voltage, 5 V ± 5%

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Supply voltage range, PECL PV_{CC} . . . . . –0.5 V to 7 V
Input voltage range, TTL . . . . . –1.2 V to 7 V
Input voltage range, PECL . . . . . 0 V to PV_{CC}
Input/output clamp current range . . . . . –50 mA to 50 mA
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	V
PV_{CC}	Supply voltage, PECL		4.75		5.25	V
V_{IH}	High-level input voltage, TTL		2			V
V_{IL}	Low-level input voltage, TTL				0.8	V
V_{IH}	High-level input voltage, CMOS	V_{CC} = 4.75 V	3.32			V
		V_{CC} = 5.25 V	3.67			
V_{IL}	Low-level input voltage, CMOS	V_{CC} = 4.75 V			1.42	V
		V_{CC} = 5.25 V			1.57	
V_{IH}	High-level input voltage, PECL (see Note 2)		3.8			V
V_{IL}	Low-level input voltage, PECL (see Note 2)				3.4	V
T_A	Operating free-air temperature		–40		85	°C

NOTE 2: All limits are given according to the absolute-magnitude convention.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, TTL	V_{CC} = 4.75 V,	I_{IK} = –18 mA			–1.2	V
V_{OH}	High-level output voltage, CMOS	V_{CC} = 4.75 V,	I_{OH} = –4 mA	4.25			V
V_{OL}	Low-level output voltage, CMOS	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
V_{OH}	High-level output voltage, TTL	V_{CC} = 4.75 V,	I_{OH} = –2 mA	4.25			V
V_{OL}	Low-level output voltage, TTL	V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.5	V
V_{OH}	High-level output voltage, PECL	PV_{CC} = 5 V,	I_{OH} = –22.4 mA	4		4.3	V
V_{OL}	Low-level output voltage, PECL	PV_{CC} = 5 V,	I_{OL} = 7.6 mA	3		3.4	V
I_I	Input current, TTL/CMOS	V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±1	µA
I_{IH}	High-level input current, PECL	V_{CC} = 5.25 V,	V_I = 4.45 V			25	µA
I_{IL}	Low-level input current, PECL	V_{CC} = 5.25 V,	V_I = 3.35 V			25	µA
I_{CC1}	Supply current‡	V_{CC} = 5.25 V, f_i = 155.52 Mbits/s	I_O = 0,			100	mA
I_{CC2}	Supply current§	V_{CC} = 5.25 V,	f_i = 155.52 Mbits/s			175	mA
C_i	Input capacitance, TTL				4		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ PECL outputs are unterminated.
§ PECL outputs are terminated with 50 Ω to 3 V.

timing requirements (see Figures 1 and 2)

All timing intervals are measured at $(V_{OH} – V_{OL})/2$ or $(V_{IH} – V_{IL})/2$ as applicable. TTL/CMOS outputs have a load capacitance of C_L = 25 pF. PECL outputs are terminated with 50 Ω to 3 V.

		MIN	NOM	MAX	UNIT
$t_{w(RXSC)H}$	Pulse duration, RXSC high	2.9			ns
$t_{w(RXSC)L}$	Pulse duration, RXSC low	2.9			ns
$t_{c(RXSC)}$	Clock cycle time, RXSC		6.43		ns
$t_{su(RXSD)}$	Setup time, RXSD before RXSC↑	3			ns
$t_{h(RXSD)}$	Hold time, RXSD after RXSC↑	1			ns

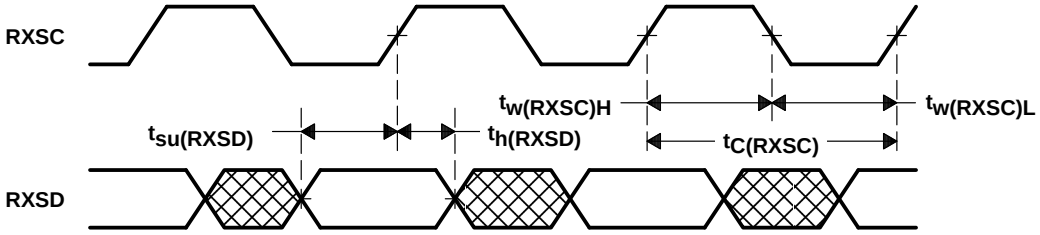


Figure 1. Line-Side Input Clock and Data

		MIN	NOM	MAX	UNIT
$t_{w(RXF)}$	Pulse duration, RXF		51.44		ns
$t_{w(RXBC)H}$	Pulse duration, RXBC high	23			ns
$t_{w(RXBC)L}$	Pulse duration, RXBC low	23			ns
$t_{c(RXBC)}$	Clock cycle time, RXBC		51.44		ns
$t_{d(RXBD)}$	Delay time, RXBD after RXBC↓	–1		6	ns
$t_{d(RXF)}$	Delay time, RXF↑ after RXBC↓	0		6	ns

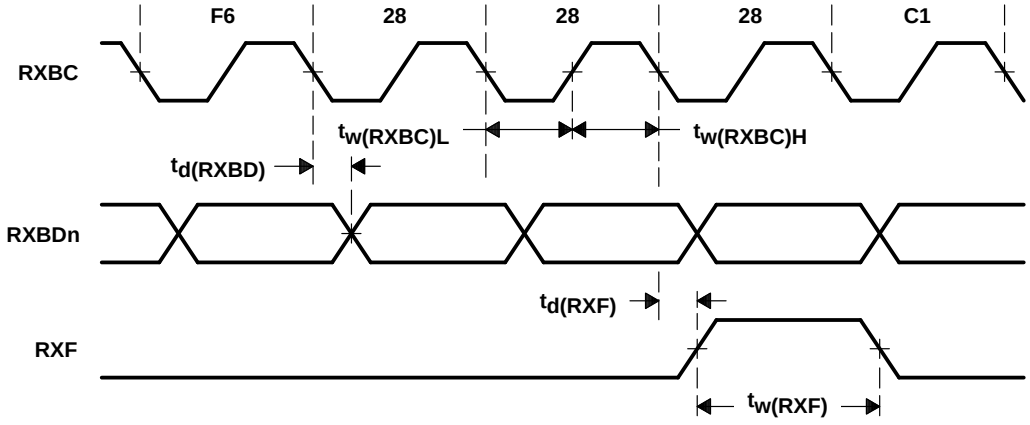


Figure 2. Terminal-Side Byte Output

timing requirements (see Figures 3 and 4) (continued)

		MIN	NOM	MAX	UNIT
$t_{w(TXBC)H}$	Pulse duration, TXBC high	18			ns
$t_{w(TXBC)L}$	Pulse duration, TXBC low	18			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		51.44		ns
$t_{su(TXBD)1}$	Setup time, TXBD before TXBC↓	5			ns
$t_{h(TXBD)1}$	Hold time, TXBD after TXBC↓	5			ns
$t_{su(TXF)1}$	Setup time, $\overline{TXF}$ before TXBC↓	5			ns
$t_{h(TXF)1}$	Hold time. $\overline{TXF}$ before TXBC↓	5			ns

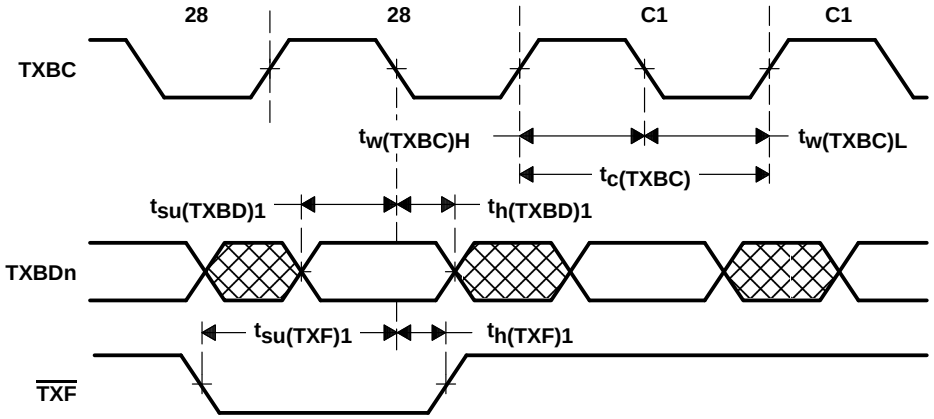


Figure 3. Terminal-Side Byte Input (TPINV low)

		MIN	NOM	MAX	UNIT
$t_{w(TXBC)H}$	Pulse duration, TXBC high	18			ns
$t_{w(TXBC)L}$	Pulse duration, TXBC low	18			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		51.44		ns
$t_{su(TXBD)2}$	Setup time, TXBD before TXBC↑	5			ns
$t_{h(TXBD)2}$	Hold time, TXBD after TXBC↑	5			ns
$t_{su(TXF)2}$	Setup time, $\overline{TXF}$ before TXBC↑	5			ns
$t_{h(TXF)2}$	Hold time, $\overline{TXF}$ after TXBC↑	5			ns

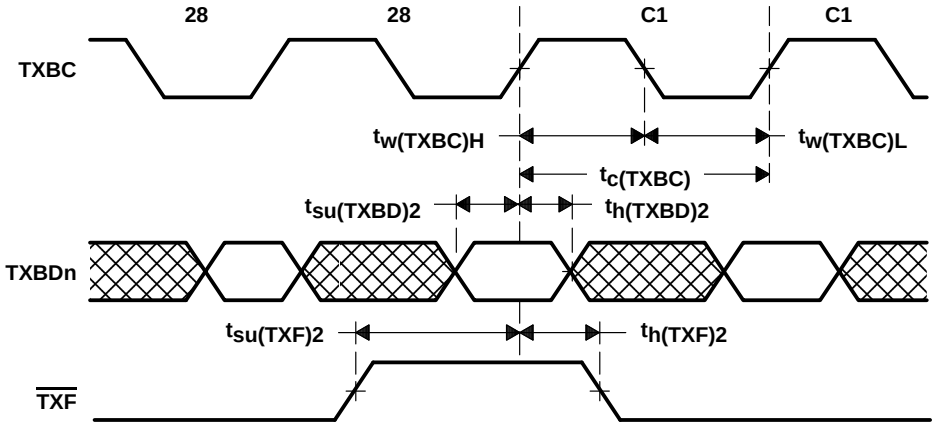


Figure 4. Terminal-Side Byte Input (TPINV high)

timing requirements (see Figures 5 and 6) (continued)

		MIN	NOM	MAX	UNIT
$t_{w(RXF)}$	Pulse duration, RXF high		51.44		ns
$t_{w(RXBC)H}$	Pulse duration, RXBC high	9			ns
$t_{w(RXBC)L}$	Pulse duration, RXBC low	9			ns
$t_{c(RXBC)}$	Clock cycle time, RXBC		25.72		ns
$t_{d(RXBD)}$	Delay time, RXBD after RXBC↓	–1		6	ns
$t_{d(RXF)}$	Delay time, RXF↑ after RXBC↓	0		6	ns

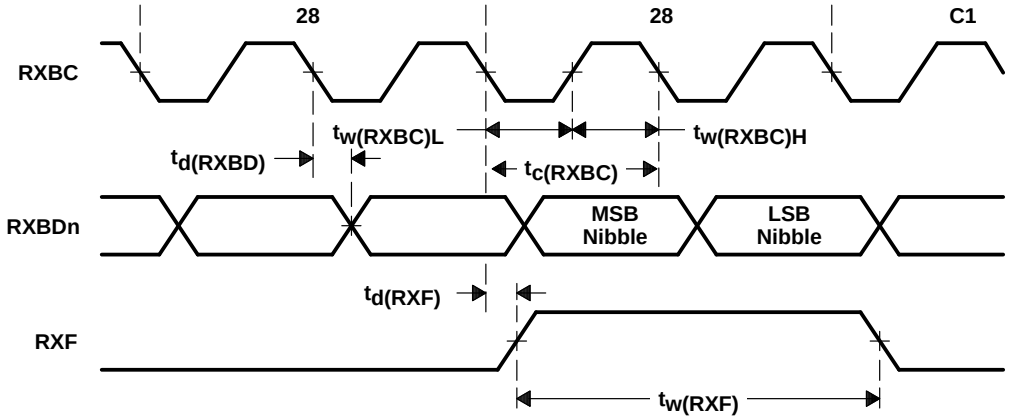


Figure 5. Terminal-Side Nibble Output

		MIN	NOM	MAX	UNIT
$t_{w(TXBC)H}$	Pulse duration, TXBC high	9			ns
$t_{w(TXBC)L}$	Pulse duration, TXBC low	9			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		25.72		ns
$t_{su(TXBD)3}$	Setup time, TXBD before TXBC↓	5			ns
$t_{h(TXBD)3}$	Hold time, TXBD after TXBC↓	5			ns
$t_{su(TXF)3}$	Setup time, $\overline{TXF}$ before TXBC↓	5			ns
$t_{h(TXF)3}$	Hold time, $\overline{TXF}$ after TXBC↓	5			ns

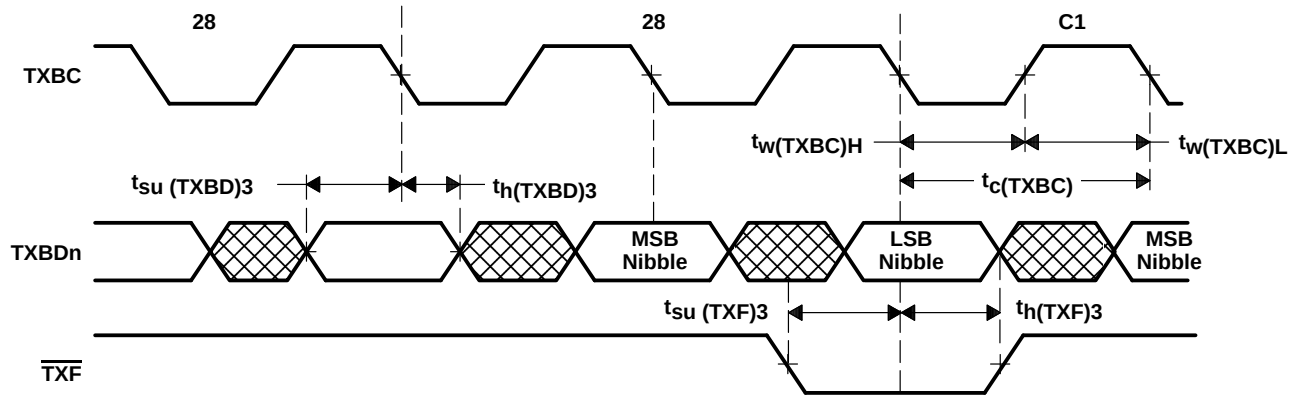


Figure 6. Terminal-Side Nibble Input (TPINV low)

timing requirements (see Figures 7 and 8) (continued)

		MIN	NOM	MAX	UNIT
$t_{w(TXBC)H}$	Pulse duration, TXBC high	9			ns
$t_{w(TXBC)L}$	Pulse duration, TXBC low	9			ns
$t_{c(TXBC)}$	Clock cycle time, TXBC		25.72		ns
$t_{su(TXBD)4}$	Setup time, TXBD before TXBC↑	5			ns
$t_{h(TXBD)4}$	Hold time, TXBD after TXBC↑	5			ns
$t_{su(TXF)4}$	Setup time, $\overline{TXF}$ before TXBC↑	5			ns
$t_{h(TXF)4}$	Hold time, $\overline{TXF}$ before TXBC↑	5			ns

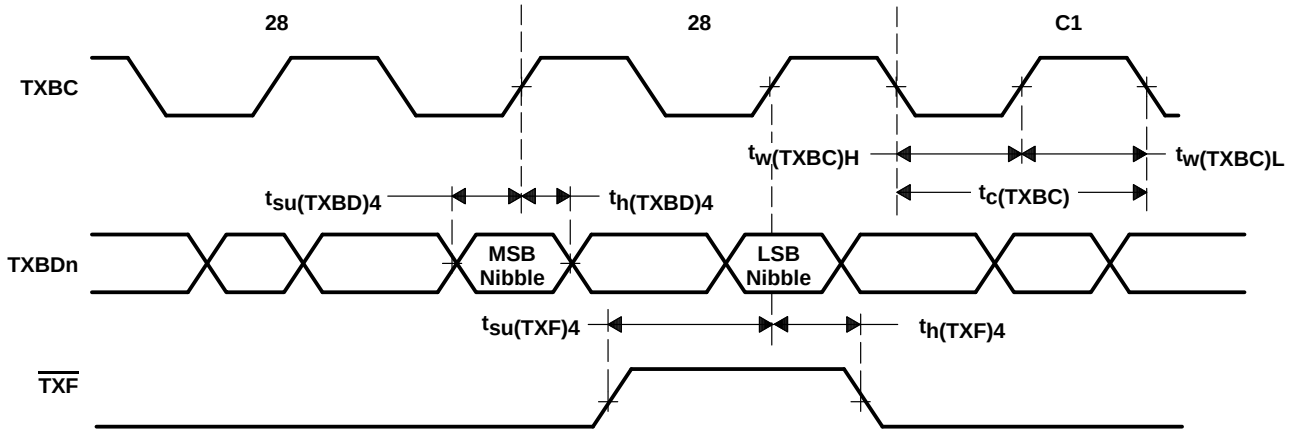


Figure 7. Terminal-Side Nibble Input (TPINV high)

		MIN	NOM	MAX	UNIT
$t_{w(TXRF)L}$	Pulse duration, $\overline{TXRF}$ low		51.44		ns
$t_{w(TXRC)H}$	Pulse duration, TXRC high	23			ns
$t_{w(TXRC)L}$	Pulse duration, TXRC low	23			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		51.44		ns
$t_{d(TXRF)}$	Delay time, $\overline{TXRF}$↓ after TXRC↑	0		6	ns

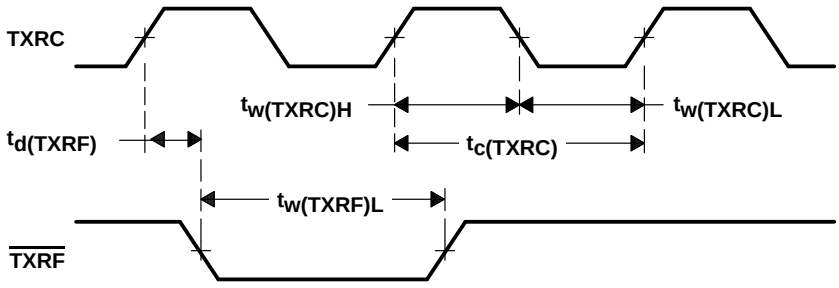


Figure 8. Terminal-Side Byte Reference Signals Output (TPINV Low)

timing requirements (see Figures 9 and 10) (continued)

		MIN	NOM	MAX	UNIT
$t_{w(TXRF)H}$	Pulse duration, $\overline{TXRF}$ high		51.44		ns
$t_{w(TXRC)H}$	Pulse duration, TXRC high	23			ns
$t_{w(TXRC)L}$	Pulse duration, TXRC low	23			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		51.44		ns
$t_{d(TXRF)}$	Delay time, $\overline{TXRF}\uparrow$ after TXRC$\uparrow$	0		6	ns

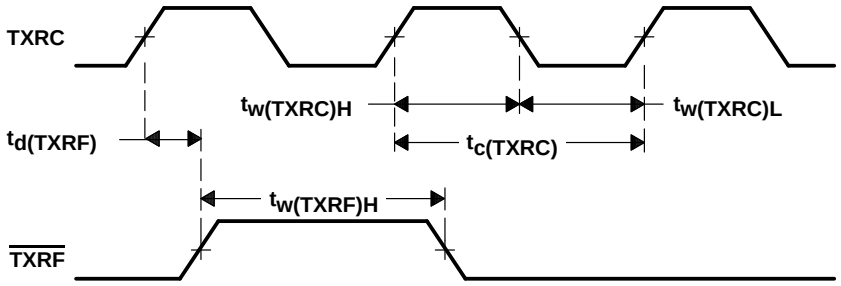


Figure 9. Terminal-Side Byte Reference Signals Output (TPINV High)

		MIN	NOM	MAX	UNIT
$t_{w(TXRF)}$	Pulse duration, $\overline{TXRF}$		25.72		ns
$t_{w(TXRC)H}$	Pulse duration, TXRC high	9			ns
$t_{w(TXRC)L}$	Pulse duration, TXRC low	9			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		25.72		ns
$t_{d(TXRF)}$	Delay time, $\overline{TXRF}\downarrow$ after TXRC$\uparrow$	0		6	ns

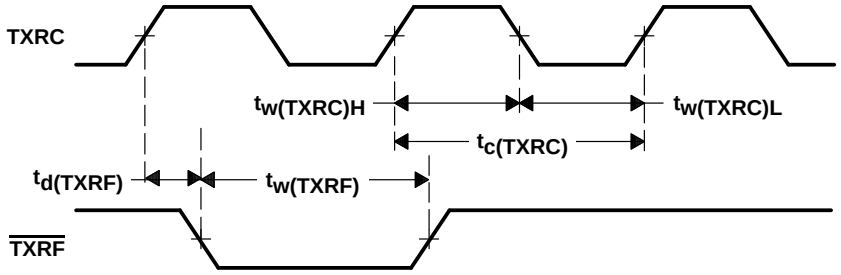


Figure 10. Terminal-Side Nibble Reference Signals Output (TPINV low)

timing requirements (see Figures 11, 12, and 13) (continued)

		MIN	NOM	MAX	UNIT
$t_{w(TXRF)2}$	Pulse duration, $\overline{TXRF}$		25.72		ns
$t_{w(TXRC)H}$	Pulse duration, TXRC high	9			ns
$t_{w(TXRC)L}$	Pulse duration, TXRC low	9			ns
$t_{c(TXRC)}$	Clock cycle time, TXRC		25.72		ns
$t_{d(TXRF)}$	Delay time, $\overline{TXRF}\uparrow$ after TXRC$\downarrow$	0		6	ns

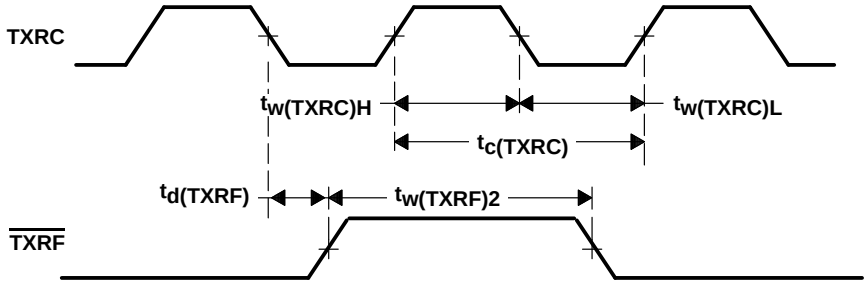


Figure 11. Terminal-Side Nibble Reference Signals Output (TPINV high)

		MIN	MAX	UNIT
$t_{d(OOF/LOF)}$	Delay time, OOF/LOF after $\overline{OOFN}\uparrow$	0	312	ns
$t_{w(OOFN)}$	Pulse duration, $\overline{OOFN}$	105		ns

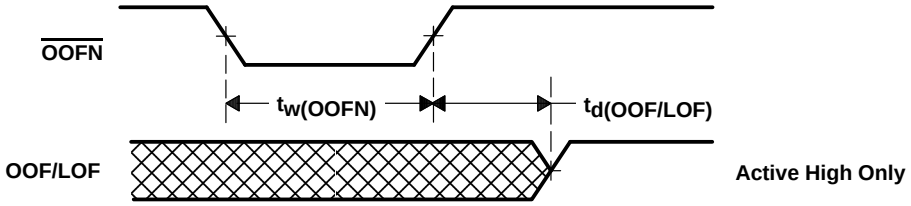


Figure 12. $\overline{OOFN}$ Resetting Frame

		MIN	MAX	UNIT
$t_{d(TXRC)R}$	Delay time, TXRC after $\overline{RESET}\uparrow$	6	30	ns
$t_{d(TXRF)}$	Delay time, $\overline{TXRF}\downarrow$ after TXRC$\uparrow$	0	6	ns
$t_{w(RESET)}$	Pulse duration, $\overline{RESET}$ low	105		ns

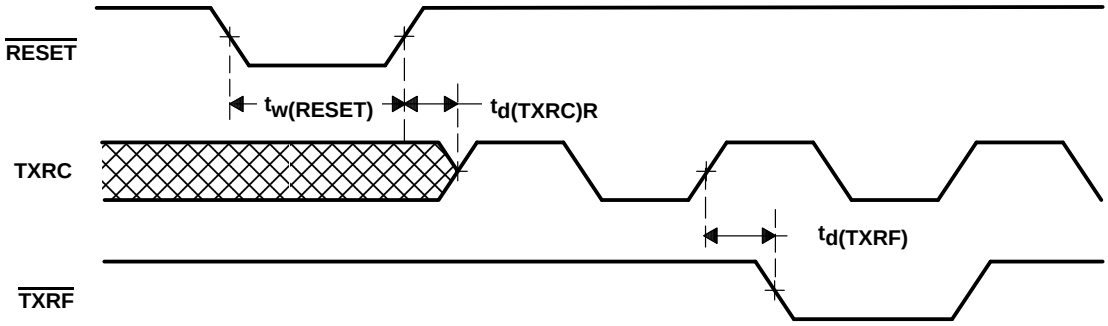


Figure 13. $\overline{RESET}$ Effect of Reference Clock and Frame (TPINV low)

timing requirements (see Figures 14 and 15) (continued)

		MIN	MAX	UNIT
$t_{d(TXRC)R}$	Delay time, TXRC after $\overline{RESET}\uparrow$	6	30	ns
$t_{d(TXRF)}$	Delay time, $\overline{TXRF}\uparrow$ after TXRC$\uparrow$	0	6	ns
$t_{w(RESET)}$	Pulse duration, $\overline{RESET}$	105		ns

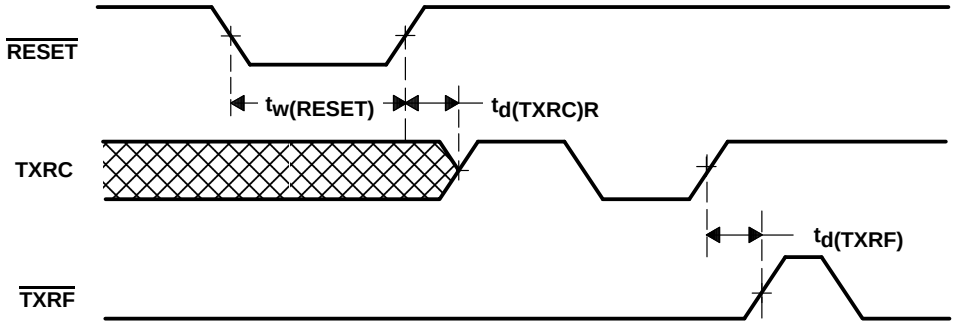
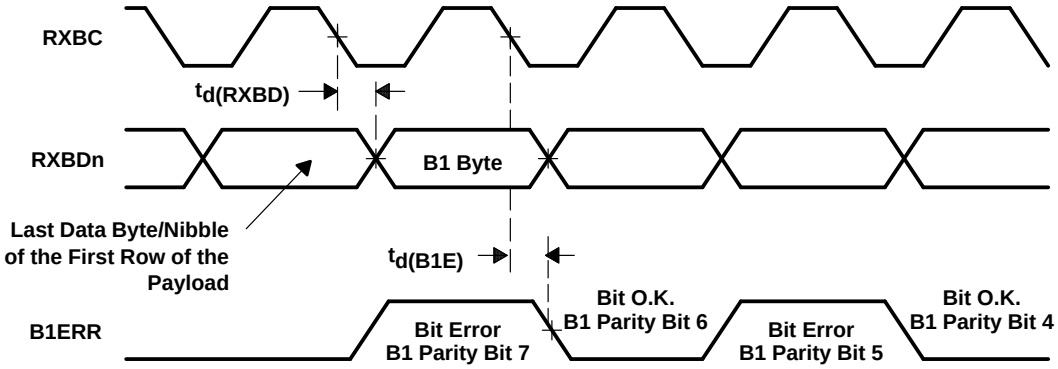


Figure 14. $\overline{RESET}$ Effect of Reference Clock and Frame (TPINV hIgh)

		MIN	MAX	UNIT
$t_{d(RXBD)}$	Delay time, RXBD after RXBC$\downarrow$	0	6	ns
$t_{d(B1E)}$	Delay time, B1ERR$\downarrow$ after RXBC$\downarrow$	0	6	ns

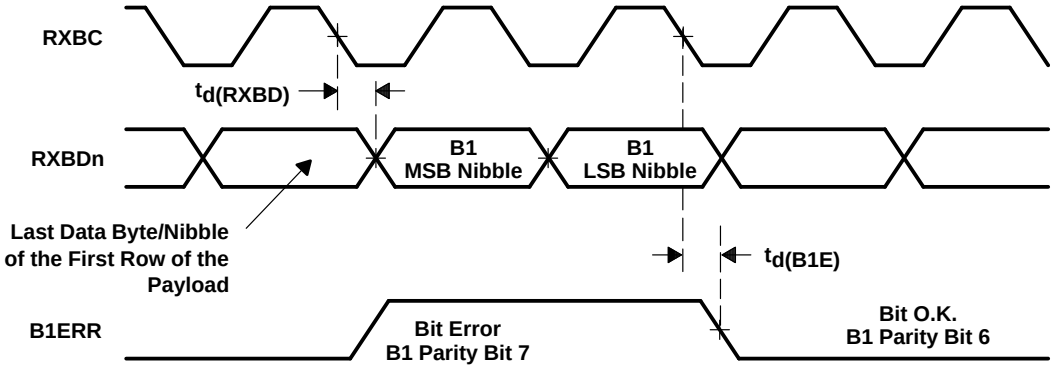


NOTE: Four time slots of B1ERR output are shown; up to eight bits may be in error in a given frame.

Figure 15. B1 Error Pulse Timing – Byte Mode

timing requirements (see Figures 16 and 17) (continued)

		MIN	MAX	UNIT
$t_{d(RXBD)}$	Delay time, RXBD after RXBC↓	0	6	ns
$t_{d(B1E)}$	Delay time, B1ERR↓ after RXBC↓	0	6	ns



NOTE: Four time slots of B1ERR output are shown; up to eight bits may be in error in a given frame.

Figure 16. B1 Error Pulse Timing – Nibble Mode

		MIN	NOM	MAX	UNIT
$t_{w(TXSC)L}$	Pulse duration, TXSC low	2.9			ns
$t_{w(TXSC)H}$	Pulse duration, TXSC high	2.9			ns
$t_{c(TXSC)}$	Clock cycle time, TXSC		6.43		ns
$t_{su(TXSD)}$	Setup time, TXSD before TXSC↑	1			ns
$t_{h(TXSD)}$	Hold time, TXSD after TXSC↑	1.25			ns

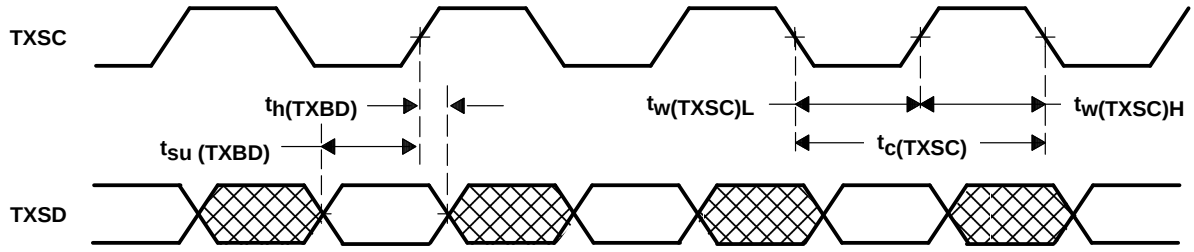


Figure 17. Line-Side PECL Output Timing

timing requirements (see Figure 18 and 19) (continued)

		MIN	NOM	MAX	UNIT
$t_{d(RXRF)}$	Delay time, $\overline{RXRF}\uparrow$ after $\overline{RESET}\uparrow$	51.44		130	ns
$t_{w(RXRF)}$	Pulse duration, $\overline{RXRF}$		51.44		ns

Figure 18. $\overline{RESET}$ Receive Reference Timing

		MIN	NOM	MAX	UNIT
$t_{c(HSCK)}$	Clock cycle time, HSCK		6.43		ns
$t_{w(HSCK)H}$	Pulse duration, HSCK high	2.9			ns
$t_{w(HSCK)L}$	Pulse duration, HSCK Low	2.9			ns

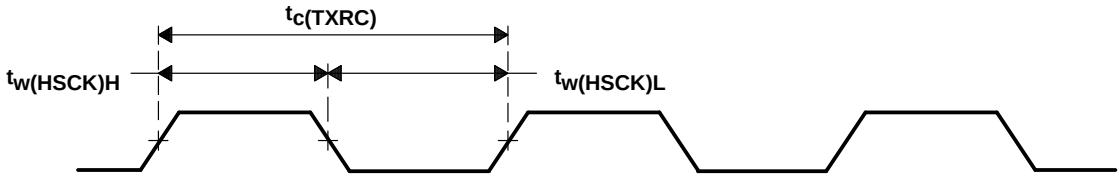


Figure 19. HSCK Input

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.