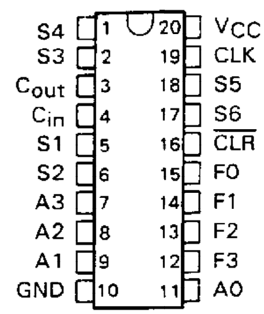
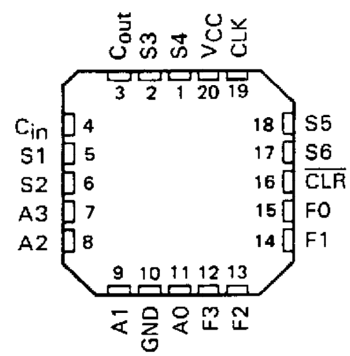
SDLS212 D2112, MARCH 1976—REVISED OCTOBER 1980

- 4-Bit Slice is Cascadable to N-Bits
- Designed Specifically for Microcontroller/ Next-Address Generator Functions
- Increment/Decrement by One (Immediate or Direct Symbolic Addressing Modes)
- Offset, Vector, or Branch (Indexed or Relative Addressing Modes)
- Store Up to Four Returns or Links (Program Return Address from Subroutine)
- Program start or Initialize (Return to Zero or Clear Mode)
- On-Chip Edge-Triggered Output Register (Provides Steady-State Micro-Address/ Instruction)
- High-Density 20-Pin Dual-in-Line Package with 300-Mil Row Pin Spacing

SN54S482 . . . J PACKAGE
SN74S482 . . . J OR N PACKAGE
(TOP VIEW)



SN54S482 . . . FH PACKAGE
SN74S482 . . . FN PACKAGE
(TOP VIEW)

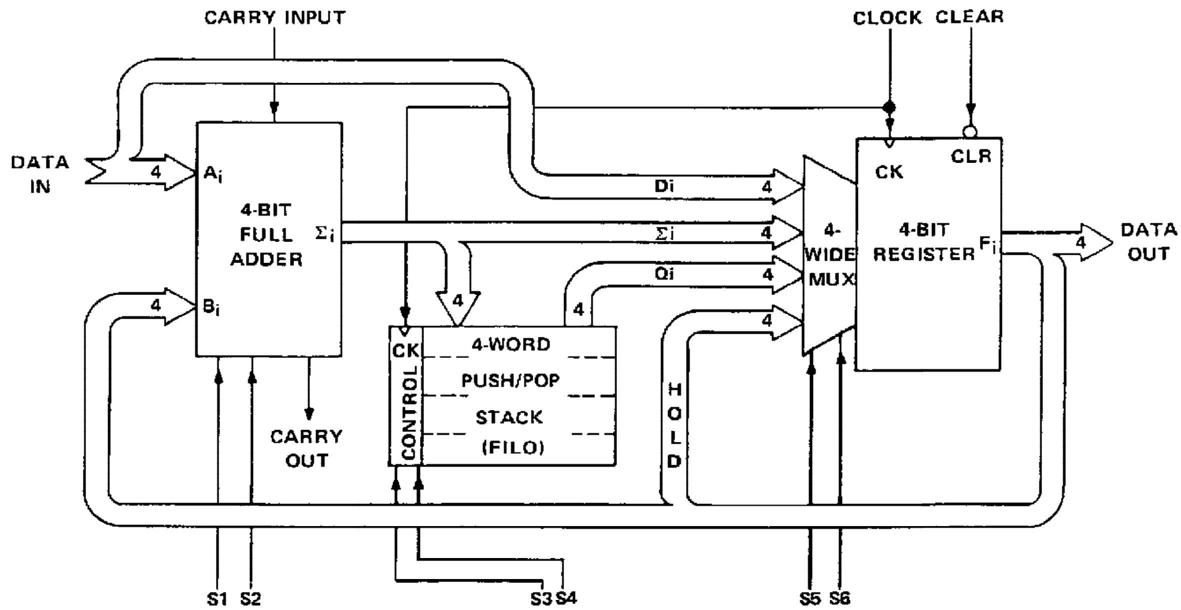


description

The 'S482 is a high-performance Schottky TTL 4-bit-slice control element for use in any computer/control application requiring the coupling of high-performance bipolar speeds with the flexibility of microprogram control and bit-slice expandability. When used as a next-address generator, two 'S482 elements can address up to 256 words of microprogram; three elements can address up to 4096 words of microprogram; or a number of 'S482 elements can generate N words in multiples of four lines.

Comprised of an output register, push-pop stack, and a full adder, the 'S482 provides the capability to implement multiway testing needed to generate or to determine and select the source of the next function of microprogram address.

functional block diagram



output register and source functions

The 4-bit edge-triggered register provides a steady-state output throughout each system clock cycle. An asynchronous clear extends the multiway testing to directly implement system initialization at ROM address zero.

Two source-select lines (S5, S6) provide the output register with access to either the current instruction (no change), an operand or address stored in the push-pop stack, the output of a four-function full adder, or a direct data-in address port. The sources and functions are summarized in Table I and II.

In bus applications, provision must be made to control negative spikes. When low, the output latches can be disturbed if the outputs are forced more negative than −0.5 V.

TABLE I. REGISTER-SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (Di)
L	H	FULL ADDER OUTPUTS (Σi)
H	L	PUSH-POP STACK OUTPUTS (Qi)
H	H	REGISTER OUTPUTS (HOLD)

H ≡ high level, L ≡ low level

TABLE II. PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	Di
	L	L	L	H	↑	H	QiA0*	Σi
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	Σi*	Di
	L	H	L	H	↑	H	Σi*	Σi
	L	H	H	L	↑	H	Σi*	QiA0
	L	H	H	H	↑	H	Σi*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	Di
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i = 3, 2, 1, 0
Ai = Data inputs
QiA = Push-pop stack word A output (internal)
QiA0 = the level of Qi before the indicated inputs conditions were established.

Fi = Device outputs
Fi0 = the level of Fi before the indicated input conditions were established
Σi = Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QiD, QiD0 → QiC, QiC0 → QiB, QiB0 → QiA
‡QiA0 → QiB, QiB0 → QiC, QiC0 → QiD

push-pop stack control

The 4-word push-pop stack can be used for nesting up to four levels of program or return (link) addresses. In the load mode, the first (top) word is filled with new data from the output of the full adder, and no push occurs meaning that previous data at that location is lost. However, all other word locations in the push-pop stack remain unchanged. In the push mode, the new word is again entered in the first (top) location; however, previous data residing in the top three words are pushed down one word location and retained at their new locations. The bottom word is written over and lost.

In the pop mode, words in the push-pop stack move up one location on each clock transition. A unique function is provided by the bottom (fourth) register as its content is retained during the pop mode, and after 3 clock transitions, all words in the stack are filled with the operand/address that occupied the bottom register.

The operand/address will remain available indefinitely if stack functions are limited to the pop or hold modes.

The push-pop stack functions are shown in Tables II and III.

TABLE III. PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL.		REG.	REG.	REG.	REG.	INPUT/
		S3	S4	D	C	B	A	OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	Σi IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← Σi	Σi IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

μlink operations show previous data location after clock transition.

full adder

The four-function full adder is controllable from select inputs S1 and S2 to perform:

A or B incrementation, or decrementation of B
Unconditional jumps or relative offsets
No change
Return to zero or one

Incrementation can be implemented by forcing a carry (high) into the ALU. In this mode either of the following options are possible:

1. Increment (A plus zero plus carry)
2. Increment B (zero plus B plus carry), or decrement B (all highs at A then A plus B with carry input low and disregard, don't use, carry out)
3. Increment the jump or offset (A plus B plus carry)
4. Start at zero or one and increment on each clock (select zero plus zero plus carry, then select zero plus B plus carry), or set register to N and decrement B (see 2 above).
5. No change (carry input is always active and removal of carry combined with either the ALU or register hold mode will retain the current address).

Unconditional jumps can be implemented by applying and selecting the jump directly from the data inputs to the output register. Offset can be accomplished by summing the output register with the offset magnitude (A plus B) with carry low.

The ALU functions are shown in Table IV.

TABLE IV. ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS c-in

compound generator functions

As the function-select lines of the register sources, push-pop stack, and adder are independent, compound functions can be selected to occur on the next clock transition.

Subroutine branches and returns can be simplified by saving the return or link addresses in the push-pop stack. This branch-and-save function can be accomplished on the same clock time as follows:

DATA-IN	ADDER	PUSH-POP STACK	REGISTER SOURCE
Branch address	Zero plus B plus one (S1 = H, S2 = L)	Push (S3 = S4 = H)	Data-in (S5 = S6 = L)

Up to four branches can be made with the return stored in the 4-word push-pop stack.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Off-state output voltage . . . . 5.5 V
Operating free-air temperature range: SN54S482 . . . . −55°C to 125°C
SN74S482 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1. All voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54S482			SN74S482			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	C_{out}			−1			−1	mA
		Any F			−2			−2	mA
I_{OL}	Low-level output current	C_{out}			10			10	mA
		Any F			16			16	mA
t_w	Pulse duration	CLK high or low	50			30			ns
		$\overline{CLR}$ low	15			15			ns
t_{su}	Setup time, before CLK↑	Data-in, S5, S6	0			0			ns
		Data-in via adder to stack	35			30			ns
		Data-in via adder to output latch	25			20			ns
		S1, S2	40			30			ns
		S3, S4	20			15			ns
		$\overline{CLR}$, inactive state	0			0			ns
t_r	CLK input rise time		20			25			ns
t_h	Hold time, after CLK↑	Data-in, S5, S6	30			25			ns
		Data-in via adder	15			10			ns
		S1, S2	15			10			ns
		S3, S4	25			20			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S482 MIN	SN54S482 TYP‡	SN54S482 MAX	SN74S482 MIN	SN74S482 TYP‡	SN74S482 MAX	UNIT
V_{IK}		V_{CC} = MIN,	I_L = −18 mA			−1.2			−1.2	V
V_{OH}	C_{out}	V_{CC} = MIN,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
	Any F	V_{CC} = MIN,	I_{OH} = −2 mA	2.5	3.4		2.7	3.4		
V_{OL}	C_{out}	V_{CC} = MIN,	I_{OL} = 10 mA			0.5			0.5	V
	Any F	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	
I_I		V_{CC} = MIN,	V_I = 5.5 V			1			1	mA
I_{IH}	S1, S2, C_{in}	V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
	S3, S4, S5, S6, CLK					0.1			0.1	mA
	$\overline{CLR}$					0.25			0.25	
	Any A					0.15			0.15	
I_{IL}	S1, S2	V_{CC} = MAX,	V_I = 0.5 V			−1			−1	mA
	C_{in}					−0.8			−0.8	
	S3, S4					−1.2			−1.2	
	Any A, S5, S6					−2			−2	
	$\overline{CLR}$					−4			−4	
	CLK					−2.8			−2.8	
I_{OS}§		V_{CC} = MAX		−40		−110	−40		−110	mA
I_{CC}		V_{CC} = MAX			90	130		90	140	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = MIN to MAX, C_L = 15 pF, R_L = 280 Ω, T_A = MIN to MAX						UNIT
			SN54S482			SN74S482			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Any F		12	30		12	25	ns
t_{PHL}				15	30		15	25	
t_{PHL}	$\overline{CLR}$	Any F		12	25		12	20	ns
t_{PLH}	C_{in}	C_{out}		12	22		12	18	ns
t_{PHL}				10	22		10	18	
t_{PLH}	Any A	C_{out}		17	30		17	25	ns
t_{PHL}				12	30		12	23	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: See General Information Section for load circuit and voltage waveforms.