SN54S350, SN74S350
FOUR-BIT SHIFTER WITH THREE-STATE OUTPUTS

SDLS209

D2745, DECEMBER 1983 — REVISED MARCH 1988

- **Shifts 4-Bits of Data to 0, 1, 2 or 3 Places Under Control of Two Select Lines**
- **Three-State Outputs for Bus Organized Systems**
- **6.5 ns Typical Data Propagation Delay**

description

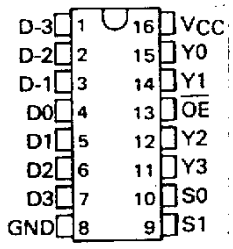
The 'S350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes shifts of the data word. This makes it possible to perform shifts of 0, 1, 2, or 3 places on words of any length, with suitable interconnection.

A 7-bit data word is introduced at the D inputs and is shifted according to the code applied to the select inputs S0 and S1. Y0 through Y3 are 3-state outputs controlled by an output enable, $\overline{OE}$. When $\overline{OE}$ is low, the outputs follow the selected data inputs; when $\overline{OE}$ is high, the outputs are in a high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical with zeroes pulled in at either or both ends of the shifting field, arithmetic with the sign bit repeated during a shift down, or end-around with the data word forming a continuous loop.

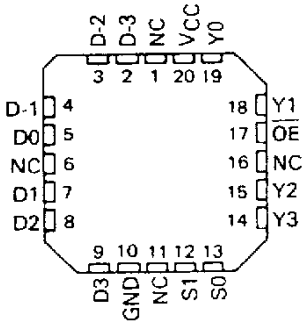
FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{OE}$	S1	S0	Y0	Y1	Y2	Y3
H	X	X	Z	Z	Z	Z
L	L	L	D0	D1	D2	D3
L	L	H	D-1	D0	D1	D2
L	H	L	D-2	D-1	D0	D1
L	H	H	D-3	D-2	D-1	D0

SN54S350 . . . J PACKAGE
SN74S350 . . . D OR N PACKAGE
(TOP VIEW)



SN54S350 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic equations

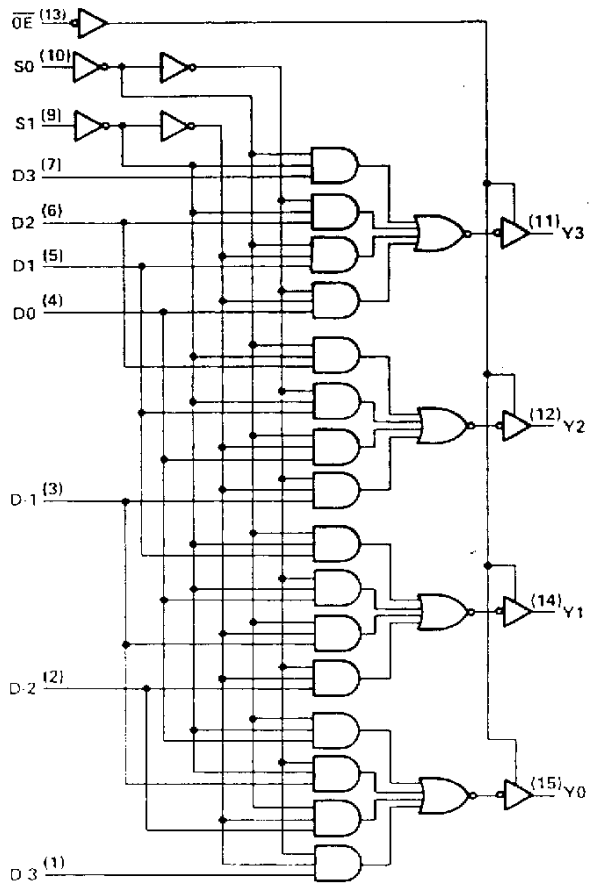
$$Y0 = \overline{S0}\,\overline{S1}\,D0 + S0\,\overline{S1}\,D\text{-}1 + \overline{S0}\,S1\,D\text{-}2 + S0\,S1\,D\text{-}3$$

$$Y1 = \overline{S0}\,\overline{S1}\,D1 + S0\,\overline{S1}\,D0 + \overline{S0}\,S1\,D\text{-}1 + S0\,S1\,D\text{-}2$$

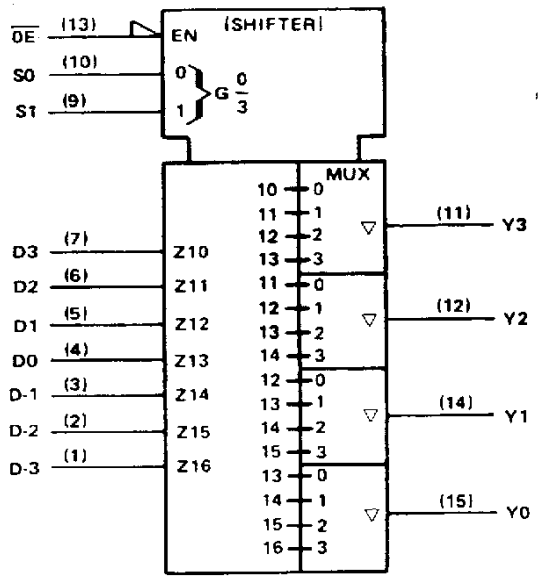
$$Y2 = \overline{S0}\,\overline{S1}\,D2 + S0\,\overline{S1}\,D1 + \overline{S0}\,S1\,D0 + S0\,S1\,D\text{-}1$$

$$Y3 = \overline{S0}\,\overline{S1}\,D3 + S0\,\overline{S1}\,D2 + \overline{S0}\,S1\,D1 + S0\,S1\,D0$$

logic diagram (positive logic)

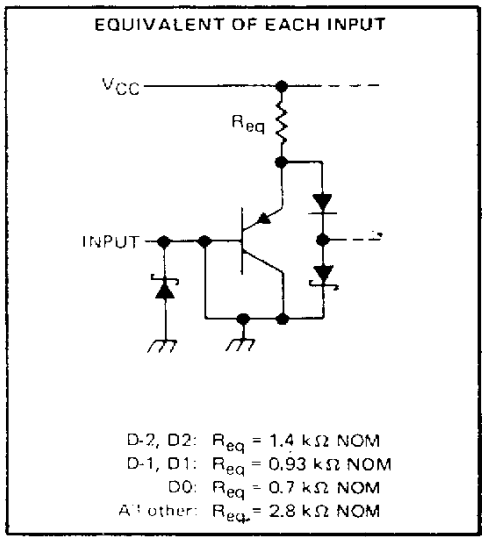


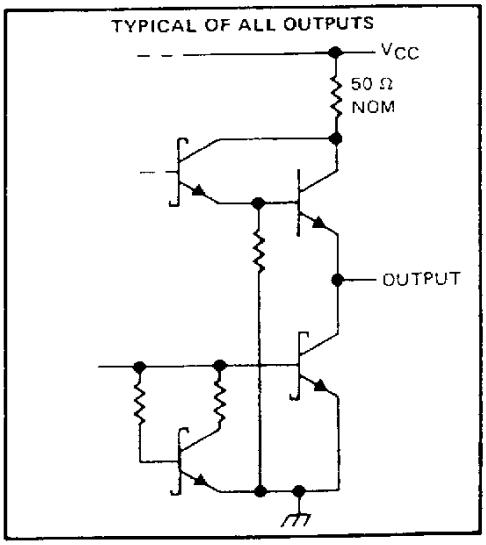
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54S350 . . . . . −55°C to 125°C
SN74S350 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S350			SN74S350			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−6.5	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S350			SN74S350			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_{OZH}		V_{CC} = MAX, V_O = 2.4 V			50			50	μA
I_{OZL}		V_{CC} = MAX, V_O = 0.5 V			−50			−50	μA
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	D-2, D-1, D-0, D1, D2 inputs	V_{CC} = MAX, V_I = 2.7 V			75			75	μA
	All others				50			50	
I_{IL}	D-2, D-1 D-0, D1, D2 inputs	V_{CC} = MAX, V_I = 0.5 V			−3			−3	mA
	All others				−2			−2	
I_{OS}§		V_{CC} = MAX, V_O = 0	−40		−100	−40		−100	mA
I_{CC}		V_{CC} = MAX, V_I = 0 All inputs = GND		60	85		60	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

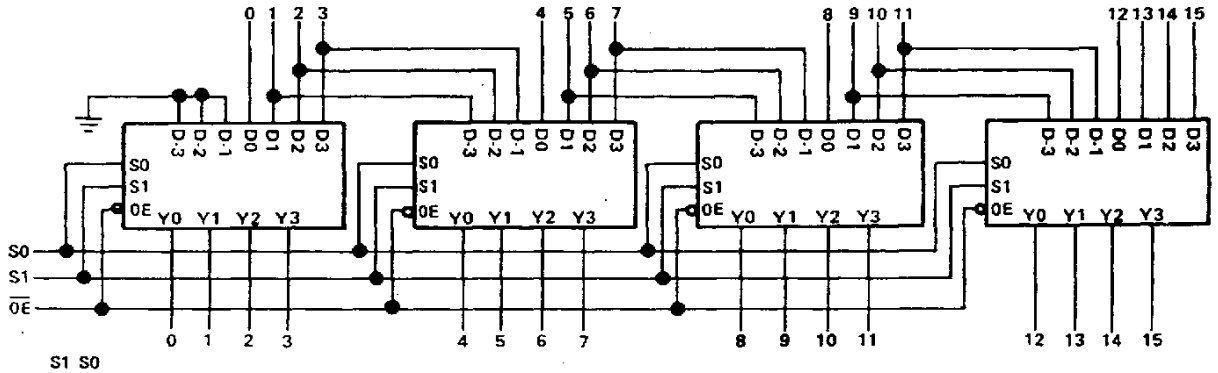
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any Y	R_L = 280 Ω, C_L = 15 pF		5	9	ns
t_{PHL}					8	12	ns
t_{PLH}	Select	Any Y			11	17	ns
t_{PHL}					13	20	ns
t_{PZH}	$\overline{OE}$	Any Y				19.5	ns
t_{PZL}						21	ns
t_{PHZ}	$\overline{OE}$	Any Y	R_L = 280 Ω, C_L = 5 pF		8	13	ns
t_{PLZ}					10	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

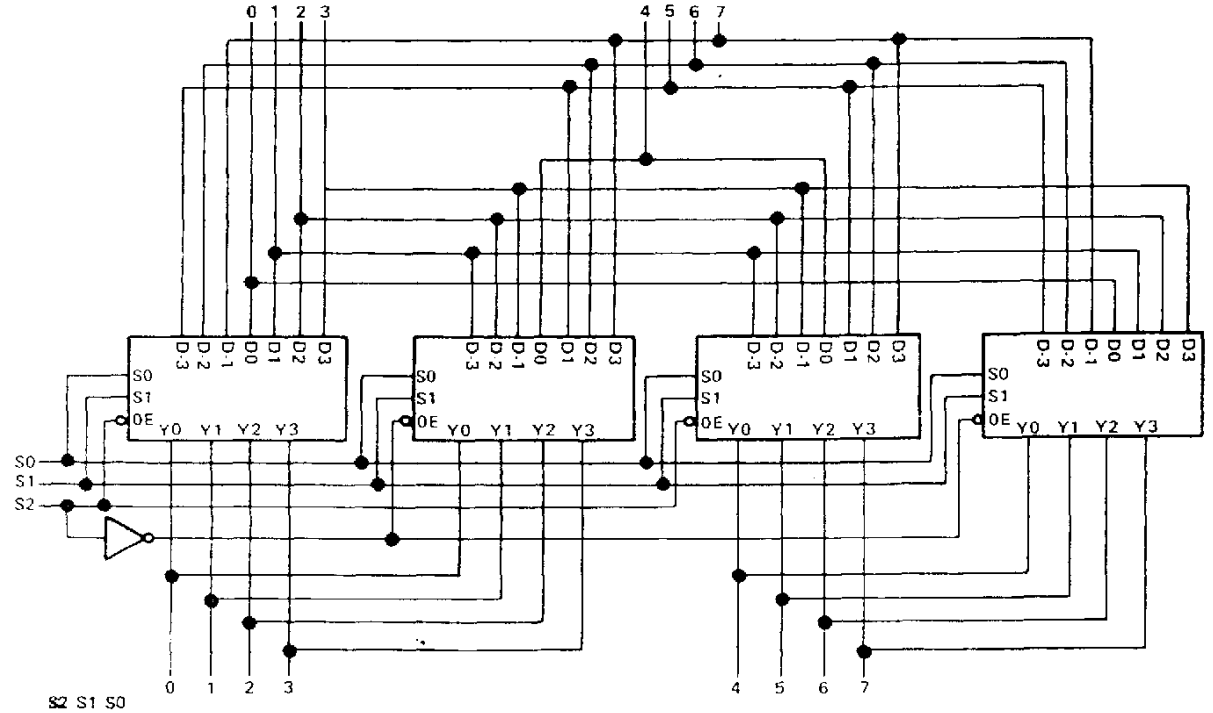
TYPICAL APPLICATION DATA

16-Bit Shift-Up 0 to 3 Places. Zero Backfill



S1	S0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

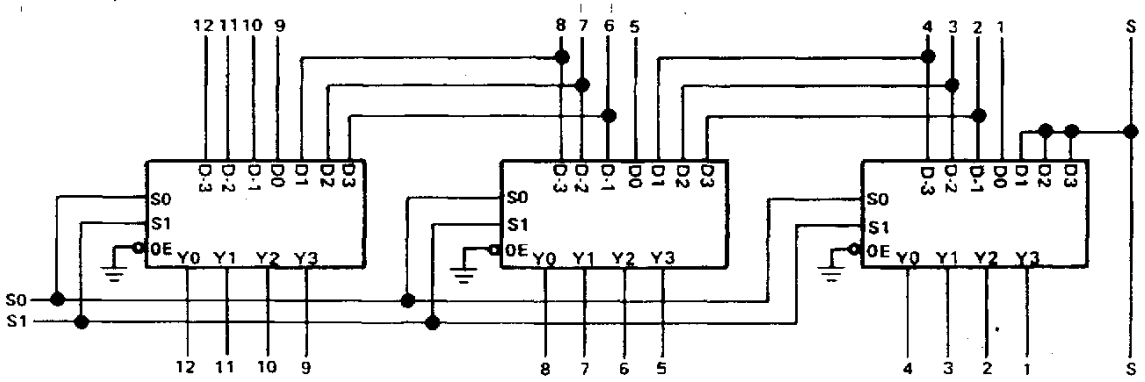
8-Bit End-Around Shift 0 to 7 Places



S2	S1	S0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

TYPICAL APPLICATION DATA

13-Bit Twos Complement Scaler



S1	S0	SCALE
L	L ÷ 8	1/8
H	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H	NO CHANGE 1

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.