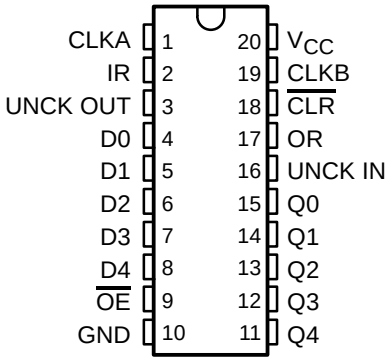
SDLS207 – SEPTEMBER 1976 – REVISED SEPTEMBER 1993

- **Independent Asychronous Inputs and Outputs**
- **16 Words by 5 Bits**
- **DC to 10-MHz Data Rate**
- **3-State Outputs**
- **Packaged in Standard Plastic 300-mil DIPs**

N PACKAGE
(TOP VIEW)



description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words by 5 bits. A memory system using the SN74S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The 3-state outputs controlled by a single output-enable ($\overline{OE}$) input make bus connection and multiplexing easy.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from dc to 10 MHz in a bit-parallel format, word by word.

Reading or writing is done independently utilizing separate asynchronous data clocks. Data can be written into the array on the low-to-high transition of either load-clock (CLKA, CLKB) input. Data can be read out of the array on the low-to-high transition of the unload-clock (UNCK IN) input (normally high). Writing data into the FIFO can be accomplished in one of two manners:

1. In applications not requiring a gated clock control, best results will be achieved by applying the clock input to one of the clocks while tying the other clock input high.
2. In applications needing a gated clock, the load clock (gate control) must be high in order for the FIFO to load on the next clock pulse.

CLKA and CLKB can be used interchangeably for either clock gate control or clock input.

Status of the SN74S225 is provided by three outputs. The input-ready (IR) output monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload-clock (UNCK OUT) output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready (OR), is high when the first word location contains valid data and UNCK IN is high. When UNCK IN goes low, OR will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are 3-state with a common control input ($\overline{OE}$). When $\overline{OE}$ is low, the data outputs are enabled to function as totem-pole outputs. A high logic level forces each data output to a high-impedance state while all other inputs and outputs remain active.The clear ($\overline{CLR}$) input invalidates all data stored in the memory array by clearing the control logic and setting OR to a low logic level on the high-to-low transition of a low-active pulse.

The SN74S225 is characterized for operation from 0°C to 70°C.

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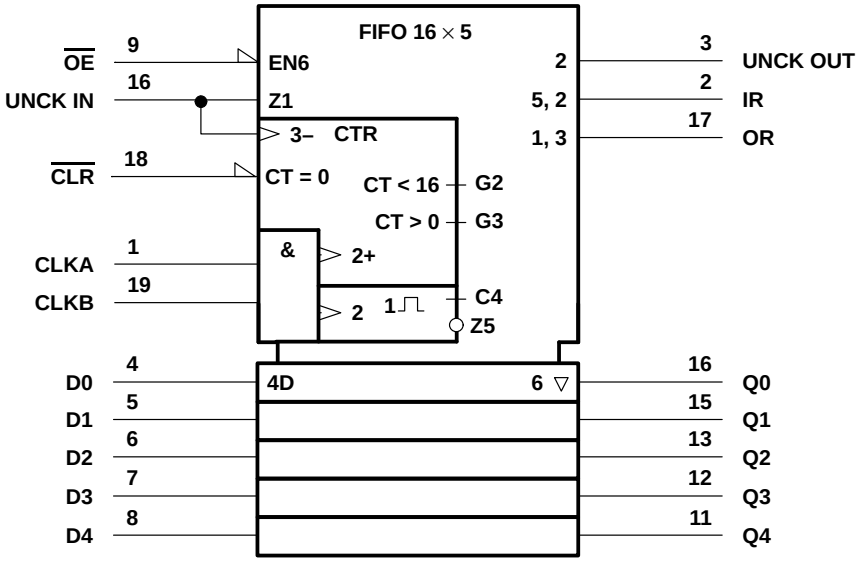
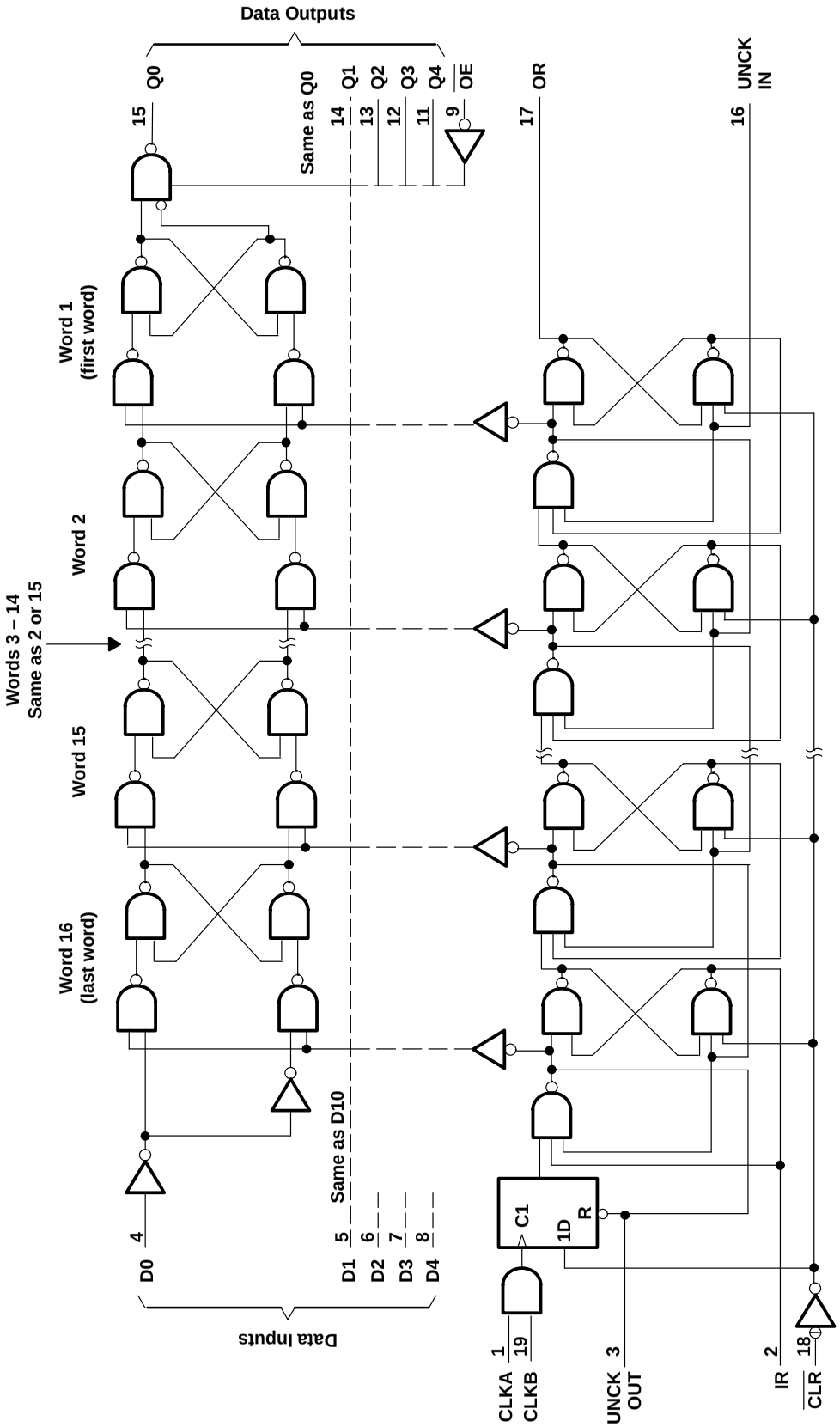
logic symbol†

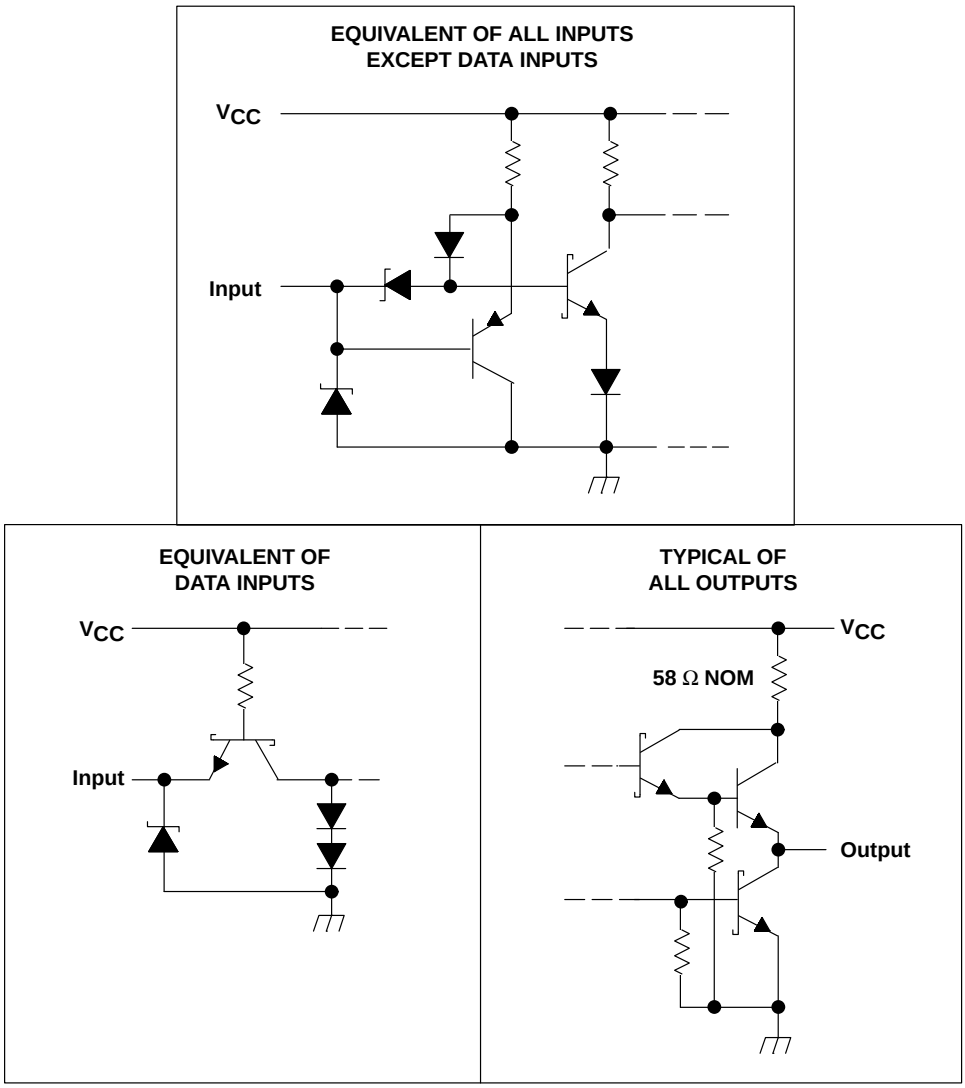


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q outputs			−6.5	mA
		All other outputs			−3.2	
I_{OL}	Low-level output current	Q outputs			16	mA
		All other outputs			8	
t_w	Pulse duration	CLKA or CLKB high	25			ns
		UNCK IN low	7			
		$\overline{CLR}$ low	40			
t_{su}	Set up time before CLKA↑ or CLKB↑	Data (see Note 2)	−20			ns
		$\overline{CLR}$ inactive	25			
t_h	Hold time after CLKA↑ or CLKB↑		70			ns
T_A	Operating free-air temperature		0		70	°C

NOTE 2: Data must be set up within 20 ns after the load clock positive transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA			−1.2	V
V_{OH}	Q outputs	V_{CC} = 4.75 V,	I_{OL} = − 6.5 mA	2.4	2.9		V
	All others	V_{CC} = 4.75 V,	I_{OL} = −3.2 mA	2.4	2.9		
V_{OL}	Q outputs	V_{CC} = 4.75 V,	I_{OL} = 16 mA		0.35	0.5	V
	All others	V_{CC} = 4.75 V,	I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.4 V			50	μA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.5 V			−50	μA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			1	mA
I_{IH}	Data	V_{CC} = 5.25 V,	V_I = 2.7 V			40	μA
	All others					25	
I_{IL}	Data	V_{CC} = 5.25 V,	V_I = 0.5 V			−1	mA
	All others					−0.25	
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0	−30		−100	mA
I_{CC}§		V_{CC} = 5.25 V			80	120	mA

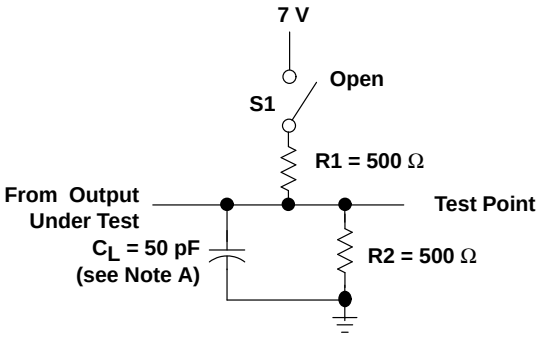
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Duration of the short circuit should not exceed one second.
§ I_{CC} is measured with all inputs grounded and the output open.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}	CLKA		C_L = 30 pF	10	20		MHz
	CLKB			10	20		
	UNCK IN			10	20		
t_w	UNCK OUT			7	14		ns
t_{dis}	$\overline{OE}$	Any Q	C_L = 5 pF		10	25	ns
t_{en}	$\overline{OE}$	Any Q	C_L = 30 pF		25	40	ns
t_{PLH}	UNCK IN	Any Q			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CLKA or CLKB	OR			190	300	ns
t_{PLH}	UNCK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{CLR}$	OR			35	60	ns
	CLKA or CLKB	UNCK OUT			25	45	
	UNCK IN				270	400	
	CLKA or CLKB	IR			55	75	
t_{PLH}	UNCK IN	IR			255	400	ns
	$\overline{CLR}$				16	35	
	OR↑	Any Q			10	20	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

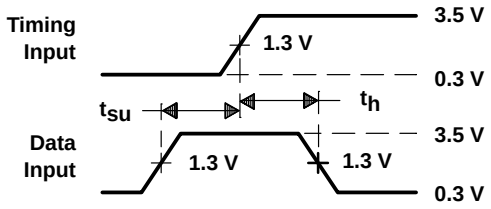
PARAMETER MEASUREMENT INFORMATION



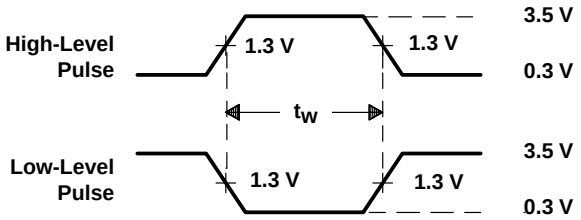
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

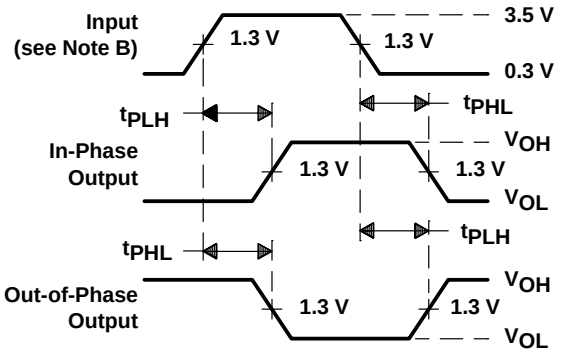
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



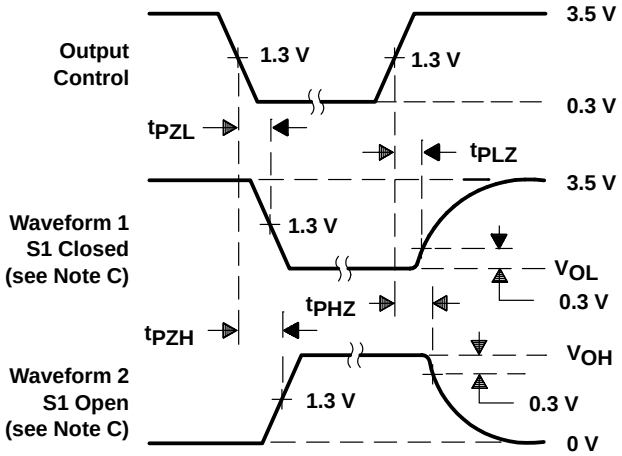
VOLTAGE WAVEFORMS
SET UP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

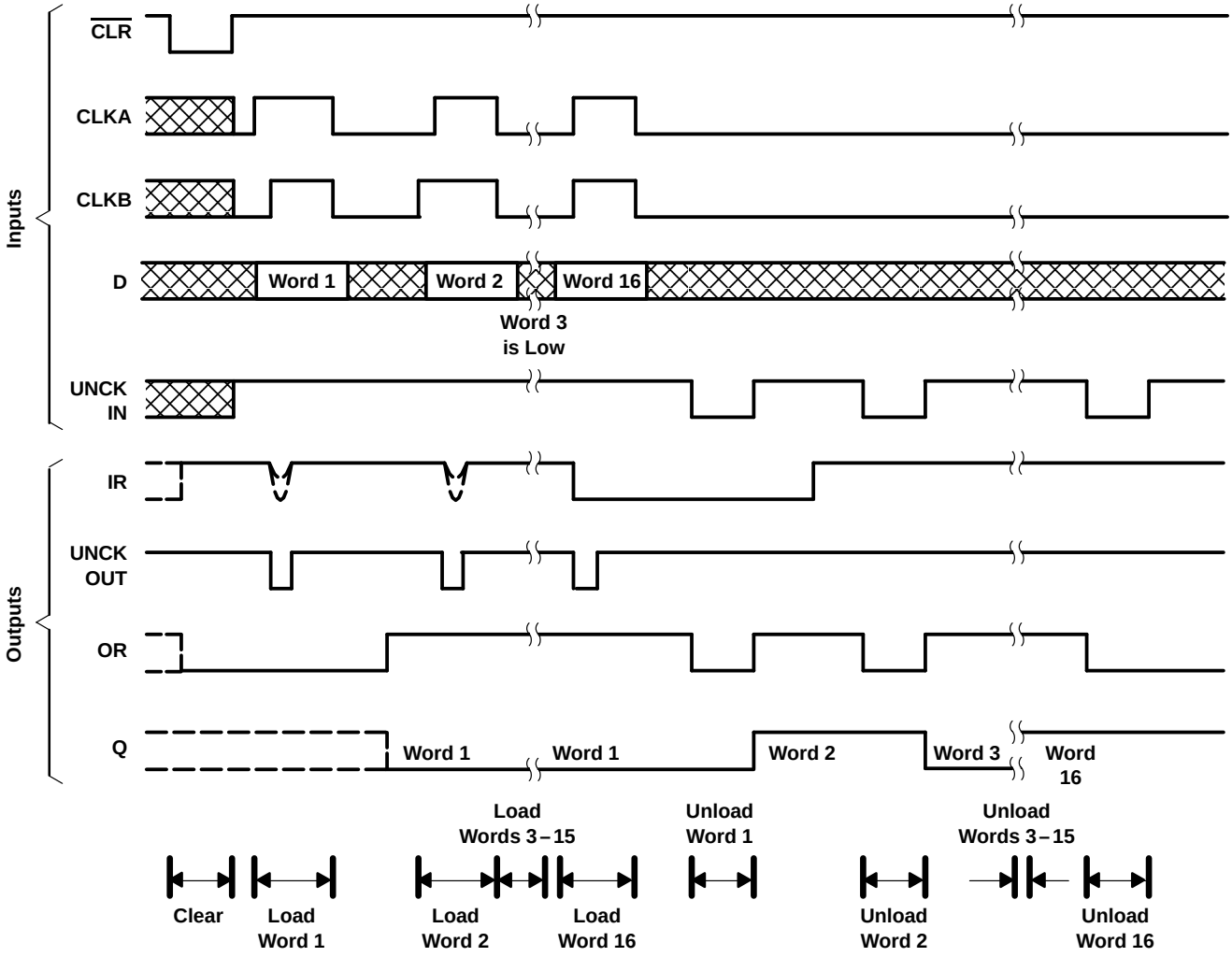


Figure 2. Typical Waveforms for a 16-Word FIFO

APPLICATION INFORMATION

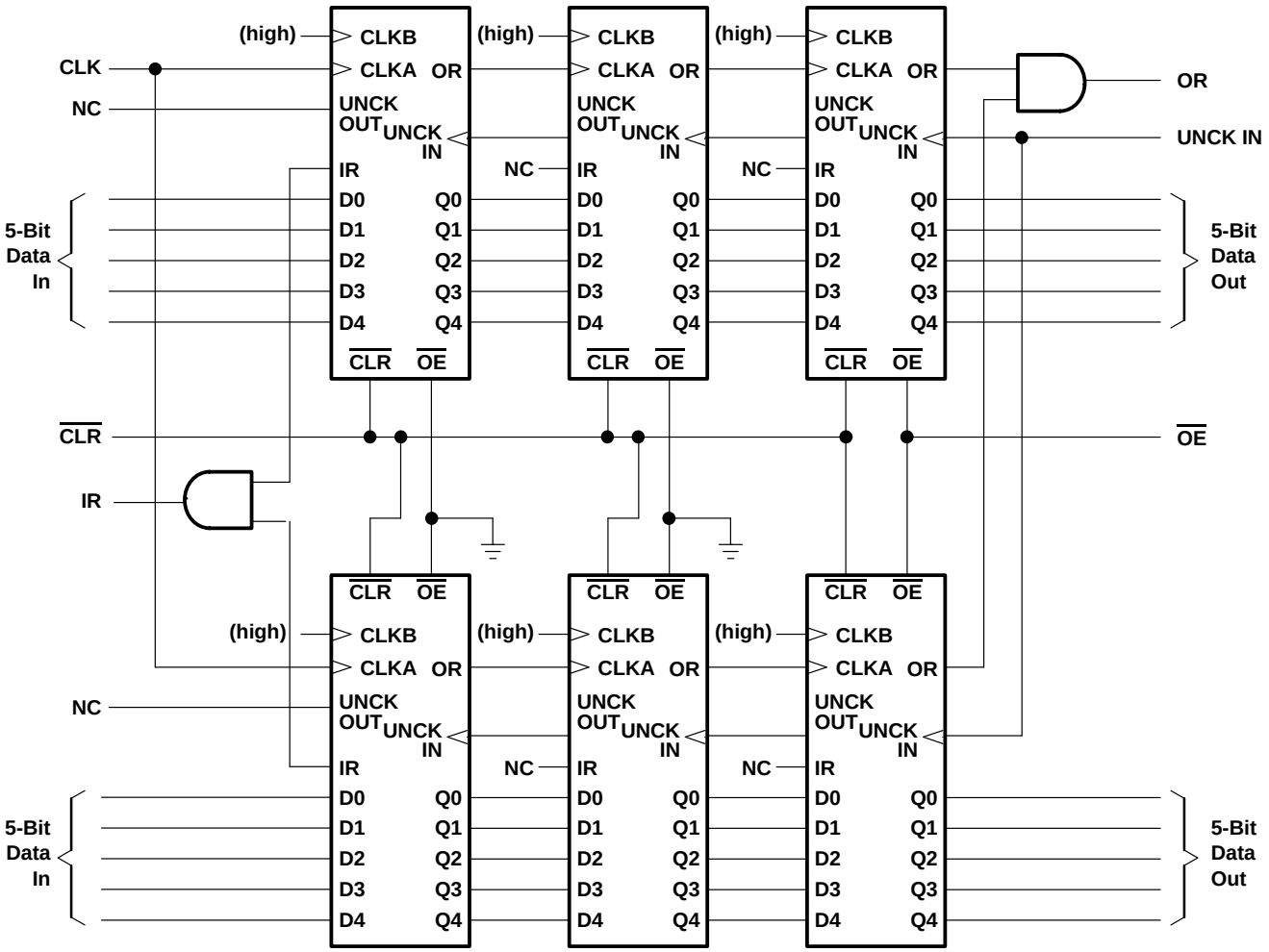


Figure 3. Expanding the SN74S225 FIFO (48 words of 10 bits shown)

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