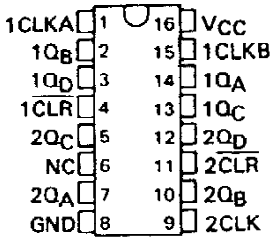
SN54LS68, SN54LS69, SN74LS68, SN74LS69
DUAL 4-BIT DECADE OR BINARY COUNTERS

SDLS196

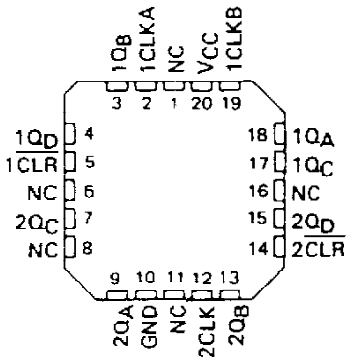
DECEMBER 1983 – REVISED MARCH 1988

- **Heavy Duty Outputs I_{OL} Rated at 8mA/16 mA**
- **Counter One of Either 'LS68 or 'LS69 Has Individual Clicks for the A Flip-Flop**
- **Direct Clear for Each 4-Bit Counter**
- **Guaranteed Maximum Count Frequency is 50 MHz for 'LS69 and 40 MHz for 'LS68**

5N54LS68, SN54LS69 . . . J PACKAGE
SN74LS68, SN74LS69 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS68, SN54LS69 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

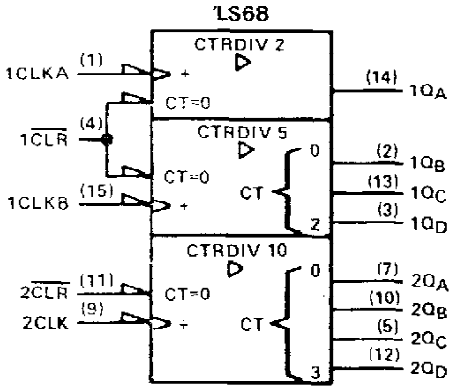
Each of the 'LS68 and 'LS69 circuits contain two four-bit counters. The 'LS68 is a dual decade counter, while the 'LS69 is a dual binary counter. Counter number one of both the 'LS68 and 'LS69 has two clock pins. Clock 1 is for the A flip-flop, while clock 2 is for the B, C, D flip-flops. Counter one of the 'LS68 can perform bi-quinary counting. All $1Q_A$ outputs are rated with sufficient I_{OL} to drive clock 2 while maintaining a full fan-out.

All clocks trigger on the high-to-low transition of the clock pulse. All counters have direct overriding clear pins which, when low, reset Q_A, Q_B, Q_C, and Q_D low regardless of the state of the clock.

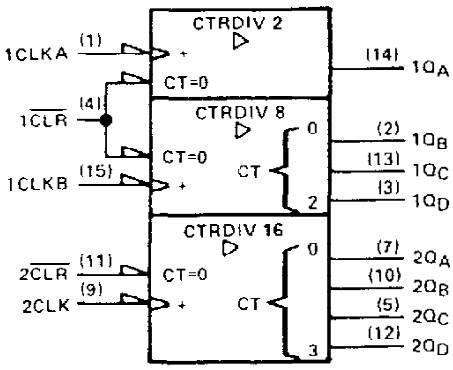
The SN54LS68 and SN54LS69 circuits are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS68 and SN74LS69 circuits are characterized for operation from 0°C to 70°C.

logic symbols†

'LS68



'LS69



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

count sequence tables

'LS68 DECADE COUNTER
BCD COUNT SEQUENCE
(See Note 1)
Applies to Counters 1 & 2

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'LS68 DECADE COUNTER
BI-QUINARY SEQUENCE
(See Note 2)
Applies to Counter 1 only

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

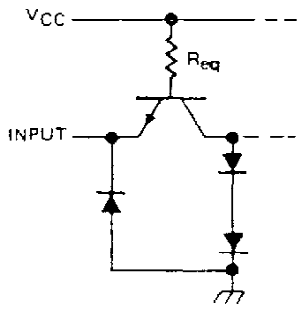
'LS69 BINARY COUNTER
BCD COUNT SEQUENCE
(See Note 3)
Applies to Counters 1 & 2

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: 1. Output $1Q_A$ is connected to 1CLK2 for BCD count.
2. Output $1Q_A$ is connected to 1CLK1 for bi-quinary count.
3. Output $1Q_A$ is connected to 1CLK2 for binary count.

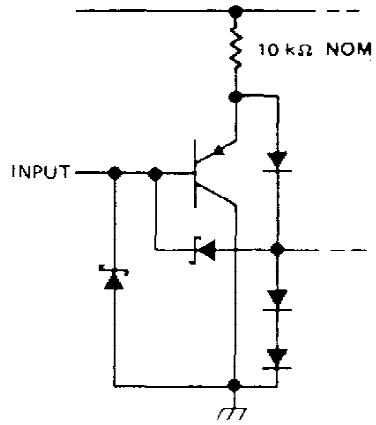
schematics of inputs and outputs

EQUIVALENT OF CLOCK INPUTS

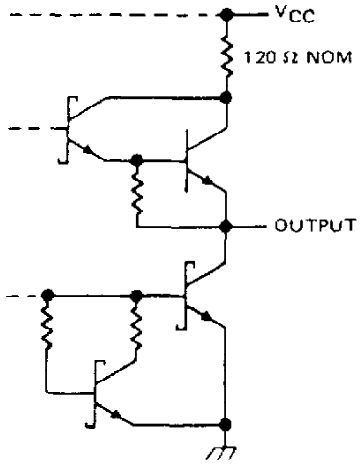


INPUT	R_{eq} NOM
1CLK1, 2CLK	4.5k Ω
1CLK2	7.5k Ω

EQUIVALENT OF $\overline{CLR}$ INPUTS

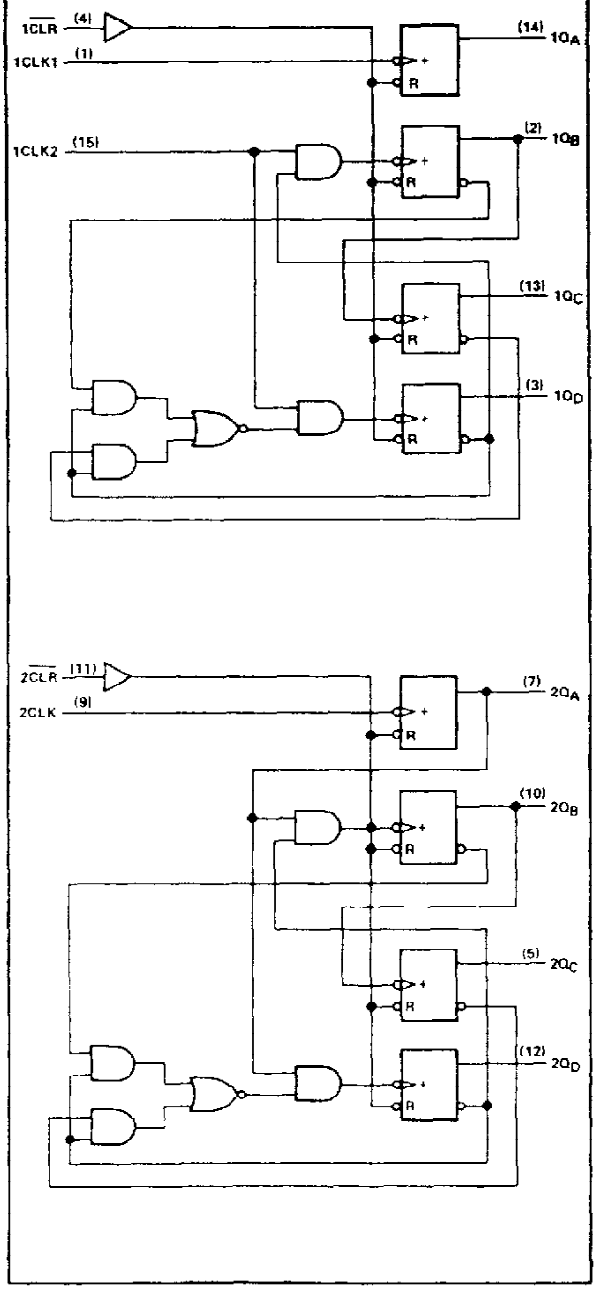


TYPICAL OF ALL OUTPUTS

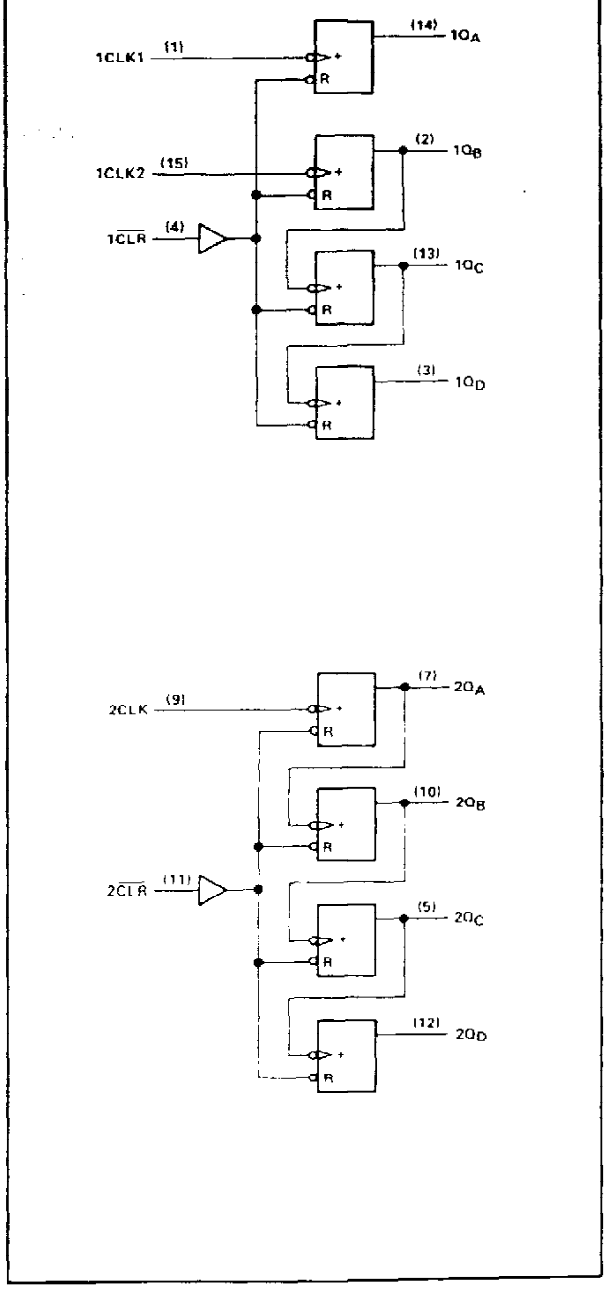


logic diagrams (positive logic)

'LS68



'LS69



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage: Clear inputs . . . . . 7 V
Clock inputs . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 4: Voltage values are with respect to network ground terminal.

recommended operating conditions

				SN54LS'			SN74LS'			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					−1			−1	mA
I_{OL}	Low-level output current					8			16	mA
f_{max}	Clock frequency	1CLK1		0		50	0		50	MHz
		1CLK2	'LS68	0		20	0		20	
			'LS69	0		25	0		25	
		2CLK	'LS68	0		40	0		40	
			'LS69	0		50	0		50	
t_w	Pulse width	1CLK1		10			10			ns
		1CLK2	'LS68	25			25			
			'LS69	20			20			
		2CLK	'LS68	13			13			
			'LS69	10			10			
		CLEAR		15			15			
t_{su}	Clear inactive-state set-up time			25			25			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_I	CLK	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
	$\overline{CLR}$	V_{CC} = MAX, V_I = 7 V				0.1			0.1	
I_{IH}	CLK	V_{CC} = MAX, V_I = 2.7 V				40			40	µA
	$\overline{CLR}$					20			20	
I_{IL}	1CLK1, 2CLK	V_{CC} = MAX, V_I = 0.4 V				−2			−2	mA
	1CLK2					−1.2			−1.2	
	$\overline{CLR}$					−0.2			−0.2	
I_{OS}§		V_{CC} = MAX, V_O = 0 V		−20		−100	−20		−100	mA
I_{CC}		V_{CC} = MAX, see Note 5			36	54		36	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 5: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS68			'LS69			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	1CLK1	$1Q_A$	R_L = 1 kΩ, C_L = 30 pF	50	70		50	70		MHz
f_{max}		$1Q_B$, $1Q_C$, $1Q_D$		20	30		25	35		MHz
f_{max}		$2Q_A$, $2Q_B$ $2Q_C$, $2Q_D$		40	60		50	70		MHz
t_{PLH}	1CLK1	$1Q_A$			7	11		7	11	ns
t_{PHL}					14	21		14	21	
t_{PLH}	1CLK2	$1Q_B$			8	12		7	11	ns
t_{PHL}					12	18		14	21	
t_{PLH}		$1Q_C$			15	23		16	24	
t_{PHL}					21	32		21	32	
t_{PLH}		$1Q_D$			8	12		25	38	
t_{PHL}					13	20		30	45	
t_{PLH}	2CLK	$2Q_A$			7	11		7	11	ns
t_{PHL}					14	21		14	21	
t_{PLH}		$2Q_B$			16	24		14	21	
t_{PHL}					19	29		19	29	
t_{PLH}		$2Q_C$			23	35		23	35	
t_{PHL}					27	40		27	40	
t_{PLH}		$2Q_D$			16	24		32	48	
t_{PHL}					19	29		36	54	
t_{PHL}	Any $\overline{CLR}$	Any Q			20	30		20	30	ns

NOTE 6: Load circuits and voltage waveforms are shown in Section 1.

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