SN54LS671, SN54LS672, SN74LS671, SN74LS672
4-BIT UNIVERSAL SHIFT REGISTERS/LATCHES WITH 3-STATE OUTPUTS

SDLS194 — D2638, JANUARY 1981 – REVISED MARCH 1988

- **4-Bit Universal Shift Registers/Latches**
- **Multiplexed Outputs for Shift Register or Latched Data**
- **Choice of Direct SR Clear ('LS671) or Synchronous SR Clear ('LS672)**
- **3-State Outputs Drive Bus Lines Directly**
- **Expandable to Any Word Length**

description

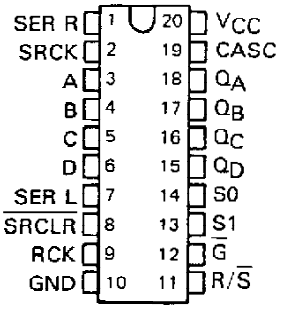
The 'LS671 and 'LS672 each contain a 4-bit universal shift register (similar to the 'LS194A) and a 4-bit storage register (similar to the 'LS175) multiplexed to a 3-state output stage (similar to the 'LS258). The user has the option of selecting the shift or storage register via the register/shift select input R/$\overline{S}$. The 'LS671 has a direct-overriding shift register clear while the 'LS672 features a synchronous shift register clear. The shift register has four distinct modes of operation, namely:

Inhibit clock (do nothing)
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Parallel (broadside) load

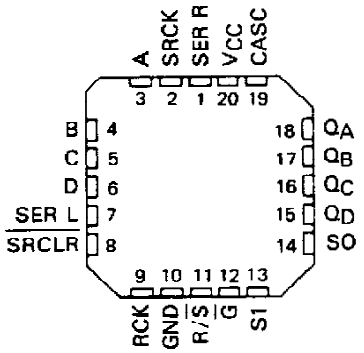
A cascade output for the shift register is provided so that full shift register functionality is provided even while the outputs are in the high-impedance mode. The cascade output presents Q_A data in the shift-left mode, Q_D data in the shift-right mode.

Both the shift register clock and the latch clock are triggered on the positive transition. The output control ($\overline{G}$) activates Q_A thru Q_D when low, it places Q_A thru Q_D into the high-impedance state when high.

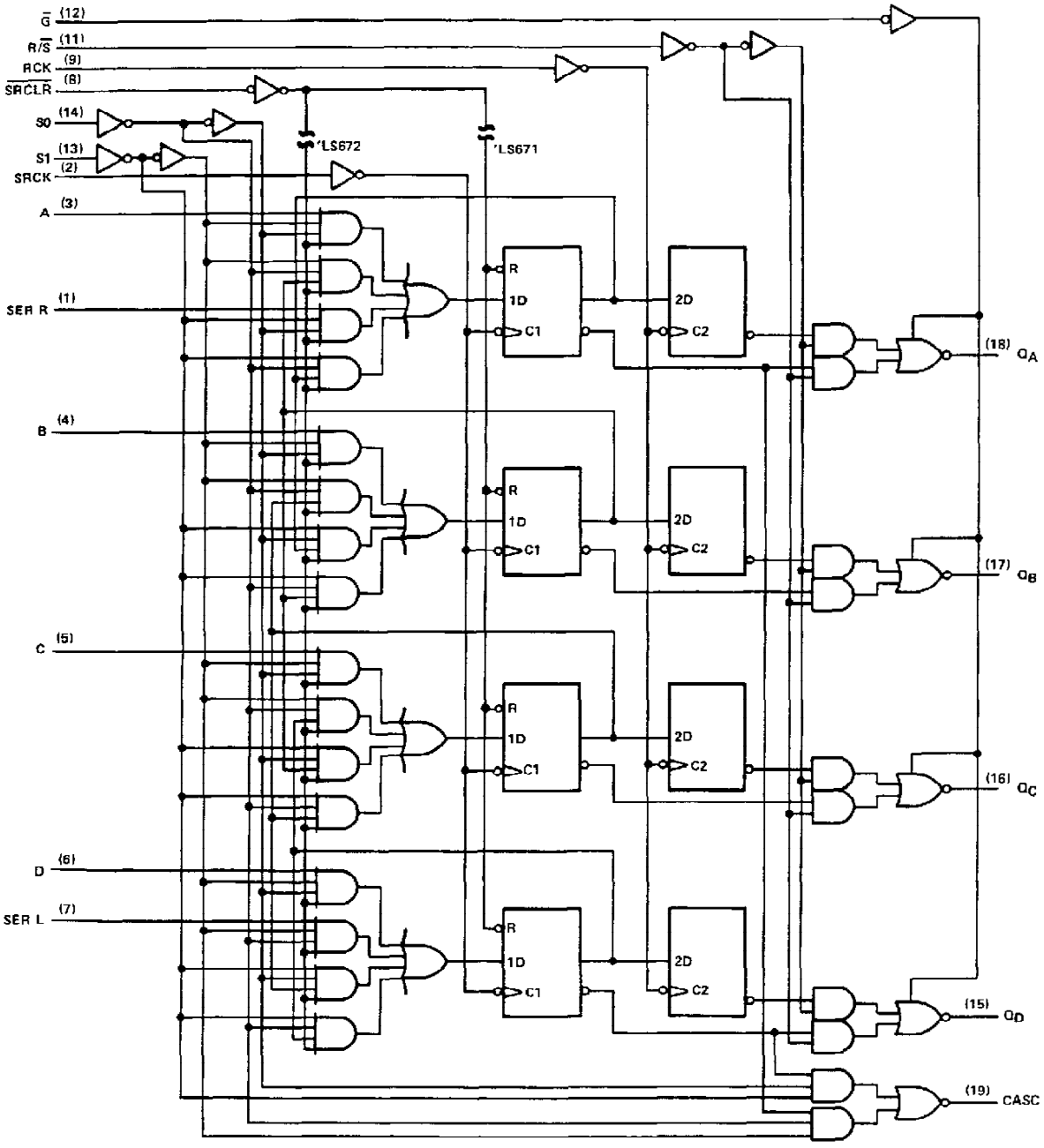
SN54LS671, SN54LS672 . . . J PACKAGE
SN74LS671, SN74LS672 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS671, SN54LS672 . . . FK PACKAGE
(TOP VIEW)

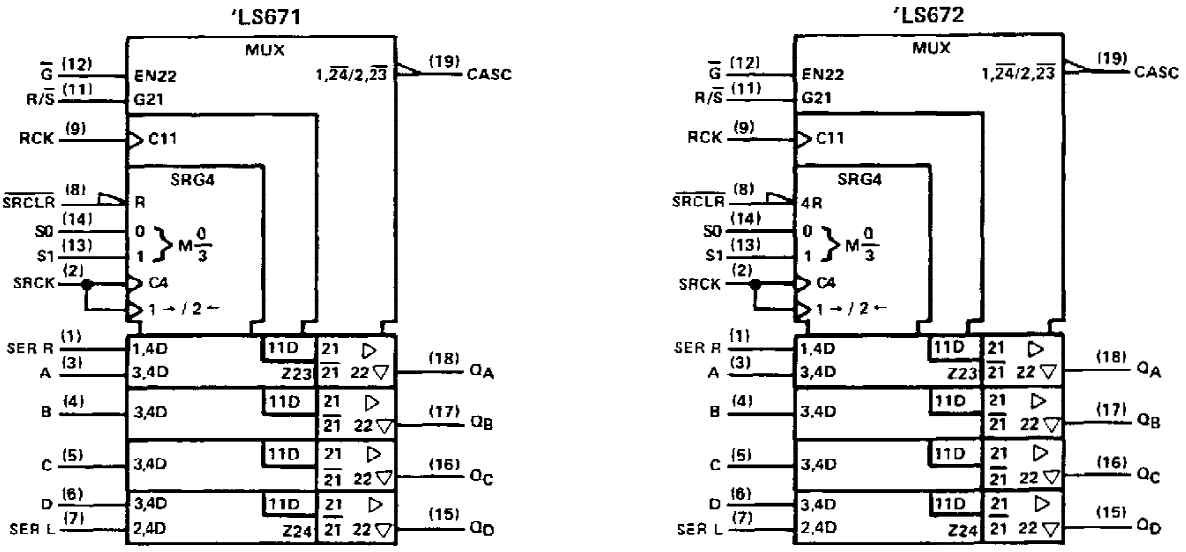


logic diagram (positive logic)



Pin numbers shown are for DW, J and N packages.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

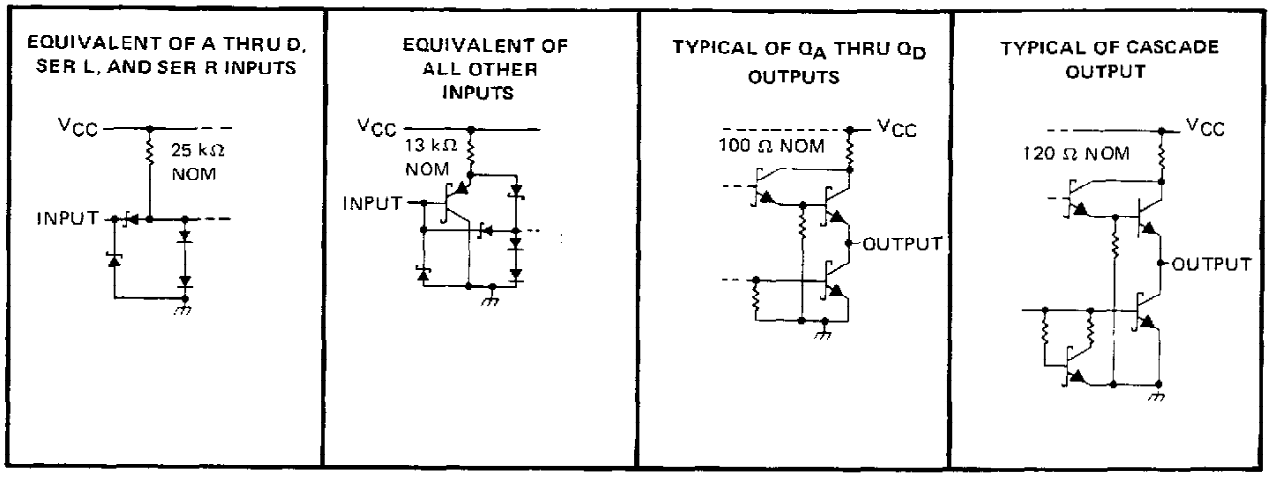
FUNCTION TABLE

			SR MODE		SRCK		SERIAL INPUTS		PARALLEL INPUTS				PARALLEL OUTPUTS				
$\overline{G}$	R/$\overline{S}$	$\overline{SRCLR}$	S1	S0	'LS671	'LS672	SL	SR	A	B	C	D	Q_A	Q_B	Q_C	Q_D	CASC‡
L	L	L	X	X	X	↑	X	X	X	X	X	X	L	L	L	L	(‡)
L	L	H	X	X	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	(‡)
L	L	H	L	L	X	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	H
L	L	H	L	H	↑	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
L	L	H	L	H	↑	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
L	L	H	H	L	↑	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Q_{Bn}
L	L	H	H	L	↑	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	Q_{Bn}
L	L	H	H	H	↑	↑	X	X	a	b	c	d	a	b	c	d	H
H	X	X	L	H	↑	↑	X	X	X	X	X	X	Z	Z	Z	Z	Q_{Cn}
H	X	X	H	L	↑	↑	X	X	X	X	X	X	Z	Z	Z	Z	Q_{Bn}
L	H	X	X	X	X	X	X	X	X	X	X	X	Internal register contents				(‡)

When the output control $\overline{G}$ is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the shift register and the output at CASC are not affected.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock
Z = high-impedance state
‡The cascade output displays the D bit of the shift register in mode 1 (S1, S0 = L, H), the A bit in mode 2 (S1, S0 = HL), and is inactive (H) in modes 0 and 3 (S1, S0 = LL and HH).

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS671, SN54LS672 . . . . . −55°C to 125°C
SN74LS671, SN74LS672 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	Cascade out			−0.4			−0.4	mA
		Q_A, Q_B, Q_C, Q_D			−1			−2.6	
I_{OL}	Low-level output current	Cascade out			4			8	mA
		Q_A, Q_B, Q_C, Q_D			12			24	
t_w	Width of SRCK, RCK, or $\overline{SRCLR}$ ('LS671 only) input pulse		30			30			ns
t_{su}	Inactive state setup time	$\overline{SRCLR}$ before SRCK ↑ ('LS671 only)	30			30			ns
t_{su}	Setup time	S0 or S1 to SRCK ↑	45			45			ns
		$\overline{SRCLR}$ ↓ ('LS672 only) to SRCK ↑	25			25			
		A, B, C, D to SRCK ↑	30			30			
		SRCK ↑ to RCK ↑	30			30			
		SER to SRCK ↑	35			35			
t_h	Hold time	Any input from SRCK ↑	0			0			ns
T_A	Operating free-air temperature		−65		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	$Q_A - Q_D$	V_{CC} = MIN,	I_{OH} = −1 mA	2.4	3.1					V
		$Q_A - Q_D$	V_{IH} = 2 V,	I_{OH} = −2.6 mA				2.4	3.1		
		CASC	V_{IL} = V_{IL} max	I_{OH} = −400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	$Q_A - Q_D$	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		$Q_A - Q_D$	V_{IH} = 2 V	I_{OL} = 24 mA					0.35	0.5	
		CASC		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		CASC		I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	$Q_A - Q_D$	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.7 V, V_{IL} = V_{IL} max			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	$Q_A - Q_D$	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 0.4 V, V_{IL} = V_{IL} max			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	A, B, C, D	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	$Q_A - Q_D$	V_{CC} = MAX,	V_O = 0 V	−30		−130	−30		−130	mA
		CASC			−20		−100	−20		−100	
I_{CC}	Supply current	All outputs low	V_{CC} = MAX,	See Note 2		35	70		35	70	mA
		All outputs high	All outputs	See Note 3		30	65		30	65	
		Q_A thru Q_D, at Hi-Z	open	See Note 4		37	70		37	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 2. I_{CCL} is tested after two 0-V to 4.5 V to 0-V pulses have been applied to SRCK and RCK while S0 is at 4.5 V and all other inputs are grounded.

3. I_{CCH} is tested after two 4.5-V to 0-V to 4.5 V pulses have been applied to SRCK and RCK while all other inputs are at 4.5 V.

4. I_{CCZ} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SRCK and RCK while S0 and $\overline{G}$ are at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS671			'LS672			UNIT
			MODE	LOAD	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SRCK ↑	CASCADE	SHIFT LEFT OR RIGHT	R_L = 2 kΩ, C_L = 15 pF		31	45		31	45	ns
t_{PHL}						14	25		14	25	
t_{PLH}	S0, S1					11	20		12	20	ns
t_{PHL}						11	20		12	20	
t_{PHL}	SRCK ↑		SR CLEAR						19	30	ns
t_{PHL}	$\overline{SRCLR}$ ↓					19	30				ns
t_{PLH}	SRCK ↑	$Q_A - Q_D$	SHIFT LEFT OR RIGHT	R_L = 667 Ω, C_L = 45 pF		10	20		10	20	ns
t_{PHL}						16	25		16	25	
t_{PLH}			SR LOAD			10	20		10	20	ns
t_{PHL}						15	25		15	25	
t_{PHL}			SR CLEAR						17	30	ns
t_{PHL}	$\overline{SRCLR}$ ↓					21	30				ns
t_{PLH}	RCK ↑		LATCH			10	20		10	20	ns
t_{PHL}						15	25		15	25	
t_{PLH}	R/$\overline{S}$ ↑		MUX			12	25		13	25	ns
t_{PHL}						15	25		15	25	
t_{PLH}	R/$\overline{S}$ ↓					17	25		17	25	ns
t_{PHL}						16	25		16	25	
t_{PZH}	$\overline{G}$ ↓		3-STATE ENABLE			16	25		16	25	ns
t_{PZL}						19	30		19	30	
t_{PHZ}	$\overline{G}$ ↑		3-STATE DISABLE	R_L = 667 Ω, C_L = 5 pF		16	25		16	25	ns
t_{PLZ}						16	25		16	25	

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

The 'LS671 or 'LS672 can easily be expanded utilizing the cascade output and the SER L and SER R inputs. A typical expansion is shown below.

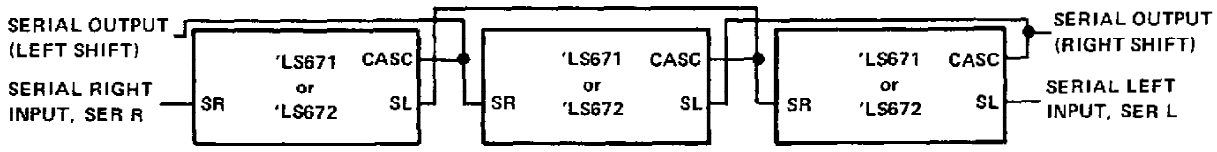


FIGURE 1 – 'LS671, 'LS672 EXPANDED TO 12 BITS, (3 PACKAGES)

Any desired word length may be obtained using the scheme shown. Corresponding control pins of all the packages are tied in common, i.e., all S0 pins are connected together, all S1 pins are connected together, etc.

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