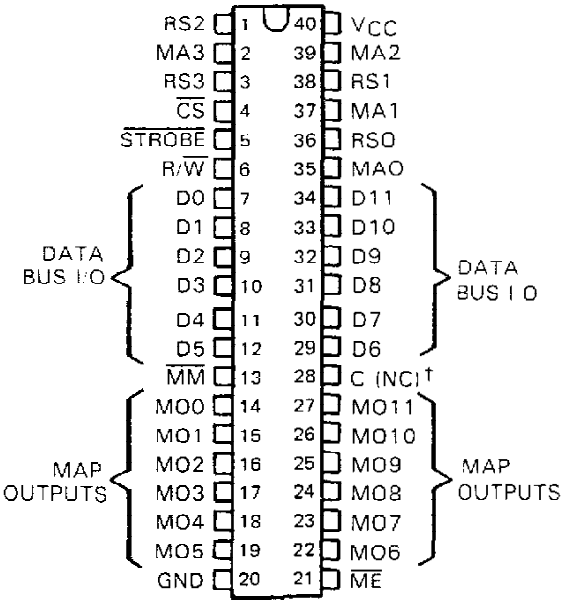
SDLS184 D2549, JANUARY 1981—REVISED APRIL 1990

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610
- 3-State Map Outputs
- Compatible with TMS9900 and Other Microprocessors

JD OR N PACKAGE
(TOP VIEW)



†This pin has no internal connection on the 'LS612.

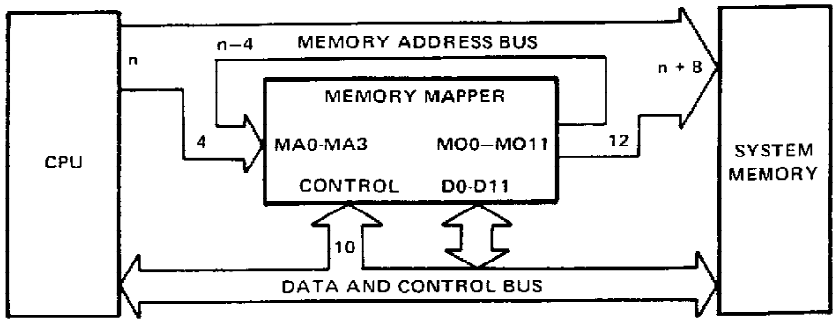
description

Each 'LS610 and 'LS612 memory-mapper integrated circuit contains a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. Each 'LS610 also contains 12 latches with an enable control.

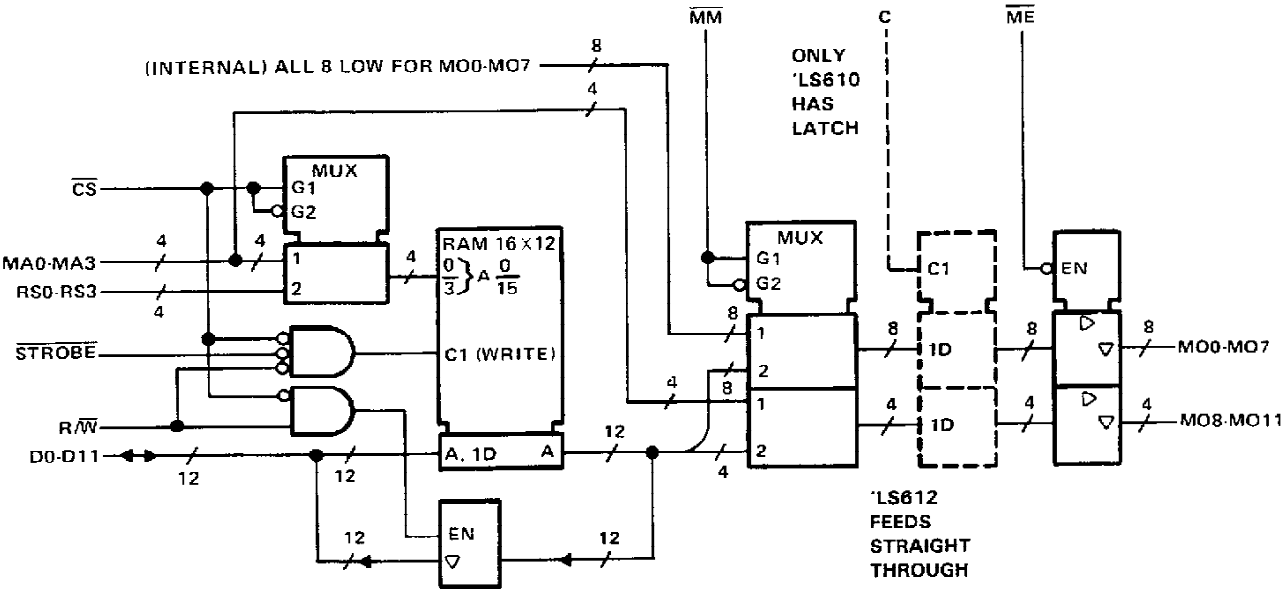
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see System Block Diagram) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus. This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation: read, write, map, and pass. Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 output stages are transparent in this mode, while the 'LS610 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at M08-M011, respectively, (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.

system block diagram



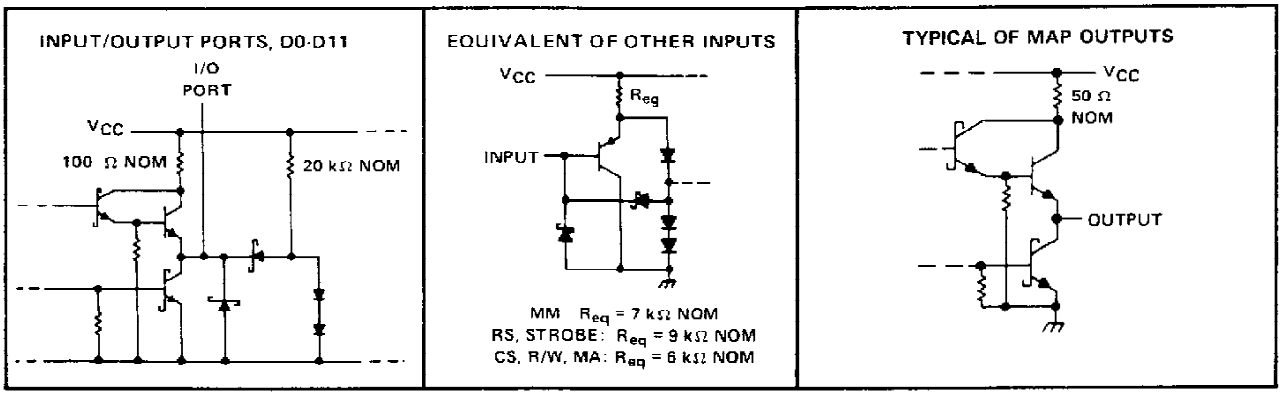
logic diagram (positive logic)



TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
C	28	Latch enable input for the 'LS610 (no internal connection for 'LS612). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
$\overline{CS}$	4	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
D0 thru D11	7-12 29-34	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
MA0 thru MA3	35, 37, 39, 2	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high).
$\overline{ME}$	21	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
$\overline{MM}$	13	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
MO0 thru MO11	14-19, 22-27	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
RS0 thru RS3	36, 38, 1, 3	Register select inputs for I/O operations.
R/$\overline{W}$	6	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
$\overline{STROBE}$	5	Strobe input used to enter data into the selected map register during I/O operations.
V_{CC}, GND	40, 20	5-V power supply and network ground (substrate) pins

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: Data Bus I/O . . . . . 5.5 V
All other inputs . . . . . 7 V
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{OH}	High-level output current		MO			−15	mA
			D			−2.6	
I_{OL}	Low-level output current		MO			24	mA
			D			8	
t_{AVCL}	Address setup time (AV before C low)	'LS610 only	See Figure 2	30			ns
t_{SLSH}	Duration of strobe input pulse		See Figure 1	75			ns
t_{CSLSL}	$\overline{CS}$ setup time ($\overline{CS}$ low to strobe low)			20			ns
t_{WLSL}	R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low)			20			ns
t_{RVSL}	RS setup time (RS valid to strobe low)			20			ns
t_{DVSH}	Data setup time (D0-D11 valid to strobe high)			75			ns
t_{SHCSH}	$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high)			20			ns
t_{SHWH}	R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high)			20			ns
t_{SHRX}	RS hold time (Strobe high to RS invalid)			20			ns
t_{SHDX}	Data hold time (Strobe high to D0-D11 invalid)			20			ns
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5	V
V_{OH}	MO	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OH} = −3 mA	2.4			V
				I_{OH} = MAX	2			
	D			I_{OH} = MAX	2.4			
V_{OL}	MO	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4	V
				I_{OL} = 24 mA		0.35	0.5	
	D			I_{OL} = 4 mA		0.25	0.4	
				I_{OL} = 8 mA		0.35	0.5	
I_{OZH}		V_{CC} = MAX, V_{IL} = MAX,	V_{IH} = 2 V, V_O = 2.7 V				20	μA
I_{OZL}	MO	V_{CC} = MAX, V_{IL} = MAX,	V_{IH} = 2 V, V_O = 0.4 V				−20	μA
	D						−400	
I_I	D	V_{CC} = MAX		V_I = 5.5 V			0.1	mA
	All others			V_I = 7 V			0.1	
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V				−0.4	mA
I_{OS}§	MO	V_{CC} = MAX			−40		−225	mA
	D				−30		−130	
I_{CC}		V_{CC} = MAX	Outputs high			112	180	mA
			Outputs low			112	180	
			Outputs disabled			180	230	

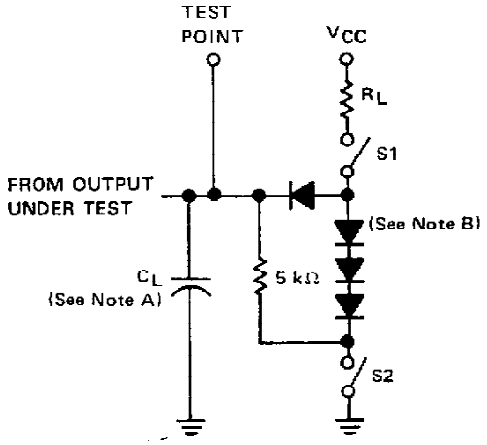
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV}	Access (enable) time	$\overline{CS}$↓	D0-11	R_L = 2 kΩ, See Figure 1, See Notes 2 and 3		28	50		26	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}$↑	D0-11			20	35		20	35	ns
t_{RVDV}	Access time	RS	D0-11			49	75		39	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}$↓	D0-11			32	50		30	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}$↑	D0-11			42	65		38	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}$↓	MO0-11	R_L = 667 Ω, See Figure 2, See Notes 2 and 3		19	30		17	30	ns
t_{CSHQV}	Access time	$\overline{CS}$↑	MO0-11			56	85		48	85	ns
t_{MLQV}	Access time	$\overline{MM}$↓	MO0-11			25	40		22	40	ns
t_{CHQV}	Access time	C↑	MO0-11			24	40				ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO0-11			46	70		39	70	ns
t_{MHQV}	Access time	$\overline{MM}$↑	MO0-11			24	40		22	40	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO8-11			19	30		13	30	ns
t_{EHQZ}	Disable time	$\overline{ME}$↑	MO0-11			14	25		14	25	ns

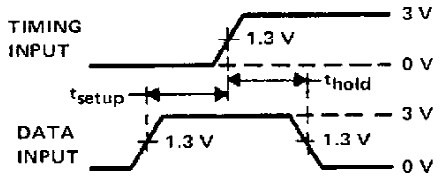
NOTES: 2. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.
3. Load circuits and voltage waveforms are shown in Parameter Measurement Information.

PARAMETER MEASUREMENT INFORMATION

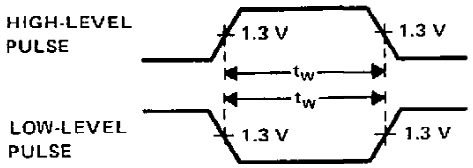


LOAD CIRCUIT FOR
3-STATE OUTPUTS

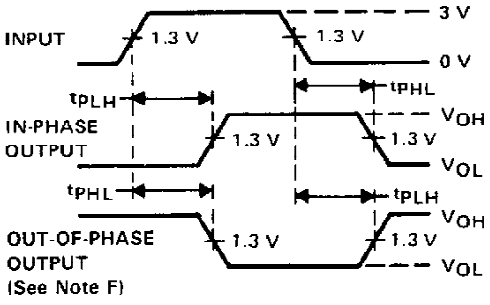
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.



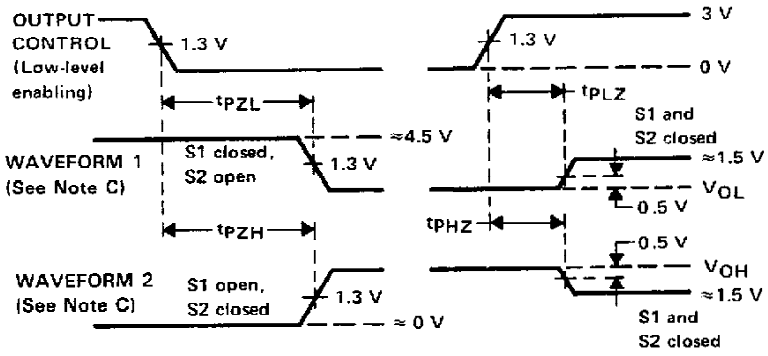
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 15 ns, t_f ≤ 6 ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.
G. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION

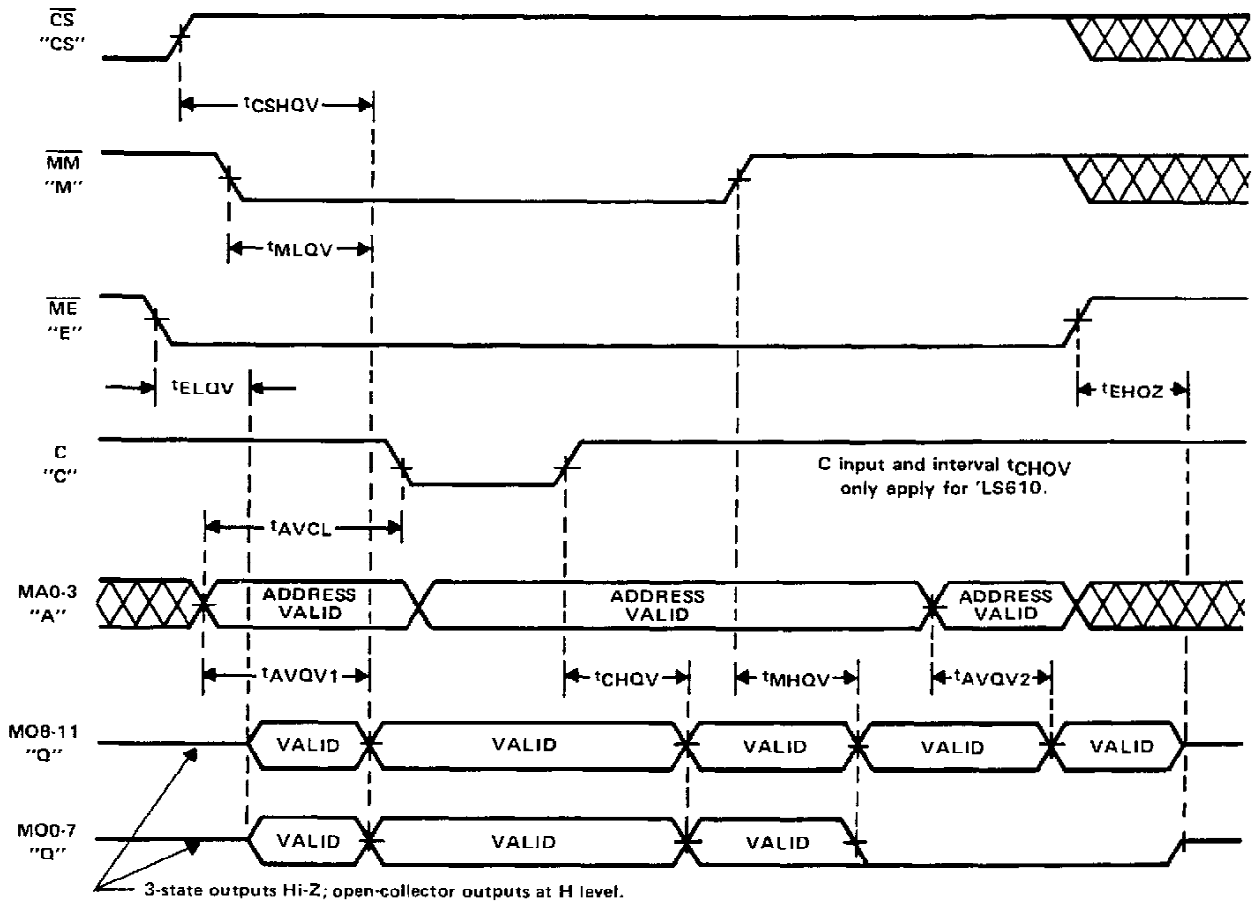


FIGURE 2. MAP AND PASS MODES

PARAMETER MEASUREMENT INFORMATION

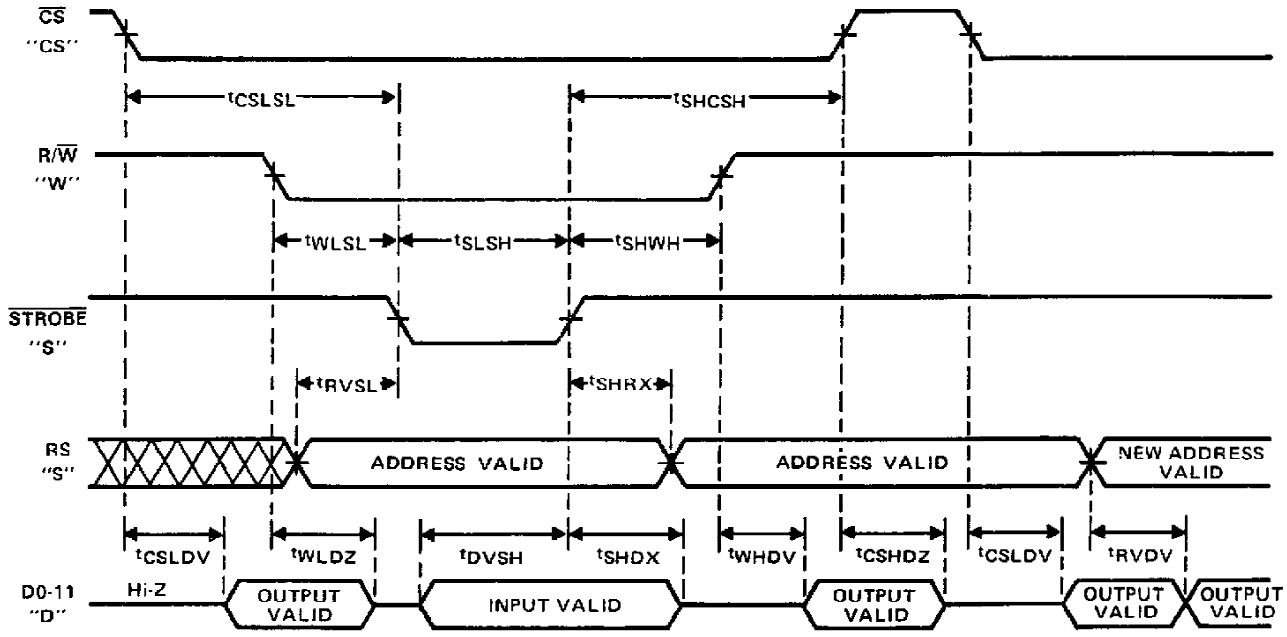


FIGURE 3. WRITE AND READ MODES

EXPLANATION OF LETTER SYMBOLS

This data sheet uses a new type of letter symbol based on JEDEC Standard 100 to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C SUBSCRIPT	SIGNAL NAME	A AND C SUBSCRIPT
C	C	$\overline{ME}$	E
$\overline{CS}$	CS	$\overline{MM}$	M
D0—11	D	R/$\overline{W}$	W
MA0—MA3	A	RS0—RS3	R
MO0—MO11	Q	$\overline{STROBE}$	S

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