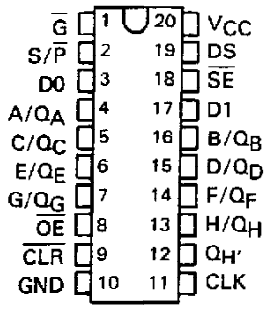
# SN54LS322A, SN74LS322A
# 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

SDLS159

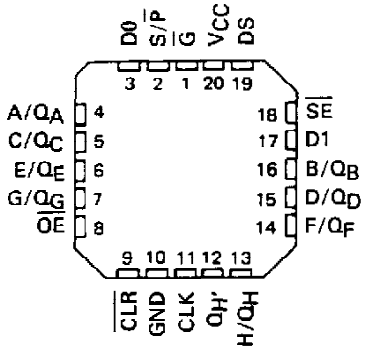
D2411, OCTOBER 1977 – REVISED MARCH 1988

- **Multiplexed Inputs/Outputs Provide Improved Bit Density**
- **3-State Outputs Drive Bus Lines Directly**
- **Sign Extend Function**
- **Direct Overriding Clear**

**SN54LS322A . . . J OR W PACKAGE**
**SN74LS322A . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54LS322A . . . FK PACKAGE**
**(TOP VIEW)**




## description

These low-power Schottky eight-bit shift registers feature multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output ($Q_{H'}$) is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the S/$\overline{P}$ inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the $Q_A$ flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

**FUNCTION TABLE**

| OPERATION | INPUTS | | | | | | | INPUTS/OUTPUTS | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | REGISTER ENABLE $\overline{G}$ | S/$\overline{P}$ | SIGN EXTEND $\overline{SE}$ | DATA SELECT DS | OUTPUT ENABLE $\overline{OE}$ | CLK | A/$Q_A$ | B/$Q_B$ | C/$Q_C$ . . . H/$Q_H$ | | $Q_{H'}$ |
| Clear | L | H | X | X | X | L | X | L | L | L | L | L |
| | L | X | H | X | X | L | X | L | L | L | L | L |
| Hold | H | H | X | X | X | L | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{H0}$ | $Q_{H0}$ |
| Shift Right | H | L | H | H | L | L | ↑ | D0 | $Q_{An}$ | $Q_{Bn}$ | $Q_{Gn}$ | $Q_{Gn}$ |
| | H | L | H | H | H | L | ↑ | D1 | $Q_{An}$ | $Q_{Bn}$ | $Q_{Gn}$ | $Q_{Gn}$ |
| Sign Extend | H | L | H | L | X | L | ↑ | $Q_{An}$ | $Q_{An}$ | $Q_{Bn}$ | $Q_{Gn}$ | $Q_{Gn}$ |
| Load | H | L | L | X | X | X | ↑ | a | b | c | h | h |

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/$\overline{P}$ input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$Q_{A0}$ . . . $Q_{H0}$ = the level of $Q_A$ through $Q_H$, respectively, before the indicated steady-state conditions were established
$Q_{An}$ . . . $Q_{Hn}$ = the level of $Q_A$ through $Q_H$, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a . . . h = the level of steady-state inputs at inputs A through H respectively



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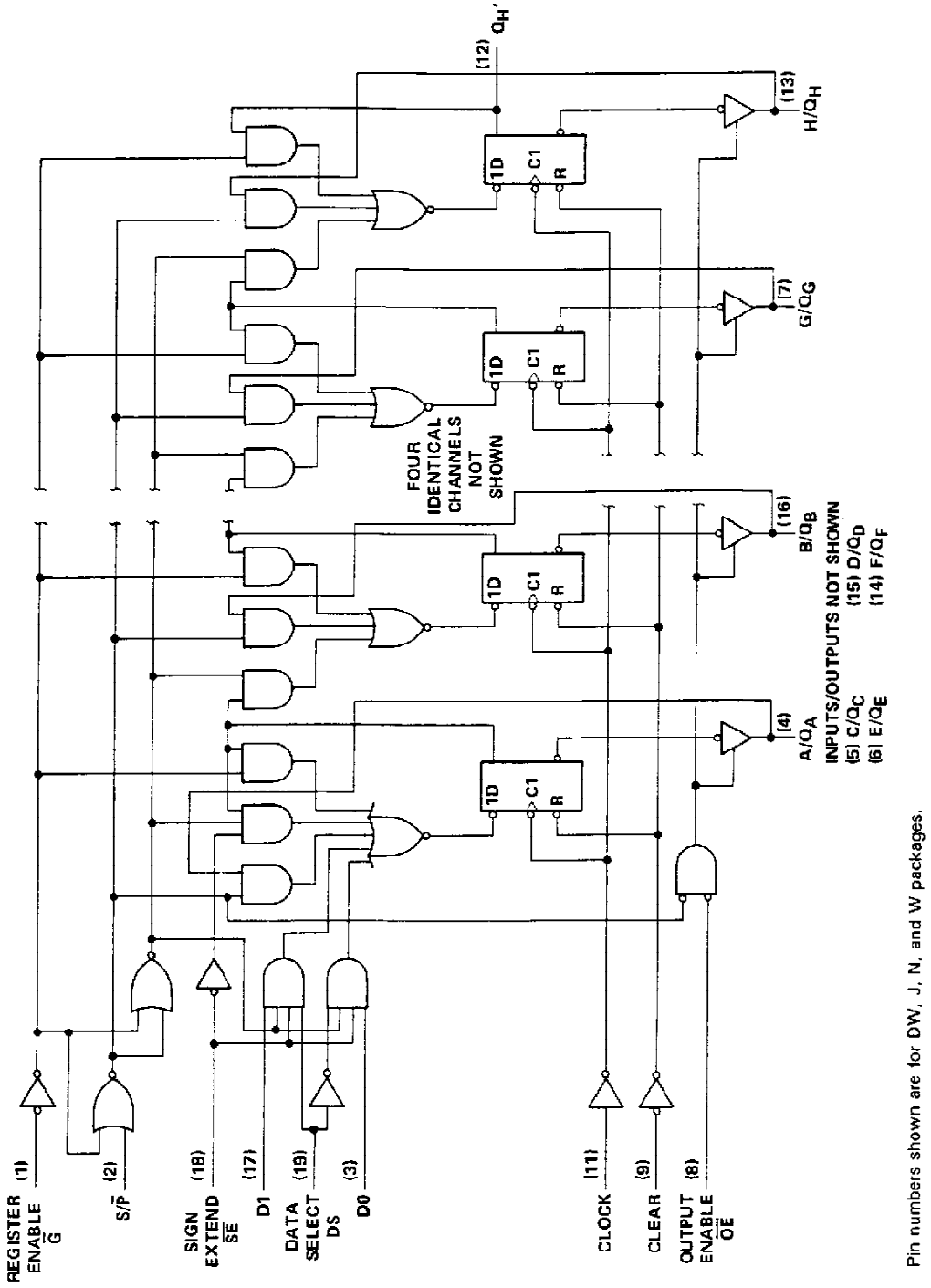
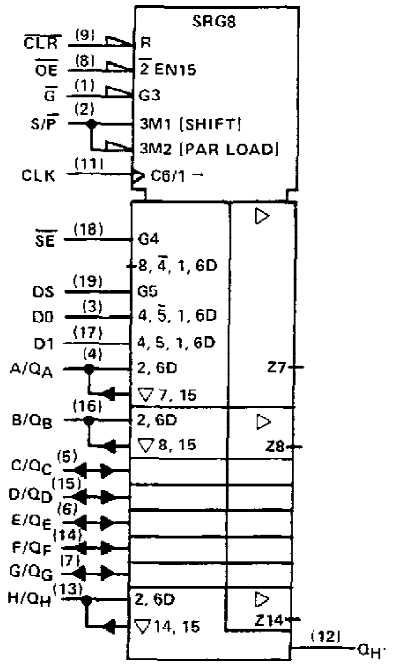
logic diagram (positive logic)



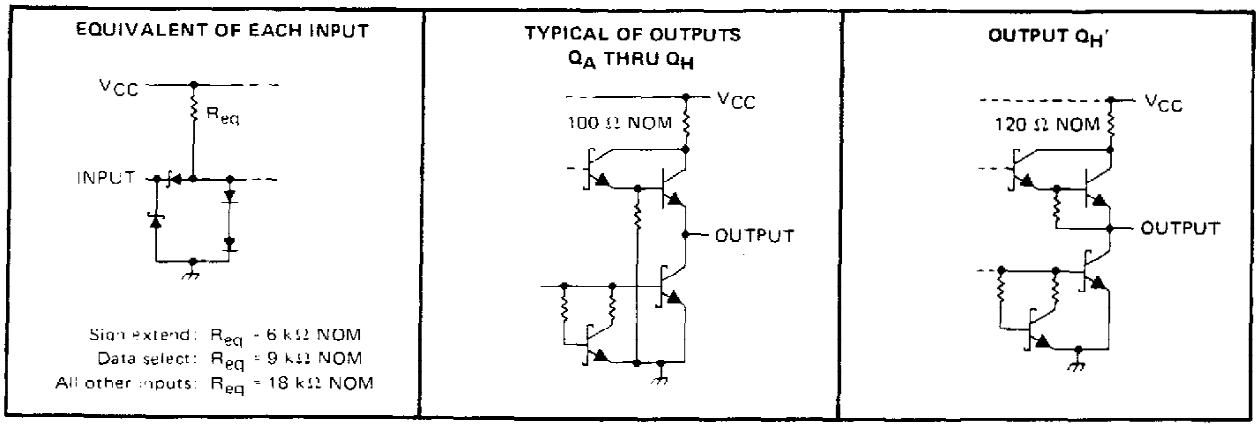

Pin numbers shown are for DW, J, N, and W packages.

## logic symbol†




†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54LS322A . . . . . −55°C to 125°C
SN74LS322A . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN54LS322A | | | SN74LS322A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.5 | V |
| $I_{OH}$ | High-level output current | $Q_A$ thru $Q_H$ | | | −1 | | | −2.6 | mA |
| | | $Q_H'$ | | | −0.4 | | | −0.4 | |
| $I_{OL}$ | Low-level output current | $Q_A$ thru $Q_H$ | | | 12 | | | 24 | mA |
| | | $Q_H'$ | | | 4 | | | 8 | |
| $f_{clock}$ | Clock frequency | | 0 | | 20 | 0 | | 20 | MHz |
| $t_{w(clock)}$ | Width of clock pulse | Clock high | 30 | | | 30 | | | ns |
| | | Clock low | 10 | | | 10 | | | |
| $t_{w(clear)}$ | | Clear low | 20 | | | 20 | | | ns |
| $t_{su}$ | Setup time | Data select | 10↑ | | | 10↑ | | | ns |
| | | High-level data† | 20↑ | | | 20↑ | | | |
| | | Low-level data† | 20↑ | | | 20↑ | | | |
| | | Clear inactive-state | 20↑ | | | 20↑ | | | |
| | | Register enable $\overline{G}$ high | 35↑ | | | 35↑ | | | |
| | | Register enable $\overline{G}$ low | 50↑ | | | 50↑ | | | |
| $t_h$ | Hold time | Data select | 10↑ | | | 10↑ | | | ns |
| | | Data† | 2↑ | | | 2↑ | | | |
| | | Register enable high or low | 0↑ | | | 0↑ | | | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

†Data includes the two serial inputs and the eight input/output data lines.
↑The arrow indicates that the rising edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS322A | | | SN74LS322A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | $Q_A$ thru $Q_H$ | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX, $I_{OH}$ = MAX | | | 2.4 | 3.2 | | 2.4 | 3.1 | | V |
| | $Q_H'$ | | | | 2.5 | 3.4 | | 2.7 | 3.4 | | |
| $V_{OL}$ | $Q_A$ thru $Q_H$ | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OL}$ = 12 mA | | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.35 | 0.5 | |
| | $Q_H'$ | | $I_{OL}$ = 4 mA | | | 0.25 | 0.4 | | 0.25 | 0.4 | |
| | | | $I_{OL}$ = 8 mA | | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $Q_A$ thru $Q_H$ | $V_{CC}$ = MAX, $V_{IH}$ = 2 V, | $V_O$ = 2.7 V | | | | 40 | | | 40 | μA |
| $I_{OZL}$ | $Q_A$ thru $Q_H$ | $V_{CC}$ = MAX, $V_{IH}$ = 2 V, | $V_O$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_I$ | A thru H | $V_{CC}$ = MAX | $V_I$ = 5.5 V | | | | 0.1 | | | 0.1 | mA |
| | Data select | | $V_I$ = 7 V | | | | 0.2 | | | 0.2 | |
| | Sign extend | | $V_I$ = 7 V | | | | 0.3 | | | 0.3 | |
| | Any other | | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | A thru H, DS | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | | 40 | | | 40 | μA |
| | Sign extend | | | | | | 60 | | | 60 | |
| | Any other | | | | | | 20 | | | 20 | |
| $I_{IL}$ | Data select | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | | −0.8 | | | −0.8 | mA |
| | Sign extend | | | | | | −1.2 | | | −1.2 | |
| | Any other | | | | | | −0.4 | | | −0.4 | |
| $I_{OS}$§ | $Q_A$ thru $Q_H$ | $V_{CC}$ = MAX, $V_O$ = 2.25 V (for 54LS only) | | | −15 | | −65 | −30 | | −130 | mA |
| | $Q_H'$ | | | | −10 | | −50 | −20 | | −100 | |
| $I_{CC}$ | | $V_{CC}$ = MAX | | | | 35 | 60 | | 35 | 60 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | See Note 2 | | 20 | 35 | | MHz |
| $t_{PLH}$ | CLK | $Q_H'$ | $R_L$ = 2 kΩ, See Note 2 | $C_L$ = 15 pF, | | 22 | 33 | ns |
| $t_{PHL}$ | | | | | | 26 | 35 | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H'$ | | | | 27 | 35 | ns |
| $t_{PLH}$ | CLK | $Q_A$ thru $Q_H$ | $R_L$ = 665 Ω, See Note 2 | $C_L$ = 45 pF, | | 16 | 25 | ns |
| $t_{PHL}$ | | | | | | 22 | 33 | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_A$ thru $Q_H$ | | | | 22 | 35 | ns |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$ thru $Q_H$ | | | | 15 | 35 | ns |
| $t_{PZL}$ | | | | | | 15 | 35 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$ thru $Q_H$ | $R_L$ = 665 Ω, See Note 2 | $C_L$ = 5 pF, | | 15 | 25 | ns |
| $t_{PLZ}$ | | | | | | 15 | 25 | |

¶ $f_{max}$ ≡ maximum clock frequency
$t_{PLH}$ ≡ propagation delay time, low-to-high-level output
$t_{PHL}$ ≡ propagation delay time, high-to-low-level output
$t_{PZH}$ ≡ output enable time to high level
$t_{PZL}$ ≡ output enable time to low level
$t_{PHZ}$ ≡ output disable time from high level
$t_{PLZ}$ ≡ output disable time from low level

NOTE 2: For testing $f_{max}$, all outputs are loaded simultaneously, each with $C_L$ and $R_L$ as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.

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