

SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156

MARCH 1974 — REVISED MARCH 1988

- Multiplexed Inputs/Outputs Provide Improved Bit Density

- Four Modes of Operations:

Hold (Store) Shift Left
Shift Right Load Data

- Operates with Outputs Enabled or at High Z

- 3-State Outputs Drive Bus Lines Directly

- Can Be Cascaded for N-Bit Word Lengths

- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear

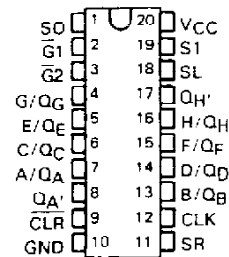
- Applications:

Stacked or Push-Down Registers
Buffer Storage, and Accumulator
Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

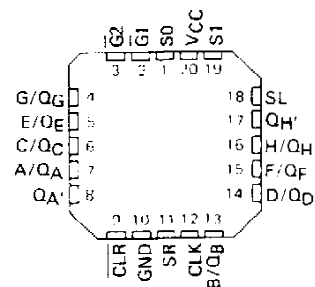
SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS299, SN54S299 . . . FK PACKAGE

(TOP VIEW)



description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS								OUTPUTS			
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	S0	G1'	G2'		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	*	X	H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QA _n
	H	L	H	L	L	*	X	L	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QA _n
Shift Left	H	H	L	L	L	*	H	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	H	QB _n	H
	H	H	L	L	L	*	L	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	L	QB _n	L
Load	H	H	H	X	X	*	X	X	a	b	c	d	e	f	g	h	a	h

* When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.

*When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip flop outputs are isolated from the input/output terminals.

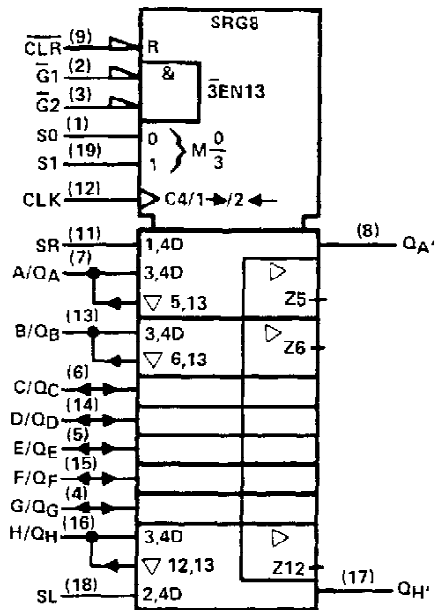
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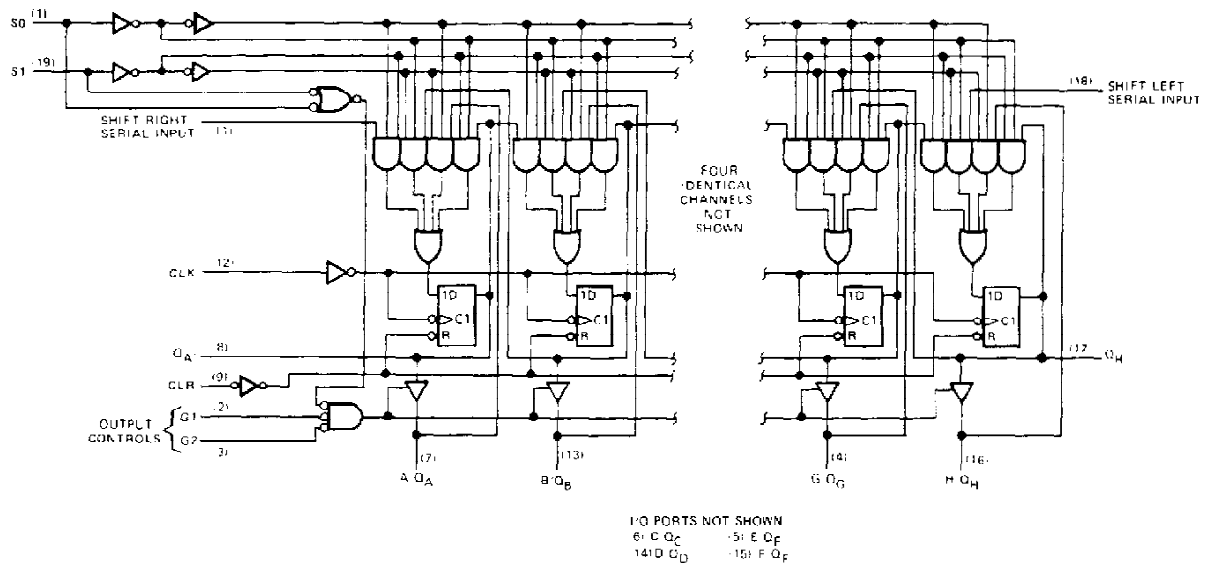
SN54LS299, SN54S299, SN74LS299, SN74S299 **8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

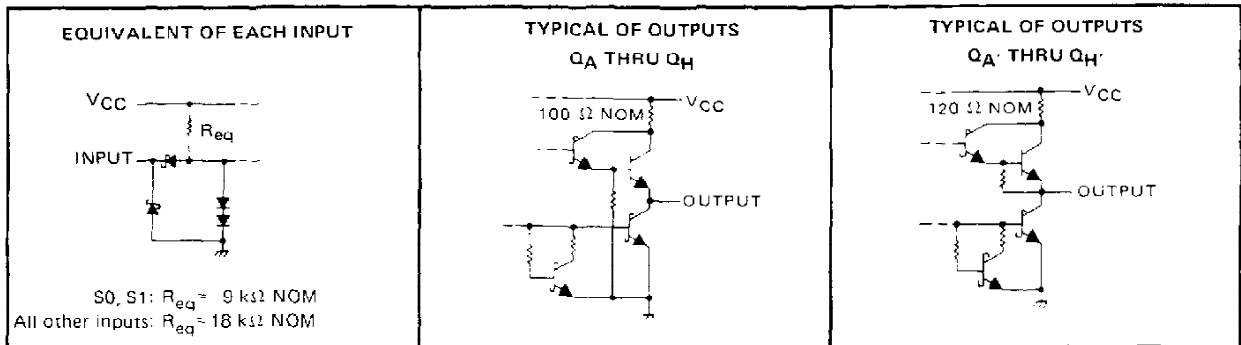
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SN54LS299, SN74LS299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS299	-55°C to 125°C
SN74LS299	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			-1			-2.6	mA
	Q_A' or Q_H'			-0.4			-0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	Q_A' or Q_H'			4			8	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_w(clock)$	Clock high	30			30			ns
	Clock low	18			10			
Width of clear pulse, $t_w(clear)$	Clear low	25			20			ns
	Clear high							
Setup time, t_{SU}	Select	35†			35†			ns
	High-level data†	20†			20†			
	Low-level data†	20†			20†			
	Clear inactive-state	24†			20†			
Hold time, t_H	Select	10†			10†			ns
	Data†	3†			0†			
Operating free-air temperature, T_A		-55		125	0		70	°C

† Data includes the two serial inputs and the eight input/output data lines.

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8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS299			SN74LS299			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	Q _A thru Q _H	2.4	3.2		2.4	3.1		V
		Q _A ' or Q _H '	2.5	3.4		2.7	3.4		
V _{OL}	Low-level output voltage	Q _A thru Q _H			I _{OL} = 12 mA	0.25	0.4		V
					I _{OL} = 24 mA			0.35 0.5	
		Q _A ' or Q _H '			I _{OL} = 4 mA	0.25	0.4		
					I _{OL} = 8 mA			0.35 0.5	
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H			V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V		40		μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H			V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V		-400		μA
I _I	Input current at maximum input voltage	S0, S1			V _{CC} = MAX, V _I = 7 V		200		μA
		A thru H			V _{CC} = MAX, V _I = 5.5 V		100		
		Any other			V _{CC} = MAX, V _I = 7 V		100		
I _{IH}	High-level input current	A thru H, S0, S1			V _{CC} = MAX, V _I = 2.7 V		40		μA
		Any other			V _{CC} = MAX, V _I = 2.7 V		20		
I _{IL}	Low-level input current	S0, S1			V _{CC} = MAX, V _I = 0.4 V		-0.8		mA
		Any other			V _{CC} = MAX, V _I = 0.4 V		-0.4		
I _{OS}	Short-circuit output current [§]	Q _A thru Q _H	-30	-130		-30	-130		mA
		Q _A ' or Q _H '	-20	-100		-20	-100		
I _{CC}	Supply current	V _{CC} = MAX	33	53		33	53		mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER [¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	20	35		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 2 kΩ, C _L = 15 pF		22	33	ns
t _{PHL}					26	39	
t _{PHL}					27	40	
t _{PLH}	CLK	Q _A thru Q _H	R _L = 665 Ω, C _L = 45 pF		17	25	ns
t _{PHL}					26	39	
t _{PHL}					26	40	
t _{PZH}	$\overline{G1}, \overline{G2}$	Q _A thru Q _H	R _L = 665 Ω, C _L = 5 pF		13	21	ns
t _{PZL}					19	30	
t _{PHZ}					10	20	
t _{PLZ}	$\overline{G1}, \overline{G2}$	Q _A thru Q _H			10	15	ns

[¶] f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

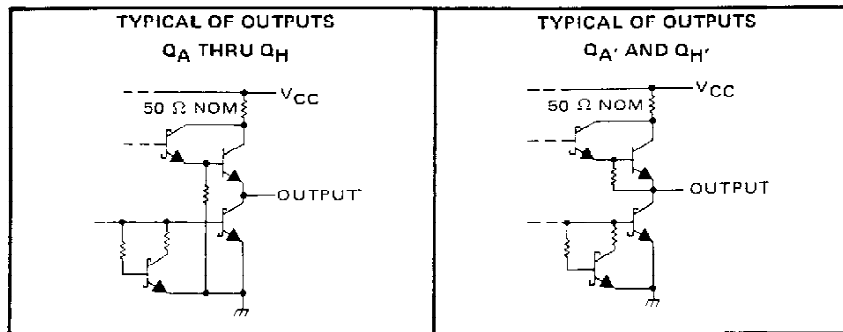
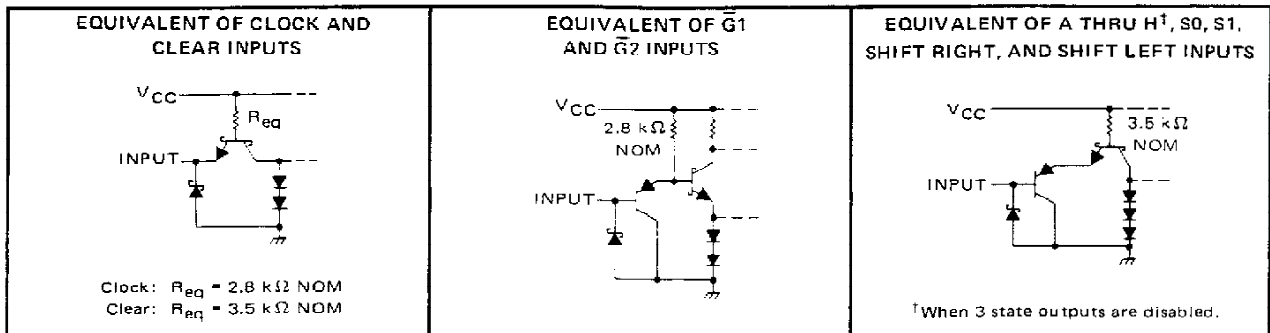
Load circuits and voltage waveforms are shown in Section 1.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S299 (See Note 1)	-55°C to 125°C
SN74S299	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			-2			-6.5	mA
	Q_A' or Q_H'			-0.5			-0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	Q_A' or Q_H'			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, t_{su}	Select	15†			15†			ns
	High-level data†	7†			7†			
	Low-level data†	5†			5†			
	Clear inactive-state	10†			10†			
Hold time, t_h	Select	5†			5†			ns
	Data†	5†			5†			
Operating free-air temperature, T_A		-55		125	0		70	C

† Data includes the two serial inputs and the eight input/output data lines.

SN54S299, SN74S299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2	V
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	2.4	3.2	V
		Q _A ' or Q _H '		2.7	3.4	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX			0.5	V
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V		100	μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V		250	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	High-level input current	A thru H, S0, S1	V _{CC} = MAX, V _I = 2.7 V		100	μA
		Any other			50	
I _{IL}	Low-level input current	CLK or CLR			-2	mA
		S0, S1	V _{CC} = MAX, V _I = 0.5 V		-500	μA
		Any other			-250	μA
					-250	μA
I _{OS}	Short-circuit output current §	Q _A thru Q _H	V _{CC} = MAX		-40	mA
		Q _A ' or Q _H '			-20	
I _{CC}	Supply current	V _{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	50	70		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 1 kΩ, C _L = 15 pF		12	20	ns
t _{PHL}		Q _A ' or Q _H '			13	20	
t _{PHL}	CLR	Q _A ' or Q _H '			14	21	ns
t _{PLH}	CLK	Q _A thru Q _H	R _L = 280 Ω, C _L = 45 pF		15	21	ns
t _{PHL}		Q _A thru Q _H			15	21	
t _{PHL}	CLR	Q _A thru Q _H			16	24	ns
t _{PZH}	G1, G2	Q _A thru Q _H	R _L = 280 Ω, C _L = 5 pF		10	18	ns
t _{PZL}		Q _A thru Q _H			12	18	
t _{PHZ}	G1, G2	Q _A thru Q _H			7	12	ns
t _{PLZ}		Q _A thru Q _H			7	12	

† f_{max} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.

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