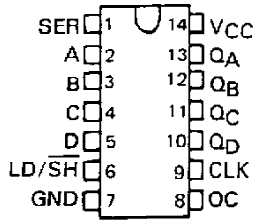
SDLS154

SN54LS295B, SN74LS295B
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

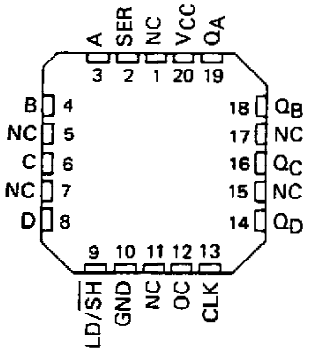
OCTOBER 1976 – REVISED MARCH 1988

- **'LS295B Offers Three Times the Sink-Current Capability of 'LS295A**
- **Schottky-Diode-Clamped Transistors**
- **Low Power Dissipation . . . 80 mW Typical (Enabled)**
- **Applications:**
  - **N-Bit Serial-To-Parallel Converter**
  - **N-Bit Parallel-To-Serial Converter**
  - **N-Bit Storage Register**

SN54LS295B . . . J OR W PACKAGE
SN74LS295B . . . D OR N PACKAGE
(TOP VIEW)



SN54LS295B . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock (CLK), serial (SER), mode (LD/$\overline{SH}$), and outputs control (OC) inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

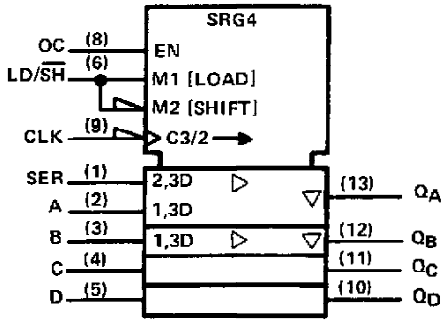
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

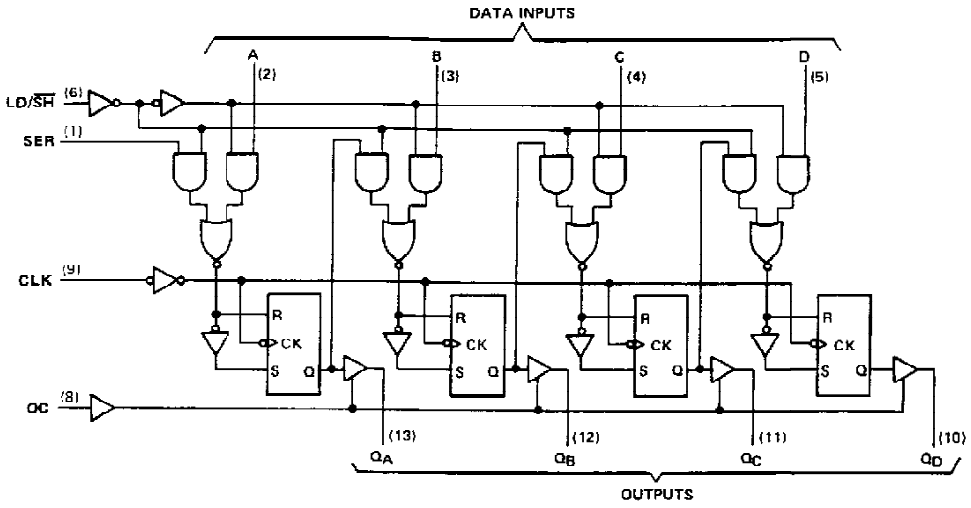
The SN54LS295B is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS295B is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

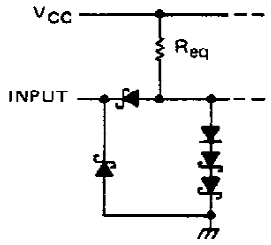
logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

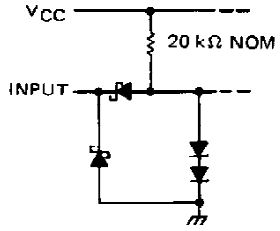
schematics of inputs and outputs

EQUIVALENT OF SERIAL AND DATA INPUTS

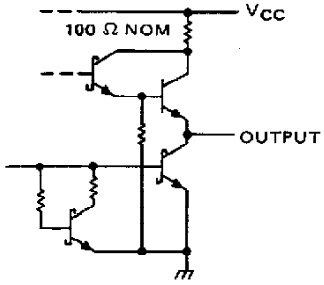


Serial: R_{eq} = 30 kΩ NOM
A, B, C, D: R_{eq} = 20 kΩ NOM

EQUIVALENT OF CLK, LD/$\overline{SH}$, AND OC INPUTS



TYPICAL OF ALL OUTPUTS



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