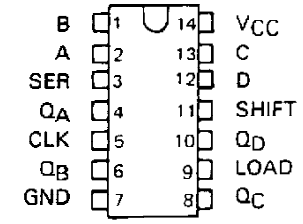
SN54178, SN74178
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

SDLS070

DECEMBER 1972 – REVISED MARCH 1988

- Typical Maximum Clock Frequency . . . 39 MHz
- Three Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Hold (Do Nothing)
- Negative-Edge-Triggered Clocking
- D-C Coupling Symplifies System Designs

SN54178 . . . J OR W PACKAGE
(TOP VIEW)



description

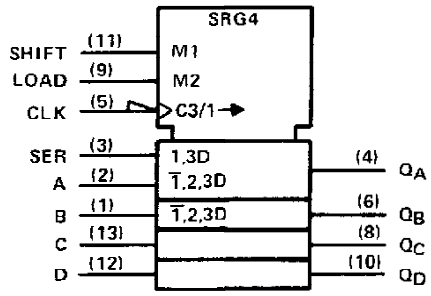
These shift registers utilize fully d-c coupled storage elements and feature synchronous parallel inputs and parallel outputs.

Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is inhibited.

Shift right is also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input.

When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register.

logic symbol†



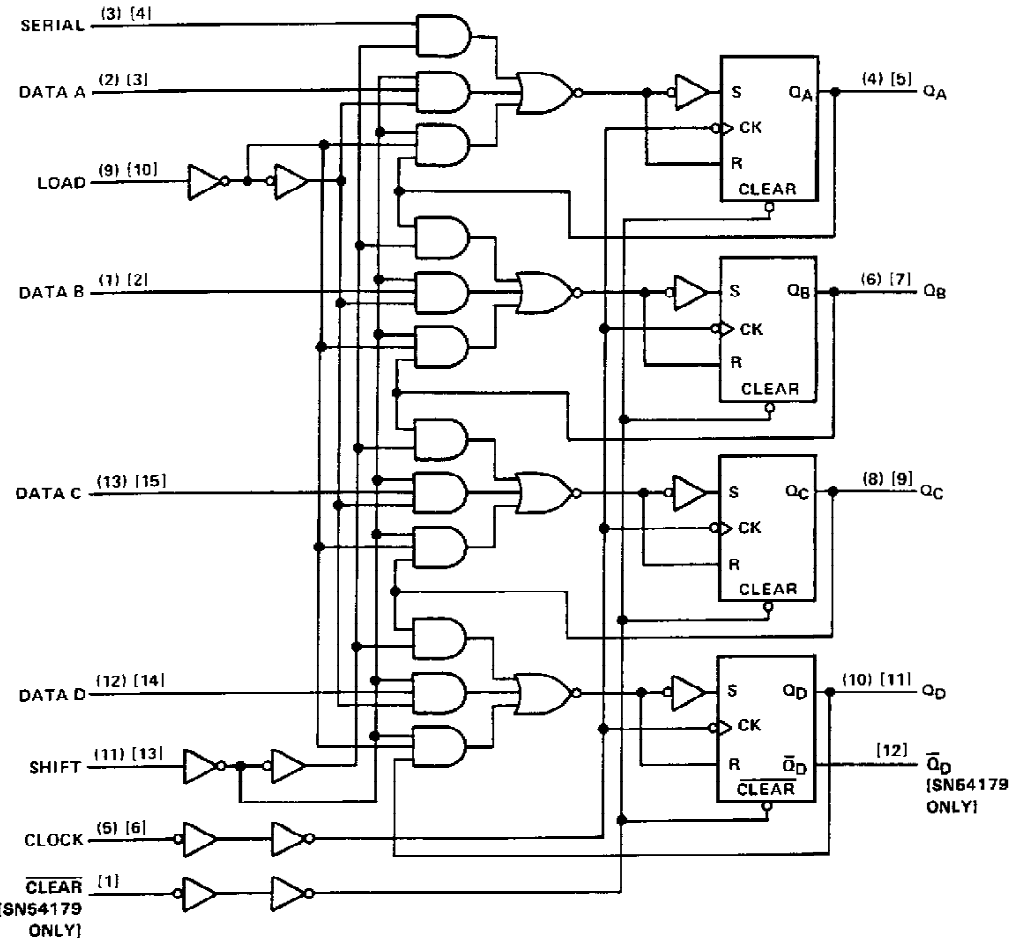
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617.12.

FUNCTION TABLE

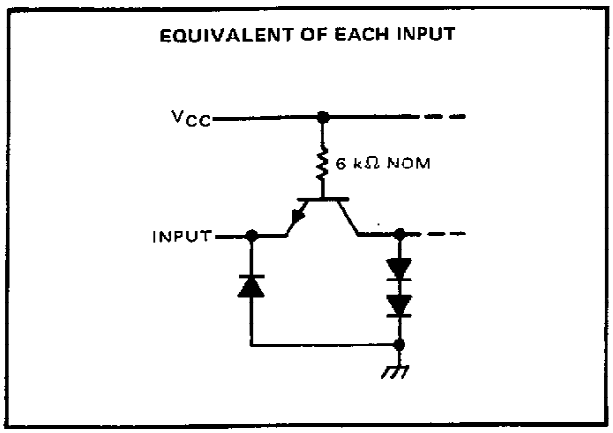
INPUTS								OUTPUTS			
SHIFT	LOAD	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
				A	B	C	D				
X	X	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	L	↓	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	↓	X	a	b	c	d	a	b	c	d
H	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

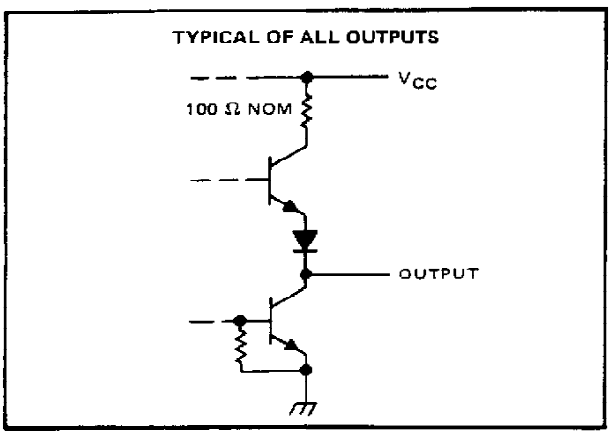
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or $\overline{Q}_D$, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↓ transition of the clock.

logic diagram (positive logic)



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54178 . . . . . −55°C to 125°C
SN74178 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54178			SN74178			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)		20			20			ns
Setup time t_{su} (see Figure 1)	Shift (H or L) or load	35			35			ns
	Data	30			30			
Hold time at any input, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54178			SN74178			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		46	70		46	75	mA

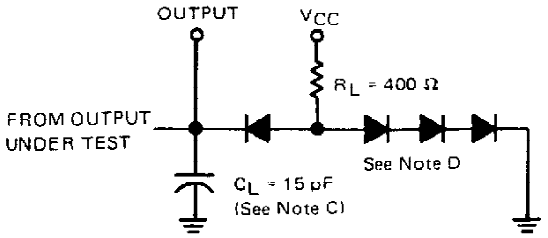
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured as follows:
a) 4.5 V is applied to serial inputs, load, shift, and $\overline{\text{clear}}$.
b) Parallel inputs A through D are grounded.
c) 4.5 V is momentarily applied to clock which is then grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

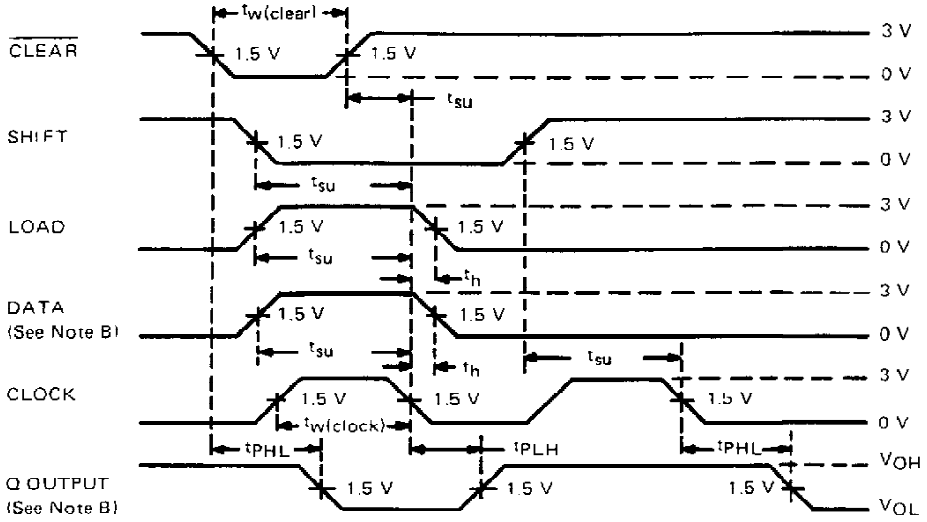
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	39		MHz
t_{PLH}	$\overline{Clear}$	$\overline{Q_D}$			15	23	ns
t_{PHL}		Q_A, Q_B, Q_C, Q_D			24	36	
t_{PLH}	Clock	Any output			17	26	ns
t_{PHL}					23	35	

†f_{max} = Maximum clock frequency
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PLH} = Propagation delay time, low-to-high-level output

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. Data input and Q output are any related pair. Serial and other data inputs are at GND. Serial data input is tested in conjunction with Q_A output in the shift mode.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064 or equivalent.

FIGURE 1–SWITCHING TIMES

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