- D-C Triggered from Active-High or Active-Low Gated Logic Inputs

- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle

- Overriding Clear Terminates Output Pulse

- '122 and 'LS122 Have Internal Timing Resistors

description

These d-c triggered multivibrators feature output pulse-duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122 and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.
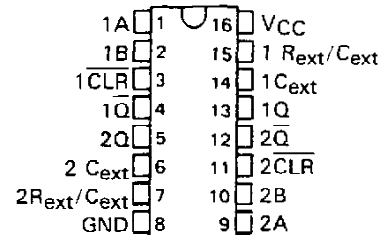
The R_{int} in nominall 10 kΩ for '122 and 'LS122.

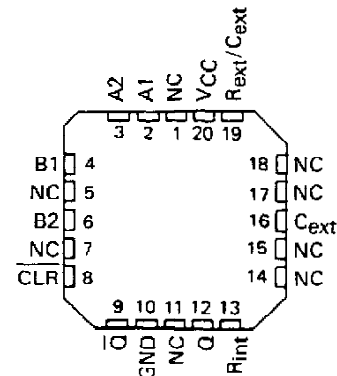**SN54123, SN54130, SN54LS123 . . . J OR W PACKAGE**
SN74123, SN74130 . . . N PACKAGE
SN74LS123 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

1A	1	16	V_{CC}
1B	2	15	1 R_{ext}/C_{ext}
1$\overline{CLR}$	3	14	1C_{ext}
1$\overline{Q}$	4	13	1Q
2$\overline{Q}$	5	12	2Q
2 C_{ext}	6	11	2$\overline{CLR}$
2R_{ext}/C_{ext}	7	10	2B
GND	8	9	2A

SN54LS122 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

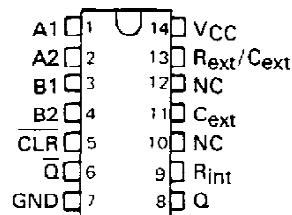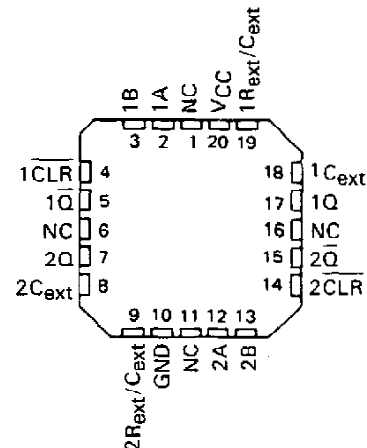**SN54122, SN54LS122 . . . J OR W PACKAGE**
SN74122 . . . N PACKAGE
SN74LS122 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

A1	1	14	V_{CC}
A2	2	13	R_{ext}/C_{ext}
B1	3	12	NC
B2	4	11	C_{ext}
$\overline{CLR}$	5	10	NC
$\overline{Q}$	6	9	R_{int}
GND	7	8	Q

SN54LS123 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

NC - No internal connection

NOTES:
1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse duration accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse durations, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

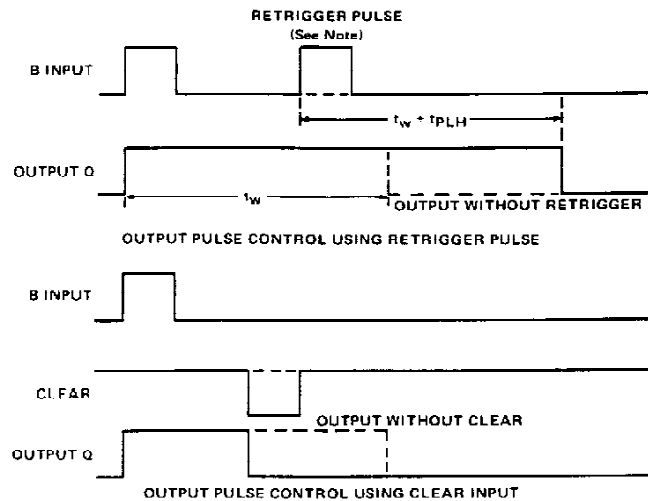# SN54122, SN54123, SN54130, SN54LS122, SN54LS123,
SN74122, SN74123, SN74130, SN74LS122, SN74LS123
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

description (continued)

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulses starting before $0.22\, C_{ext}$ (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output duration will remain unchanged.

'122, 'LS122
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

'123, '130, 'LS123
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

See explanation of function tables on page
† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

logic diagram (positive logic)

logic symbol†
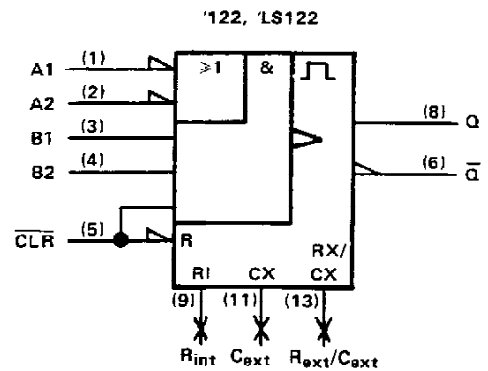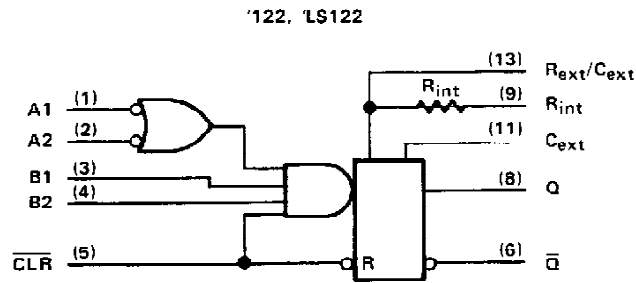
'122, 'LS122

R_{int} is nominally 10 kΩ for '122 and 'LS122

logic diagram (positive logic) (each multivibrator)

logic symbol†

'123, '130, 'LS123
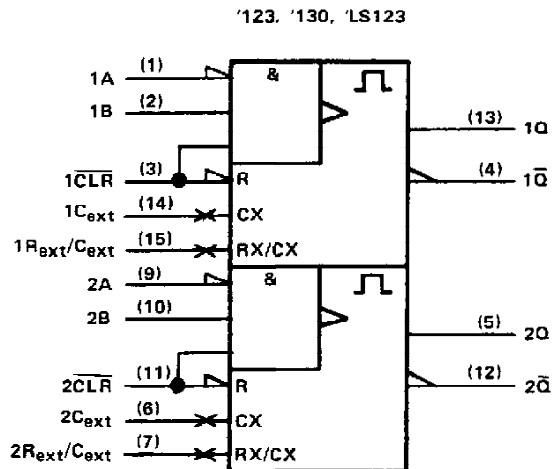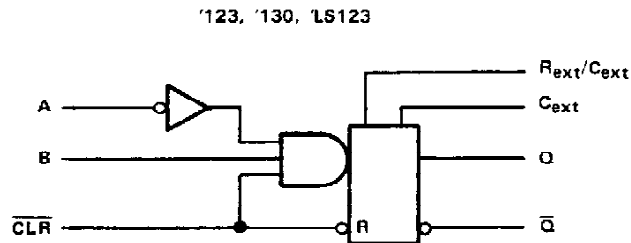
Pin numbers shown are for D, J, N, and W packages.

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs

'122, '123, '130 CIRCUITS

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS

R_{eq}

100 Ω NOM

Clear inputs : R_{eq} = 2 kΩ NOM
Other inputs : R_{eq} = 4 kΩ NOM

'LS122, 'LS123 CIRCUITS

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS

17 kΩ NOM

120 Ω NOM
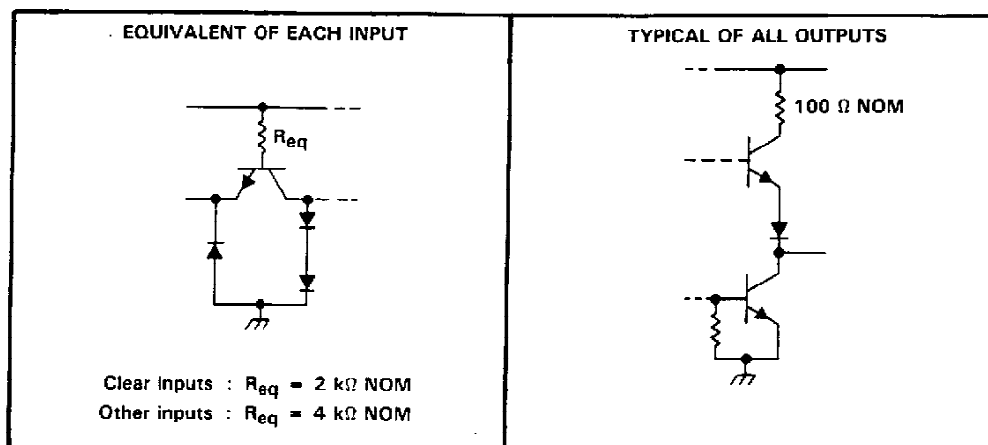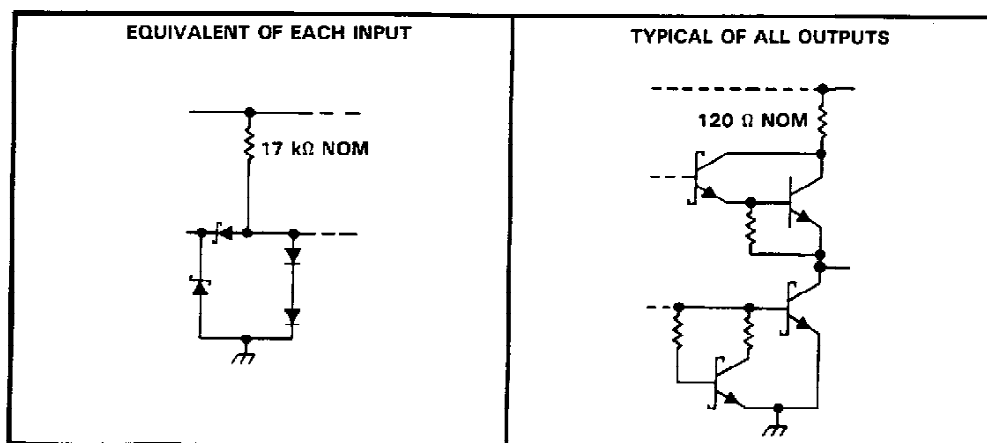
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: '122, '123, '130 . . . . 5.5 V
'LS122, 'LS123 . . . . 7 V
Operating free-air temperature range: SN54' . . . . −55°C to 125°C
SN74' . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54' MIN	SN54' NOM	SN54' MAX	SN74' MIN	SN74' NOM	SN74' MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Pulse duration, t_w	40			40			ns
External timing resistance, R_{ext}	5		25	5		50	kΩ
External capacitance, C_{ext}		No restriction			No restriction		
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'122 MIN	'122 TYP‡	'122 MAX	'123, '130 MIN	'123, '130 TYP‡	'123, '130 MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA, See Note 5	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA, See Note 5		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current — Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
	High-level input current — Clear input				80			80	
I_{IL}	Low-level input current — Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
	Low-level input current — Clear input				−3.2			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX, See Note 5	−10		−40	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX, See Notes 6 and 7		23	36		46	66	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
     6. Quiescent I_{CC} is measured (after clearing) with 4.5 V applied to all clear and A inputs, B inputs grounded, all outputs open and R_{ext} = 25 kΩ. R_{int} of '122 is open.
     7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 8

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122, '130 MIN	'122, '130 TYP	'122, '130 MAX	'123 MIN	'123 TYP	'123 MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 400 Ω		22	33		22	33	ns
	B				19	28		19	28	
t_{PHL}	A	$\overline{Q}$			30	40		30	40	ns
	B				27	36		27	36	
t_{PHL}	Clear	Q			18	27		18	27	ns
t_{PLH}		$\overline{Q}$			30	40		30	40	
t_{wQ} (min)	A or B	Q			45	65		45	76	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω	3.08	3.42	3.76	2.76	3.03	3.37	μs

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{wQ} = duration of pulse at output Q.
NOTE 8: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

	SN54LS' MIN	SN54LS' NOM	SN54LS' MAX	SN74LS' MIN	SN74LS' NOM	SN74LS' MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse duration, t_W	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	$k\Omega$
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{ILmax} I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX, See Note 13	'LS122		6	11		6	11	mA
			'LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 12. To measure V_{OH} at Q, V_{OL} at $\bar{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
   13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to A or B inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 8)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Q			23	33	ns
	B				23	44	
t_{PHL}	A	$\bar{Q}$	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 2 kΩ		32	45	ns
	B				34	56	
t_{PHL}	Clear	$\bar{Q}$			20	27	ns
t_{PLH}		$\bar{Q}$			28	45	
t_{wQ} (min)	A or B	Q			116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 2 kΩ	4	4.5	5	μs

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{wQ} = duration of pulse at output Q.
NOTE 8: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse durations when $C_{ext} \leq 1000$ pF, see Figure 4.

The output pulse duration is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse duration (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

where

K is 0.32 for '122, 0.28 for '123 and '130

R_T is in kΩ (internal or external timing resistance.)

C_{ext} is in pF

t_w is in ns

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse duration is:

$$t_w = K_D \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

K_D is 0.28 for '122, 0.25 for '123 and '130

TIMING COMPONENT CONNECTIONS
FIGURE 3
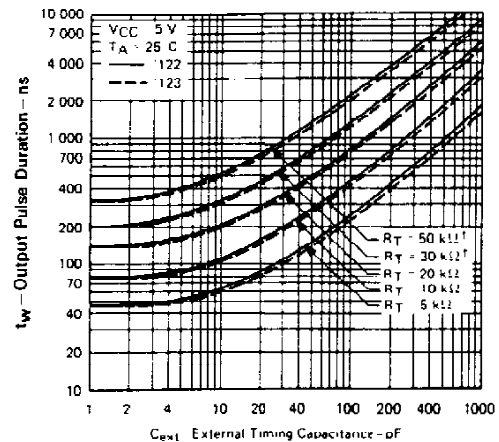

TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE

FIGURE 4

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' circuits.

$R_{ext} \leq 0.6 R_{ext} max.$
(See recommended operating conditions for $R_{ext}max$.)

Any silicon switching diode such as 1N3064 or equivalent.

TIMING COMPONENT CONNECTIONS WHEN
$C_{ext} > 1000$ p F AND CLEAR IS USED
FIGURE 2

Applications requiring more precise pulse durations (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when $C_{ext} \leq 1000$ pF, use Figure 6, or use Figure 7 where the pulse duration may be defined as:

$$t_w = K \cdot R_T \cdot C_{ext}$$

When $C_{ext} \geq 1$ μF, the output pulse width is defined as:

$$t_w = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

K is multiplier factor, see Figure 7
R_T is in kΩ (internal or external timing resistance)
C_{ext} is in pF
t_w is in ns

For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.
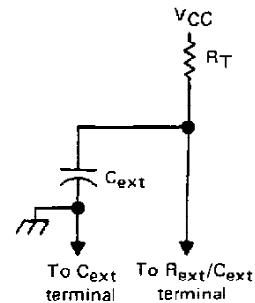
TIMING COMPONENT CONNECTIONS
FIGURE 5

'LS122, 'LS123
TYPICAL OUTPUT PULSE DURATION
vs
EXTERNAL TIMING CAPACITANCE
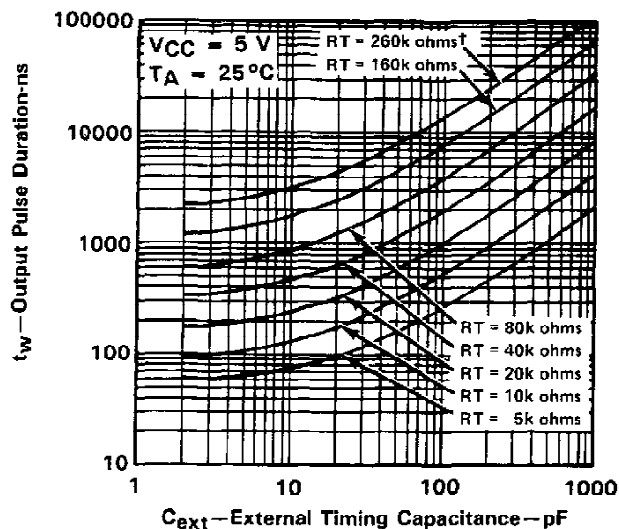
†This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 6

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123†

MULTIPLIER FACTOR
vs
EXTERNAL CAPACITOR

(K IS INDEPENDENT OF R)

C_{ext} — External Capacitor Value — uF

K — Multiplier Factor —

FIGURE 7

DISTRIBUTION OF UNITS
vs
OUTPUT PULSE DURATION

V_{CC} = 5 V
T_A = 25°C

Relative Frequency of Occurance

MEDIAN
− 20%

MEDIAN
+ 20% − ('LS122)

See Note 14

− 8%

+8% − ('LS122/
'LS123)

|←MEDIAN→|98% OF UNITS

$t_{w(out)}$—Output Pulse Duration

FIGURE 8

VARIATION IN OUTPUT PULSE DURATION
vs
SUPPLY VOLTAGE

C_{ext} = 60 pF
R_{ext} = 10 K ohms
T_A = 25°C

$t_{w(out)}$ ≈ 370 ns
at V_{CC} = 5 V

$\Delta t_{w(out)}$—Variation in Output Pulse Duration

V_{CC} — Supply Voltage — V

FIGURE 9

VARIATION IN OUTPUT PULSE DURATION
vs
FREE-AIR TEMPERATURE

V_{CC} = 5 V
C_{ext} = 60 pF
R_T = 10 K ohms

'LS122

$t_{w(out)}$ ≈ 370 ns
at T_A = 25°C

'LS122/'LS123
See Note 14

$\Delta t_{w(out)}$ — Variation in Output Pulse Duration

T_A — FREE-AIR TEMPERATURE −°C
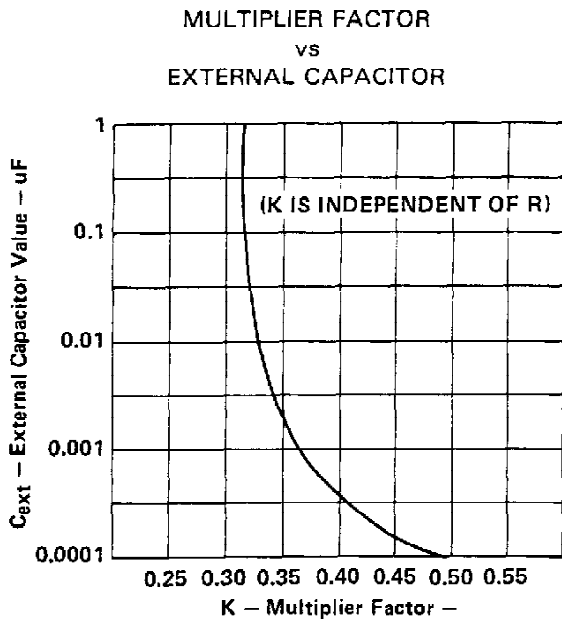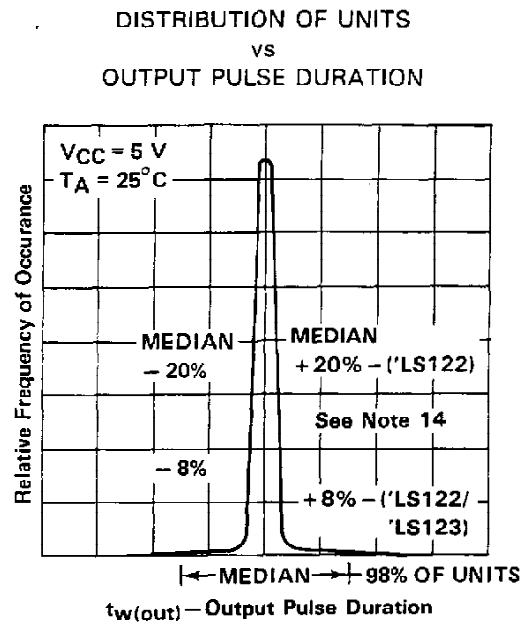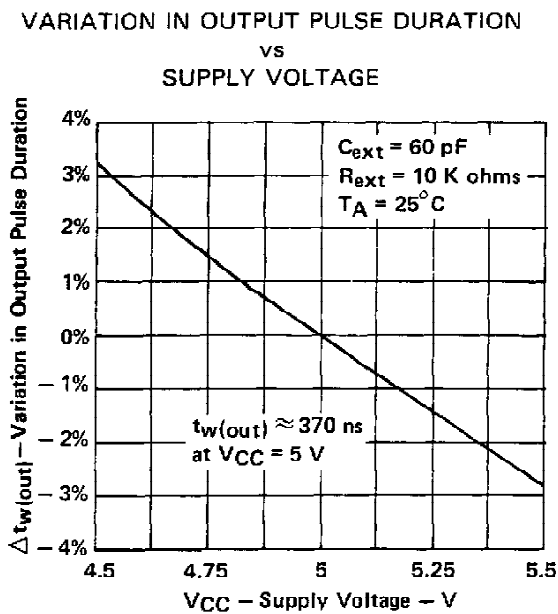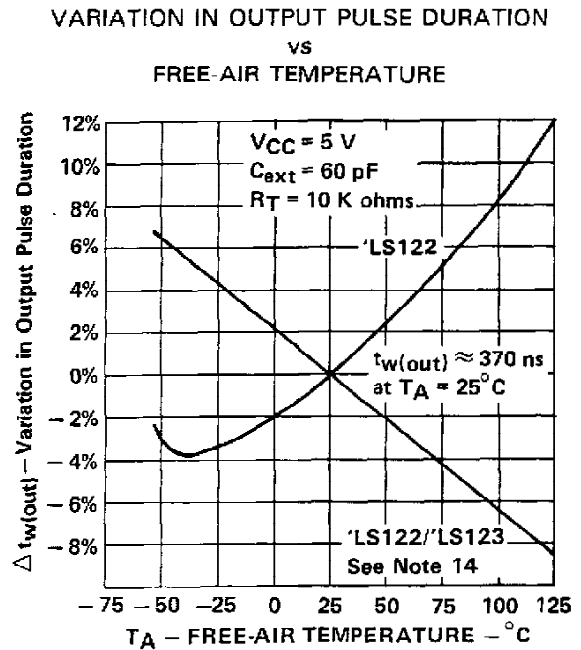
FIGURE 10

NOTE 14: For the 'LS122, the internal timing resistor, R_{int} was used. For the 'LS122/123, an external timing resistor was used for R_T.
†Data for temperatures below 0°C and above 70°C and for suply voltages below 4.75 V and above 5.25 V are applicable for SN54LS122 and SN54LS123 only.

TEXAS
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