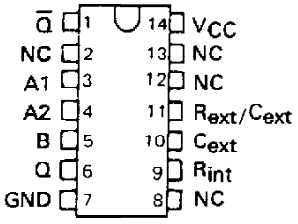
# SN54121, SN74121
# MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

MAY 1983 – REVISED MARCH 1988

- Programmable Output Pulse Width
  With $R_{int}$ . . . 35 ns Typ
  With $R_{ext}/C_{ext}$ . . . 40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

SN54121 . . . J OR W PACKAGE
SN74121 . . . N PACKAGE
(TOP VIEW)

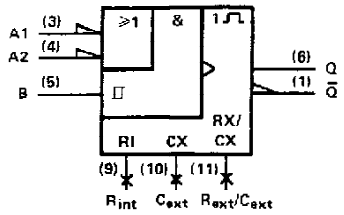



NC - No internal connection.

FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A1 | A2 | B | Q | Q̄ |
| L | X | H | L | H |
| X | L | H | L† | H† |
| X | X | L | L† | H† |
| H | H | X | L† | H† |
| H | ↓ | H | ⎍ | ⎍ |
| ↓ | H | H | ⎍ | ⎍ |
| ↓ | ↓ | H | ⎍ | ⎍ |
| L | X | ↑ | ⎍ | ⎍ |
| X | L | ↑ | ⎍ | ⎍ |

## logic symbol‡




‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

For explanation of function table symbols, see page

† These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

## description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

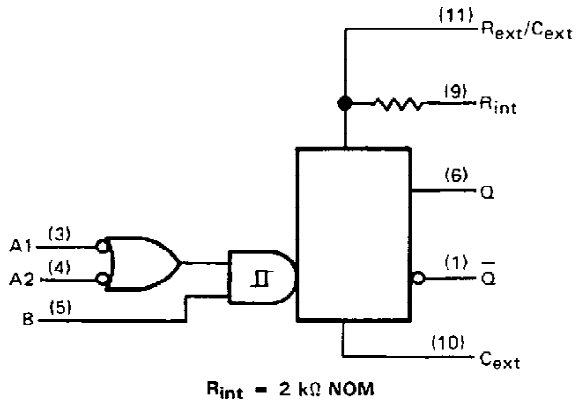
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to $V_{CC}$ noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., $R_{int}$ connected to $V_{CC}$, $C_{ext}$ and $R_{ext}/C_{ext}$ open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of $V_{CC}$ and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and $V_{CC}$ ranges for more than six decades of timing capacitance (10 pF to 10 $\mu$F) and more than one decade of timing resistance (2 k$\Omega$ to 30 k$\Omega$ for the SN54121 and 2 k$\Omega$ to 40 k$\Omega$ for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_T\ln 2 \approx 0.7\ C_{ext}R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 $\mu$F and timing resistance as low as 1.4 k$\Omega$ may be used. Also, the range of jitter-free output pulse widths is extended if $V_{CC}$ is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended $R_T$. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

## logic diagram (positive logic)



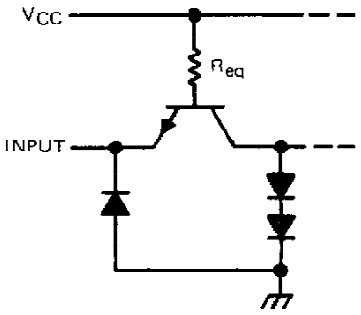

$R_{int}$ = 2 kΩ NOM

Pin numbers shown on logic notation are for J or N packages.

NOTES: 1. An external capacitor may be connected between $C_{ext}$ (positive) and $R_{ext}/C_{ext}$.
2. To use the internal timing resistor, connect $R_{int}$ to $V_{CC}$. For improved pulse width accuracy and repeatability, connect an external resistor between $R_{ext}/C_{ext}$ and $V_{CC}$ with $R_{int}$ open-circuited.

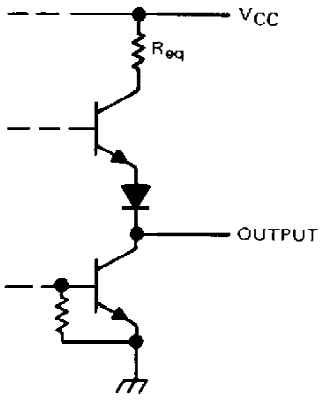
## schematics of inputs and outputs

EQUIVALENT OF EACH INPUT




| INPUT | $R_{eq}$ NOM |
|---|---|
| A1 | 4 kΩ |
| A2 | 4 kΩ |
| B | 2 kΩ |

TYPICAL OF BOTH OUTPUTS




$R_{eq}$ = 130 Ω NOM

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 3) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54121 . . . . . −55°C to 125°C
SN74121 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 3: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 54 Family | 4.5 | 5 | 5.5 | V |
| | | | 74 Family | 4.75 | 5 | 5.25 | |
| $I_{OH}$ | High-level output current | | | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | | 16 | mA |
| dv/dt | Rate of rise or fall of input pulse | Schmitt input, B | | 1 | | | V/s |
| | | Logic inputs, A1, A2 | | 1 | | | V/μs |
| $t_{w(in)}$ | Input pulse width | | | 50 | | | ns |
| $R_{ext}$ | External timing capacitance | | 54 Family | 1.4 | | 30 | kΩ |
| | | | 74 Family | 1.4 | | 40 | |
| $C_{ext}$ | External timing capacitance | | | 0 | | 1000 | μF |
| | Duty cycle | $R_T$ = 2 kΩ | | | | 67 | % |
| | | $R_T$ = MAX $R_{ext}$ | | | | 90 | |
| $T_A$ | Operating free-air temperature | | 54 Family | −55 | | 125 | °C |
| | | | 74 Family | 0 | | 70 | |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage at B input | $V_{CC}$ = MIN | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage at A input | $V_{CC}$ = MIN | | | | 0.8 | V |
| $V_{T+}$ | Positive-going threshold voltage at B input | $V_{CC}$ = MIN | | | 1.55 | 2 | V |
| $V_{T-}$ | Negative-going threshold voltage at B input | $V_{CC}$ = MIN | | 0.8 | 1.35 | | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | −1.5 | V |
| $I_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, | $I_{OH}$ = MAX | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, | $I_{OL}$ = MAX | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | A1 or A2 | | | 40 | μA |
| | | | B | | | 80 | |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | A1 or A2 | | | −1.6 | mA |
| | | | B | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | 54 Family | −20 | | −55 | mA |
| | | | 74 Family | −18 | | −55 | |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX | Quiescent | | 13 | 25 | mA |
| | | | Triggered | | 23 | 40 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output from either A input | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 4 | $C_{ext}$ = 80 pF, $R_{int}$ to $V_{CC}$ | | 45 | 70 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output from B input | | | | 35 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low level $\overline{Q}$ output from either A input | | | | 50 | 80 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low level $\overline{Q}$ output from B input | | | | 40 | 65 | ns |
| $t_{w(out)}$ | Pulse width obtained using internal timing resistor | | $C_{ext}$ = 80 pF, $R_{int}$ to $V_{CC}$ | 70 | 110 | 150 | ns |
| $t_{w(out)}$ | Pulse width obtained with zero timing capacitance | | $C_{ext}$ = 0, $R_{int}$ to $V_{CC}$ | | 30 | 50 | ns |
| $t_{w(out)}$ | Pulse width obtained using external timing resistor | | $C_{ext}$ = 100 pF, $R_T$ = 10 kΩ | 600 | 700 | 800 | ns |
| | | | $C_{ext}$ = 1 μF, $R_T$ = 10 kΩ | 6 | 7 | 8 | ms |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

## TYPICAL CHARACTERISTICS†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

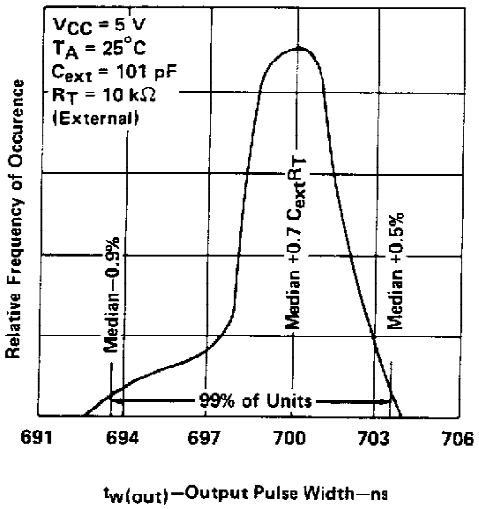



FIGURE 1

VARIATION IN INTERNAL TIMING RESISTOR VALUE
vs
FREE-AIR TEMPERATURE

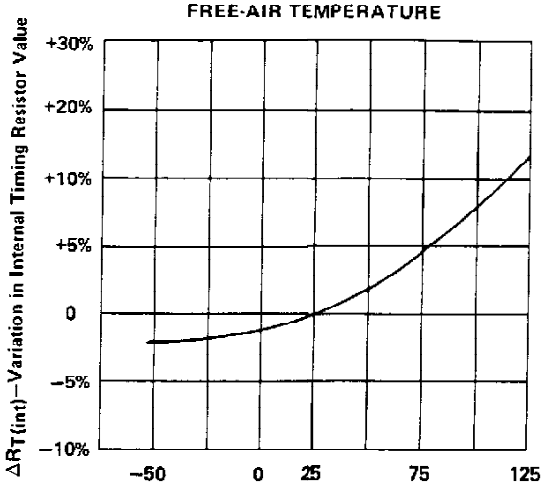



FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

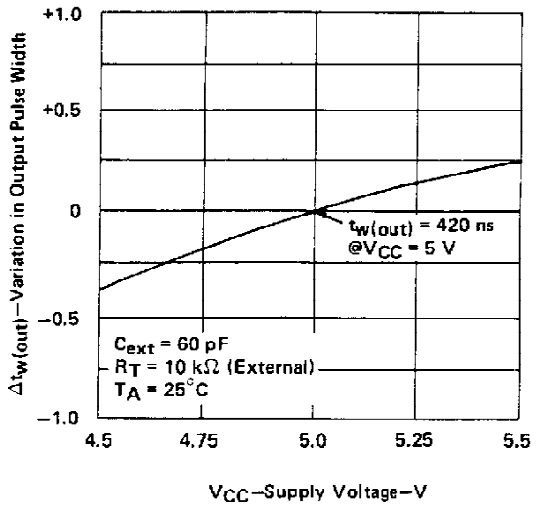



FIGURE 3

SCHMITT TRIGGER THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

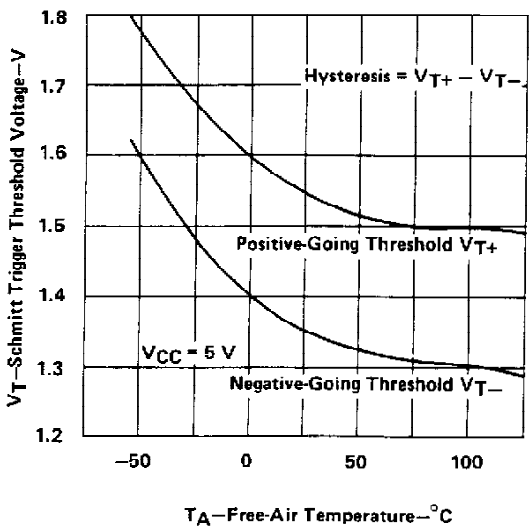



FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SN54121.

## TYPICAL CHARACTERISTICS† (continued)

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

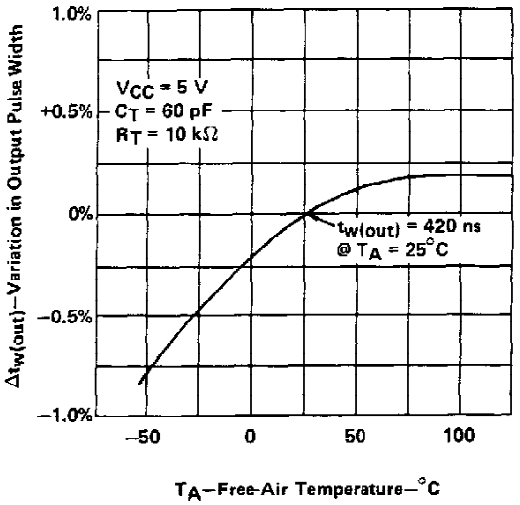



FIGURE 5

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

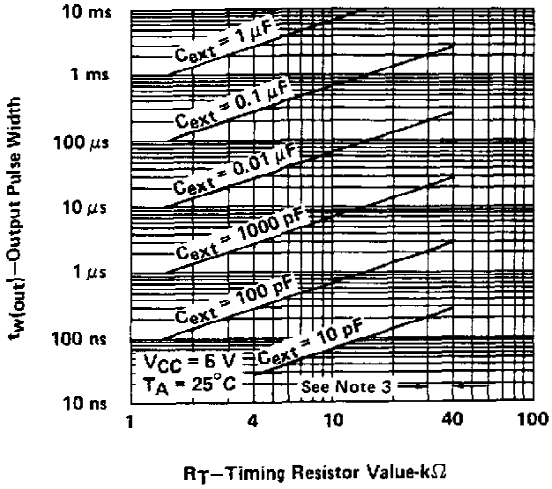



FIGURE 6

OUTPUT PULSE WIDTH
vs
EXTERNAL CAPACITANCE

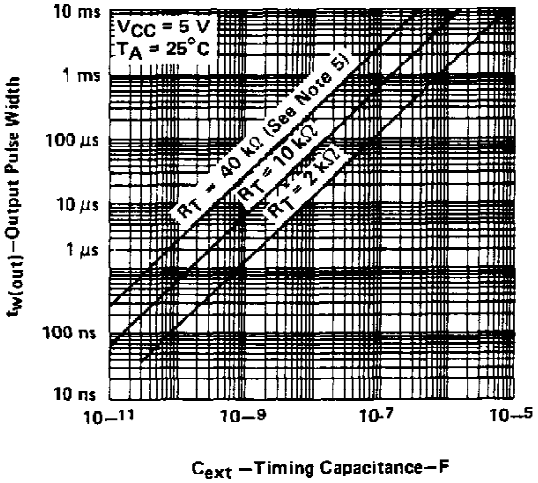



FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121.
†Data for temperatures below 0°C and above 70°C are applicable for SN54121.

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