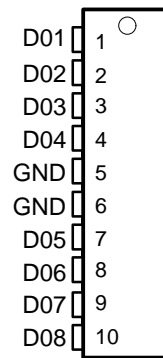- **Designed to Reduce Reflection Noise**
- **Repetitive Peak Forward Current . . . 200 mA**
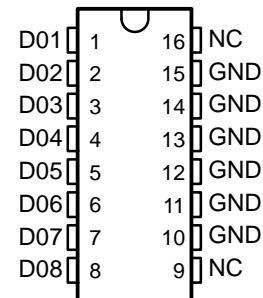- **8-Bit Array Structure Suited for Bus-Oriented Systems**

description

This Schottky barrier diode bus termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1056A is characterized for operation from 0°C to 70°C.
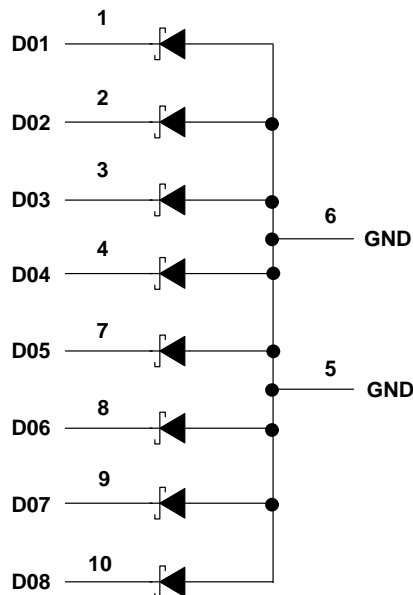
SC PACKAGE
(TOP VIEW)

D01	1	
D02	2	
D03	3	
D04	4	
GND	5	
GND	6	
D05	7	
D06	8	
D07	9	
D08	10	

D PACKAGE
(TOP VIEW)

D01	1	16	NC
D02	2	15	GND
D03	3	14	GND
D04	4	13	GND
D05	5	12	GND
D06	6	11	GND
D07	7	10	GND
D08	8	9	NC

schematic diagrams

(SC PACKAGE)

(D PACKAGE)

1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady state reverse voltage, V_R .... 7 V
Continuous forward current, I_F: any D terminal from GND .... 50 mA
                                                  total through all GND terminals .... 170 mA
Repetitive peak forward current, I_{FRM}‡: any D terminal from GND .... 200 mA
                                                              total through all GND terminals .... 1.0 A
Continuous total power dissipation at (or below) 25°C free-air temperature .... 735 mW
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ These values apply for $t_w \leq 100$ μs, duty cycle $\leq 20\%$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_R	Static reverse current	$V_R = 7$ V				5	μA
V_F	Static forward voltage	$I_F = 18$ mA			0.75	0.95	V
		$I_F = 50$ mA			0.95	1.2	
V_{FM}	Peak forward voltage	$I_F = 200$ mA			1.30		V
C_T	Total capacitance	$V_R = 0$ V,	f = 1 MHz		5	7	pF
		$V_R = 2$ V,	f = 1 MHz		4	6	

NOTE 1:   Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER		TEST CONDITIONS		MIN	TYP§	MAX	UNIT
I_X	Internal crosstalk current	Total I_F current = 1 A,	See Note 2		0.6	2	mA
		Total I_F current = 270 mA,	See Note 2		0.02	0.2	mA

§ All typical values are at $T_A = 25$°C.
NOTE 2: I_X is measured under the following conditions with one diode static, all others switching:
          Switching diodes: $t_w = 100$ μs, duty cycle = 20%;
          Static diode: $V_R = 5$ V
          The static diode input current is the internal crosstalk current I_X.

switching characteristics, $T_A = 25$°C (see Figures 1 and 2)

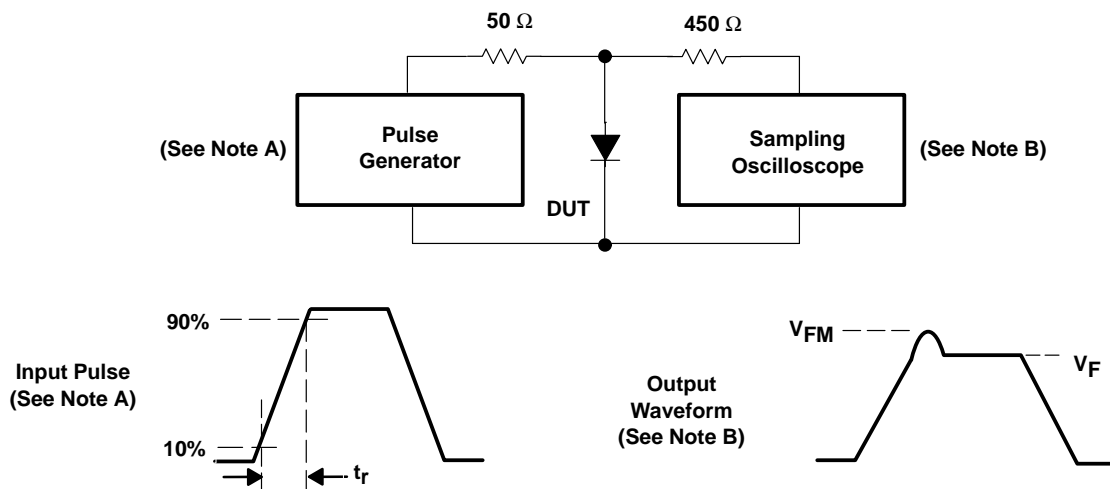| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr}	Reverse recovery time	$I_F = 10$ mA, $I_{RM} = 10$ mA, $I_R = 1$ mA, $R_L = 100$ Ω		8	10	ns

PARAMETER MEASUREMENT INFORMATION

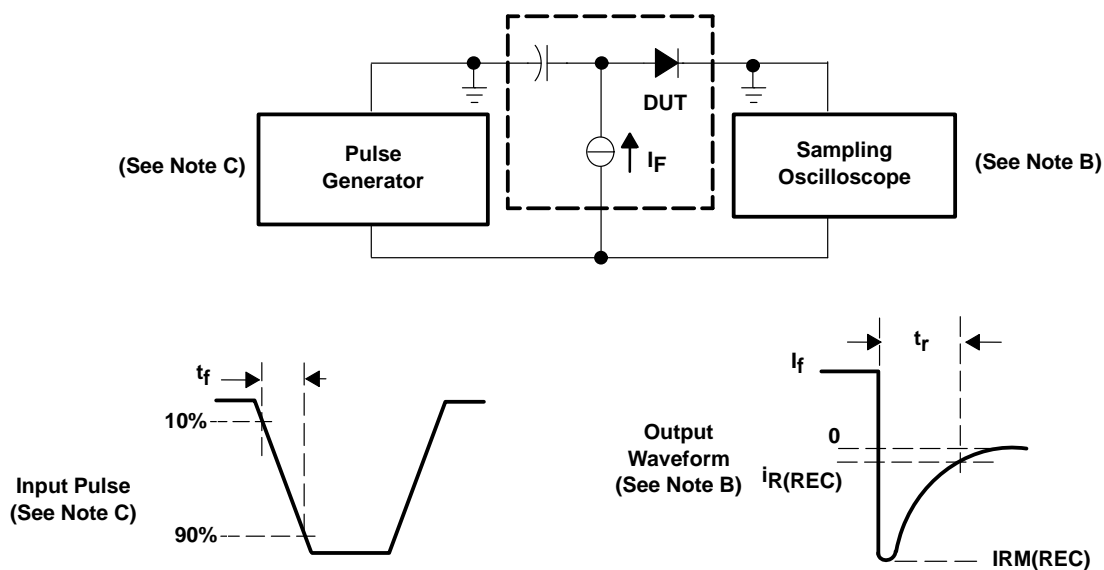**Figure 1. Forward Recovery Voltage**

Figure 2. Reverse Recovery Time

NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: t_r = 20 ns, Z_O = 50 Ω, freq = 500 Hz, duty cycle = 0.01.

B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq$ 350 ps, R_i = 50 Ω, $C_i = \leq$ 5 pF.

C. The input pulse is supplied by a pulse generator having the following characteristics: t_f = 0.5 ns, Z_O = 50 Ω, $t_w = \geq$ 50 ns, duty cycle = 0.01.

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1056 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current-voltage for the SN74S1056 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 4(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.
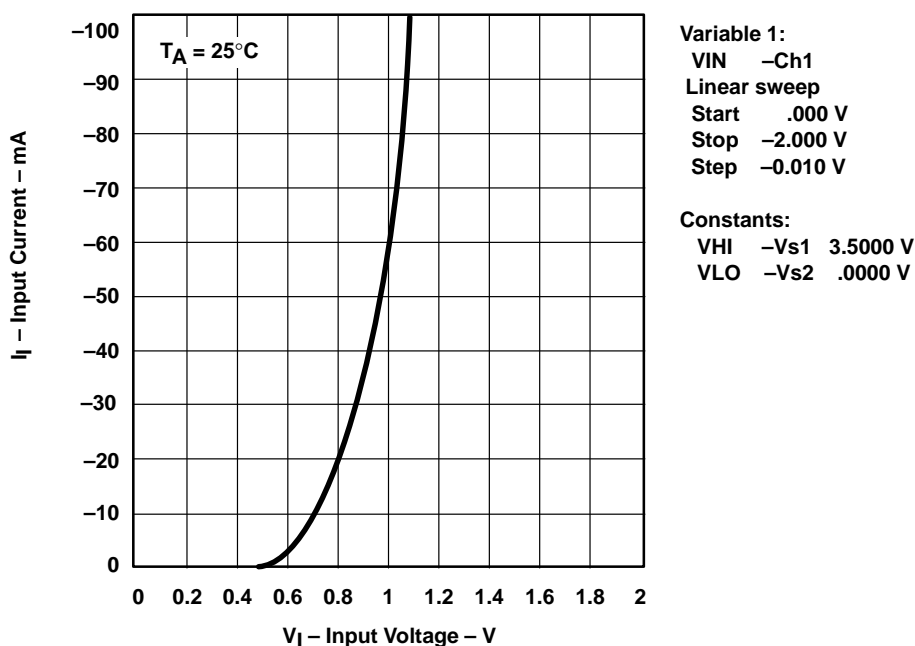

Figure 3. Typical Current-Voltage Curve

Z$_O$ = 50 Ω
Length = 36 in

(a) DIODE TEST SETUP

31.500 ns   **56.500 ns**   **81.500 ns**

**End-of-
Line
without
Diode**

End-of-Line with Diode

Vmarker 1

Vmarker 2

Ch 2   =   1.880 volts / div
Timebase =   5.00 ns / volt
Memory 1 =   1.880 volts / div
Vmarker 1 =   −1.353 volts
Vmarker 2 =   −3.647 volts

Offset   =   0.000 volts
Delay   =   56.500 ns
Delta V   =   −2.293 volts

(b) SCOPE DISPLAY

Figure 4. Diode Test Setup and Scope Display

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