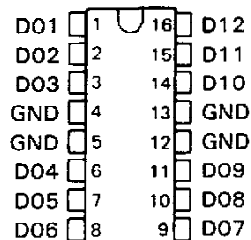


# **SN74S1050** **12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY**

SDLS015A D3228, JULY 1989—REVISED MARCH 1990

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems
- ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015
- Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs

**D OR N PACKAGE**  
(TOP VIEW)

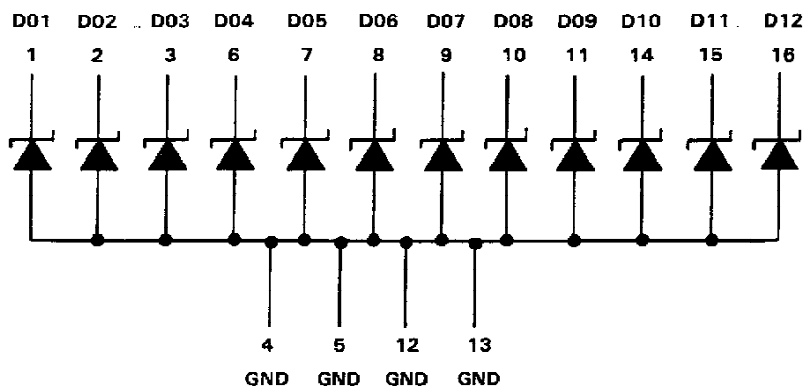


## description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1050 is characterized for operation from 0°C to 70°C.

## schematic diagram



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS**  
**INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1990, Texas Instruments Incorporated

# SN74S1050

## 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

D3228, JULY 1989—REVISED MARCH 1990

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Steady-state reverse voltage, $V_R$	7 V
Continuous forward current, $I_F$ : any D terminal from GND	50 mA
total through all GND terminals	170 mA
Repetitive peak forward current, $I_{FRM}$ : any D terminal from GND	200 mA
total through all GND terminals	1 A
Continuous total power dissipation at (or below) 25°C free-air temperature	625 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

<sup>†</sup>Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup>These values apply for  $t_W \leq 100 \mu s$ , duty cycle  $\leq 20\%$ .

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

#### single-diode operation (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>§</sup>	MAX	UNIT
$I_R$ Static reverse current	$V_R = 7 V$			5	$\mu A$
$V_F$ Static forward voltage	$I_F = 18 mA$	0.75	0.95		V
	$I_F = 50 mA$	0.95	1.2		
$V_{FM}$ Peak forward voltage	$I_F = 200 mA$		1.45		V
$C_T$ Total capacitance	$V_R = 0, f = 1 MHz$		5	10	pF
	$V_R = 2 V, f = 1 MHz$		4	8	

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

#### multiple-diode operation

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>§</sup>	MAX	UNIT
$I_X$ Internal crosstalk current	Total $I_F = 1 A$ , See Note 2		0.6	2	mA
	Total $I_F = 198 mA$ , See Note 2		0.02	0.2	

<sup>§</sup>All typical values are at  $T_A = 25^\circ C$ .

NOTE 2:  $I_X$  is measured under the following conditions with one diode static and all others switching:

Switching diodes:  $t_W = 100 \mu s$ , duty cycle = 20%; static diode:  $V_R = 5 V$ .

The static diode's input current is the internal crosstalk current  $I_X$ .

### switching characteristics at 25°C free-air temperature (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{rr}$ Reverse recovery time	$I_F = 10 mA, I_{RM}(REC) = 10 mA, I_R(REC) = 1 mA, R_L = 100 \Omega$		8	16	ns

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN74S1050

## 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

### PARAMETER MEASUREMENT INFORMATION

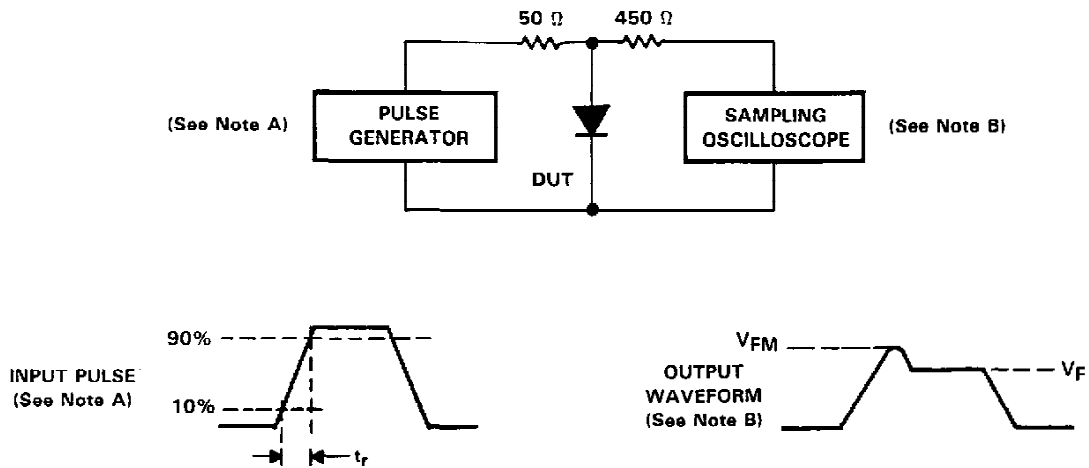


FIGURE 1. FORWARD RECOVERY VOLTAGE

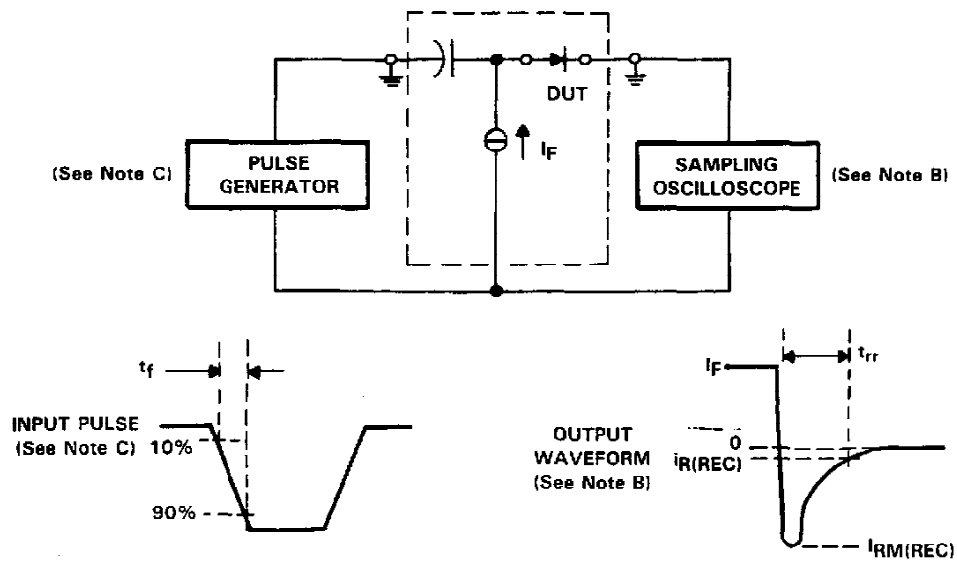


FIGURE 2. REVERSE RECOVERY TIME

- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics:  $t_r = 20$  ns,  $Z_{out} = 50$  Ω,  $f = 500$  Hz, duty cycle = 0.01.
- B. The output waveform is monitored by an oscilloscope having the following characteristics:  $t_r \leq 350$  ps,  $R_{in} = 50$  Ω,  $C_{in} = \leq 5$  pF.
- C. The input pulse is supplied by a pulse generator having the following characteristics:  $t_f = 0.5$  ns,  $Z_{out} = 50$  Ω,  $t_w = \geq 50$  ns, duty cycle  $\leq 0.01$ .

## SN74S1050 12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

### APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1052 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1052 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4 was evaluated. The resulting waveforms with and without the diode are shown in Figure 5.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

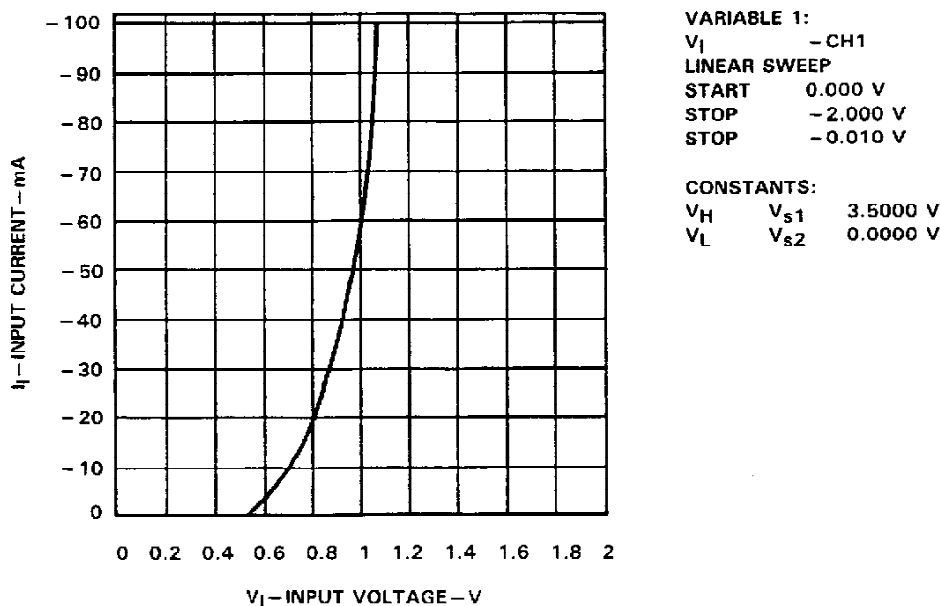


FIGURE 3. TYPICAL CURRENT-VOLTAGE CURVE

**SN74S1050**

**12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY**

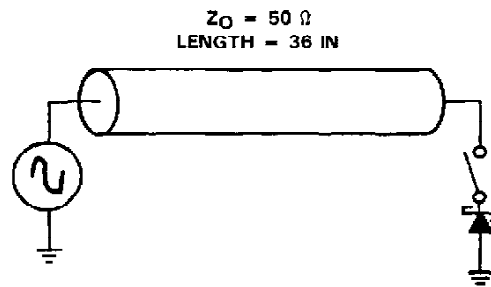


FIGURE 4. DIODE TEST SETUP

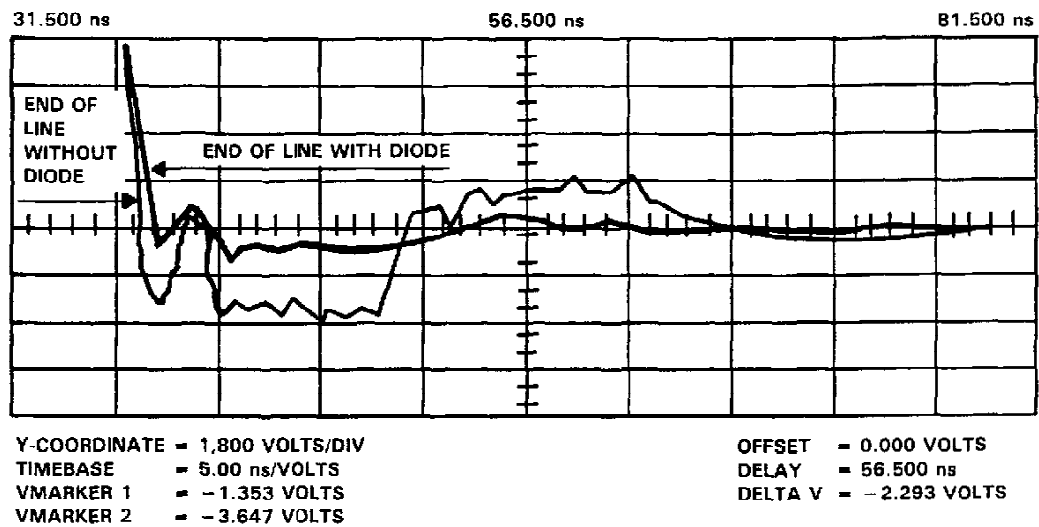


FIGURE 5. SCOPE DISPLAY

**TEXAS**  
**INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## **IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

**TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.**

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.