SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SDLS014

- Designed Specifically for High-Speed: Memory Decoders
 Data Transmission Systems
- 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Schottky-Clamped for High Performance

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these docoders can be used to minimize the effects of system decoding. When employed with highspeed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138, SN54S138, and SN74S138A decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

All of these decoder/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design.

The SN54LS138 and SN54S138 are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74LS138 and SN74S138A are characterized for operation from 0 °C to 70 °C.

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SN54LS138, SN54S138 J OR W PACKAGE SN74LS138, SN74S138A D OR N PACKAGE (TOP VIEW)
$A \begin{bmatrix} 1 \\ 0 \end{bmatrix} 16 \end{bmatrix} V_{CC}$ $B \begin{bmatrix} 2 \\ 15 \end{bmatrix} Y0$ $C \begin{bmatrix} 3 \\ 14 \end{bmatrix} Y1$ $\overline{G}2A \begin{bmatrix} 4 \\ 13 \end{bmatrix} Y2$ $\overline{G}2B \begin{bmatrix} 5 \\ 12 \end{bmatrix} Y3$ $G1 \begin{bmatrix} 6 \\ 11 \end{bmatrix} Y4$ $Y7 \begin{bmatrix} 7 \\ 10 \end{bmatrix} Y5$ $GND \begin{bmatrix} 8 \\ 9 \end{bmatrix} Y6$
SN54LS138, SN54S138 FK PACKAGE (TOP VIEW)
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

NC-No internal connection

logic symbols[†]



 [†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for D, J, N, and W packages.

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mbers shown are for D, S, N, and W packages



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SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE-TO 8-LINE DECODERS/DEMULTIPLEXERS

logic diagram and function table



Pin numbers shown are for D, J, N, and W packages.

	I)	IPUT	S							~		
ENABLE		S	SELECT			OUTPUTS						
G1	Ğ2*	С	8	Α	YO	Y1	Y2	Y3	Y4	Y5	Y6	¥7
х	н	X	x	X	н	н	н	Н	H	н	Н	н
L	х	x	х	x	н	н	н	н	н	н	н	н
н	Ĺ	L	L	L	L	н	н	н	н	н	н	н
н	L	L	L	н	н	Ļ	н	н	н	н	н	н
н	L	L	н	L	н	н	L	н	н	н	н	H
н	L	L	н	н	н	н	н	L	н	Н	н	н
н	L	н	Ļ	L	н	н	н	н	L	н	Н	н
н	L	н	L	н	н	н	н	н	н	L.	н	н
н	Ł	н	н	L	н	н	н	Н	н	н	L	н
н	L	н	н	н	н	н	н	н	н	н	н	L

'LS138, SN54138, SN74S138A FUNCTION TABLE

* $\overline{G}2 = \overline{G}2A + \overline{G}2B$ H = high level, L = low level, X = irrelevant



SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage
Operating free-air temperature range: SN54LS138, SN54S138
SN74LS138, SN74S138A
Storage temperature range

NOTE 1: Voltage values are with respect to network ground terminal.



SN54LS138, SN74LS138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

recommended operating conditions

		SI	N54LS1	38	SI	N74LS1	38	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			v
VIL	Low-level input voltage			0.7			0.8	v
ЮН	High-level output current			-0.4			-0.4	mA
^I OL	Low-level output current			4			8	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				SN54LS138			S				
PARAMETER		MIN	TYP‡	MAX	MIN	TYP	MAX				
⊻ік	VCC = MIN,	_lj = -18 mA				- 1.5			-1.5	V	
Voн	V _{CC} = MIN, I _{OH} = -0.4 m	$V_{IH} = 2 V, V_{IL} = MAX,$		2.5	3.4		2.7	3.4		v	
	$V_{CC} = MIN,$	$V_{\rm H}$ = 2 V,	IOL = 4 mA		0.25	0.4		0.25	0.4		
VOL	$V_{IL} = MAX$		1 _{0L} = 8 mA					0.35	0.5	v	
ч	VCC = MAX	$V_{I} \neq 7 V$				Q.1			0.1	mA	
ЧН	$V_{CC} = MAX,$	VI = 2.7 V				20			20	μA	
- <u>-</u>	Vcc = MAX,		Enable			-0.4			-0.4	mА	
կլ	VCC = MAA,	VI = 0:4 V	A, B, C			-0.2			-0.2	ША	
los [§]	VCC - MAX			- 20		- 100	- 20		- 100	mΑ	
^I CC	$V_{CC} = MAX$	Outputs enabled and open			6.3	10		6.3	10	mA	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, $T_A = 25$ °C. [§]Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

PARAMETER	TER ¹ FROM TO LEVELS TEST CONDITIONS		154LS1: 174LS1:	UNIT																
	(INPUT)		OF DELAY			MIN	TYP	MAX												
^t PLH			2				11	20	ns											
^t PHL	Binary		•		A				A		*	.	A	2				18	41	ns
tpLH	Select	Απγ					21	27	ns											
^t PHL			3	RL = 2 kΩ.	Сլ = 15 рЕ,		20	39	ns											
^t PLH												See Note 2		12	18	ns				
tPHL	Enable		2	2	2	2	2	2			20	32	Э ns 3 ns 2 ns							
tPLH		Αηγ	2			(14	26	ns											
^t PHL			ۍ ا				13	38	ns											

switching characteristics, VCC = 5 V, TA = 25° C

 $\P_{tp_{LH}}$ = propagation delay time, low-to-high-level ouput

tpHL = propagation delay time, high-to-low-level output NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



SN54S138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)		<i>.</i>	 7 V
Input voltage			 5.5 V
Operating free-air temperature range:	SN54S138		 –55°C to 125°C
	SN74S138A		 0°C to 70°C
Storage temperature range			 -65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54S138 SN74S138			8A	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
VIL	Low-level input voltage			0.8			0.8	V
юн	High-level output current			- 1			-1	mΑ
^I OL	Low-level output current			20			20	mA
TA	Operating free-air temperature	- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	-	SN54S138 SN74S138A			UNIT		
				MIN	TYP [‡]	MAX	
Vik	$V_{CC} = MIN$	l∣ = −18 mA				-1.2	v
N	Martin Ballhi		SN54S'	2.5	3.4		V
∨он	V _{CC} ≠ MIN,	$V_{IH} = 2 V$, $V_{IL} = 0.8 V$. $I_{OH} = -1 mA$	SN74S'	2.7	3.4		· ·
VOL	$V_{CC} = MIN,$	V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA				0.5	V
4	$V_{CC} = MAX$	$V_{ } = 5.5 V$				1	mA
^I IH	VCC = MAX.	VI = 2.7 V				50	μA
۱ <u>۱</u> ۲	$V_{CC} = MAX,$	$V_1 = 0.5 V$				- 2	mΑ
los§	$V_{CC} = MAX$			-40	_	- 100	mA
'cc	$V_{CC} = MAX,$	Outputs enabled and open			49	74	mΑ

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25 °C.

[§] Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.



SN54S138, SN74S13BA **3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS**

switching characteristics, $V_{CC} = 5 V$, $T_A = 25 °C$

PARAMETER	FROM TO LEVELS TEST CONDITIONS		SN54S138 SN74S138A			UNIT												
	(INPUT)	(OUTPUT)	OF DELAY		MIN	ТҮР	MAX											
^t PLH			2			4.5	7	ns										
^t PHL	Binary		4	A	A	4	4	4	4.000	A	2			7	10.5	ns		
tPLH	Select	Any	3]		7.5	12	ns										
^t PHL		1	3	R _L ≕ 280 Ω, C _L = 15 pF		8	12	ns										
tPLH							<u> </u>						2	See Note 2		5	8	กร
^t PHL	Enable		2			7	11	ns										
^t PLH		Any		}	_	7	11	ns										
^t PHL		1 1							3	1		7	11	ris				

[†]tPLH = propagation delay time, low-to-high-level output
 tpHL = propagation delay time, high-to-low-level output
 NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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