

SN54LS114A, SN54S114, SN74LS114A, SN74S114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

MARCH 1973—REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Ceramic Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS114A and SN54S114 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS114A and SN74S114A are characterized for operation from 0°C to 70°C .

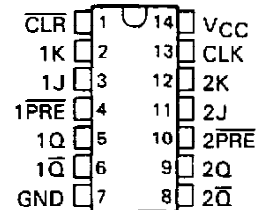
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^{\dagger}	H^{\dagger}
H	H	\downarrow	L	L	Q_0	\bar{Q}_0
H	H	\downarrow	L	H	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q_0	\bar{Q}_0

\dagger The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

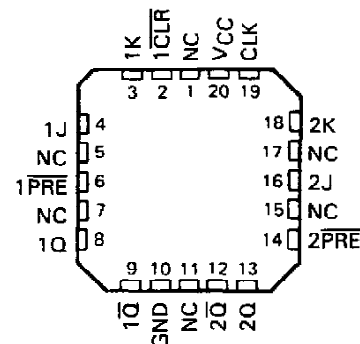
SN54LS114A, SN54S114 . . . J OR W PACKAGE
 SN74LS114A, SN74S114A . . . D OR N PACKAGE

(TOP VIEW)



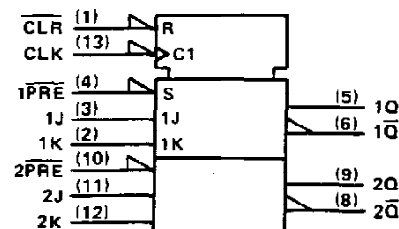
SN54LS114A, SN54S114 . . . FK PACKAGE

(TOP VIEW)



NC—No internal connection

logic symbol†



\dagger This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

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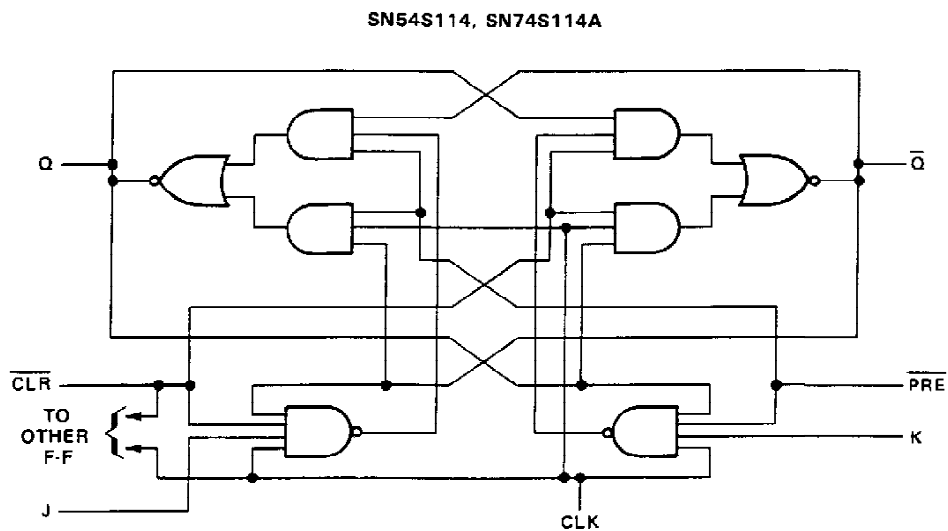
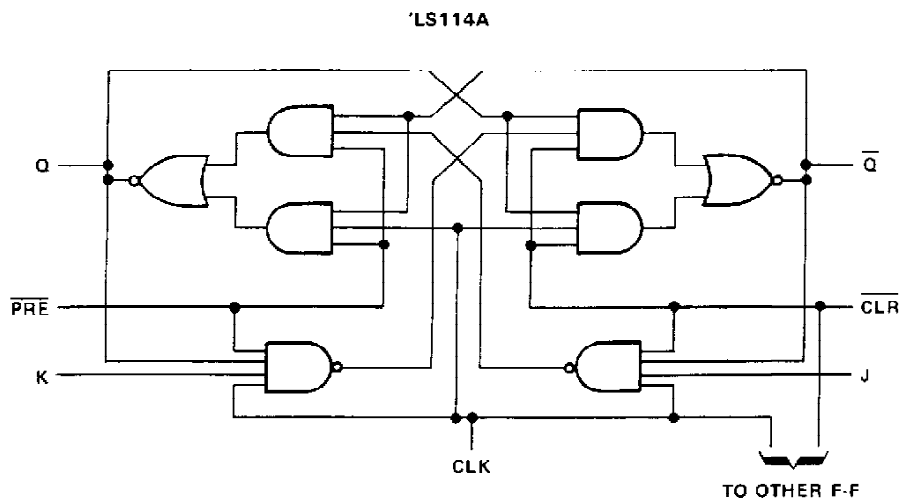
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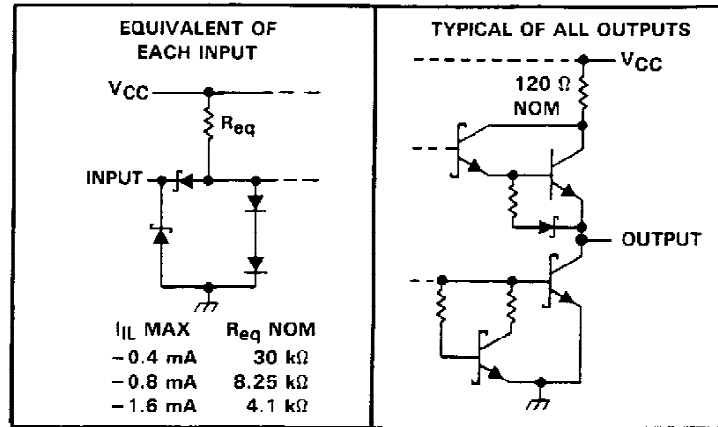
logic diagram (positive logic)



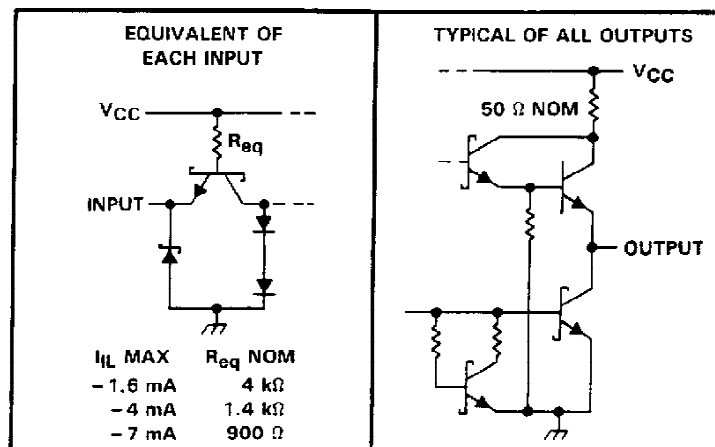
**SN54LS114A, SN54S114, SN74LS114A, SN74S114A
DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS
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schematics of inputs and outputs

'LS114A



SN54S114, SN74S114A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS114A	7 V
SN54S114, SN74S114A	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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SN54LS114A, SN74LS114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

			SN54LS114A			SN74LS114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
I _{OH}	High-level output current				-0.4			-0.4	mA
I _{OL}	Low-level output current				4			8	mA
f _{clock}	Clock frequency		0		30	0		30	MHz
t _w	Pulse duration	CLK	20			20			ns
		PRE or CLR low	25			25			
t _{su}	Set up time-before CLK↓	Data high or low	20			20			ns
		CLR inactive	25			25			
		PRE inactive	20			20			
t _h	Hold time-data after CLK↓		0			0			ns
T _A	Operating free-air temperature		-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS114A			SN74LS114A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA					-1.5			-1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA			2.5	3.4		2.7	3.4		V
V _{OL}		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA				0.25	0.4		0.25	0.4	V
		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA							0.35	0.5	
I _I	J or K	V _{CC} = MAX, V _I = 7 V					0.1			0.1	mA
	CLR						0.6			0.6	
	PRE						0.3			0.3	
	CLK						0.8			0.8	
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V					20			20	µA
	CLR						120			120	
	PRE						60			60	
	CLK						160			160	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V					-0.4			-0.4	mA
	CLR						-1.6			-1.6	
	PRE						-0.8			-0.8	
	CLK						-1.6			-1.6	
I _{OS} §		V _{CC} = MAX, See Note 2			-20		-100	-20		-100	mA
I _{CC} (Total)		V _{CC} = MAX, See Note 3				4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.



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SN54LS114A, SN74LS114A
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max}			$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	30	45		MHz
t_{PLH}	$\overline{\text{CLR}}$, $\overline{\text{PRE}}$ or CLK	Q or $\overline{\text{Q}}$			15	20	ns
t_{PHL}					15	20	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



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SN54S114, SN74S114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

			SN54S114			SN74S114A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				− 1			− 1	mA
I _{OL}	Low-level output current				20			20	mA
t _w	Pulse duration	CLK	6			6			ns
		CLK low	6.5			6.5			
		PRE or CLR low	8			8			
t _{su}	Setup time	Data high or low	7			7			ns
t _h	Hold time-data after CLK↓		0			0			ns
T _A	Operating free-air temperature		− 55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S114		SN74S114A		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN,	I _I = -18 mA	-1.2		-1.2		V
V _{OH}		V _{CC} = MIN, I _{OH} = -1 mA	V _{IH} = 2 V, V _{IL} = 0.8 V,	2.5	3.4	2.7	3.4	V
V _{OL}		V _{CC} = MIN, I _{OL} = 20 mA	V _{IH} = 2 V, V _{IL} = 0.8 V,	0.5		0.5		V
I _I		V _{CC} = MAX,	V _I = 5.5 V	1		1		mA
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V		50		50		μA
	CLR			200		200		
	PRE			100		100		
	CLK			200		200		
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.5 V		-1.6		-1.6		mA
	CLR			-14		-14		
	PRE			-7		-7		
	CLK			-8		-8		
I _{OS} §		V _{CC} = MAX		-40	-100	-40	-100	mA
I _{CC} #		V _{CC} = MAX, See Note 3		15	25	15	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Values are average per flip-flop.

NOTE 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 280 Ω, C _L = 15 pF	80	125		MHz
t _{PLH}	PRE or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$			4	7	ns
t _{PHL}	PRE or $\overline{\text{CLR}}$ (CLK high)	$\overline{\text{Q}}$ or Q			5	7	ns
	PRE or $\overline{\text{CLR}}$ (CLK low)				5	7	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$			4	7	ns
t _{PHL}					5	7	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



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